M52047SP

COLOR APERTURE IMPROVEMENT

DESCRIPTION

The M52047SP is a semiconductor integrated circuit for improving CTV color signal aperture. Circuit includes CAI (Color Aperture Improvement) and CNC (Color Noise Canceller).

FEATURES

- CAI improves color transient signal by switching three signals delayed by two delay lines for each B-Y and R-Y.
- Delay time adjustable via internal delay line.
- CAI can be adjusted by changing external voltage.
- No Y/C time lag between "CAI on mode" and "CAI off mode".
- CNC rejects color differential signal high frequency noise.

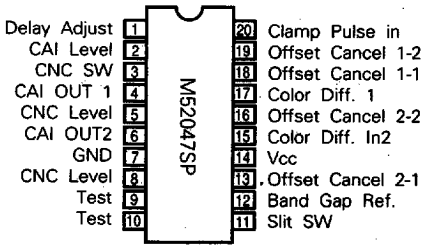
APPLICATION

Color Television

RECOMMENDED OPERATING CONDITION

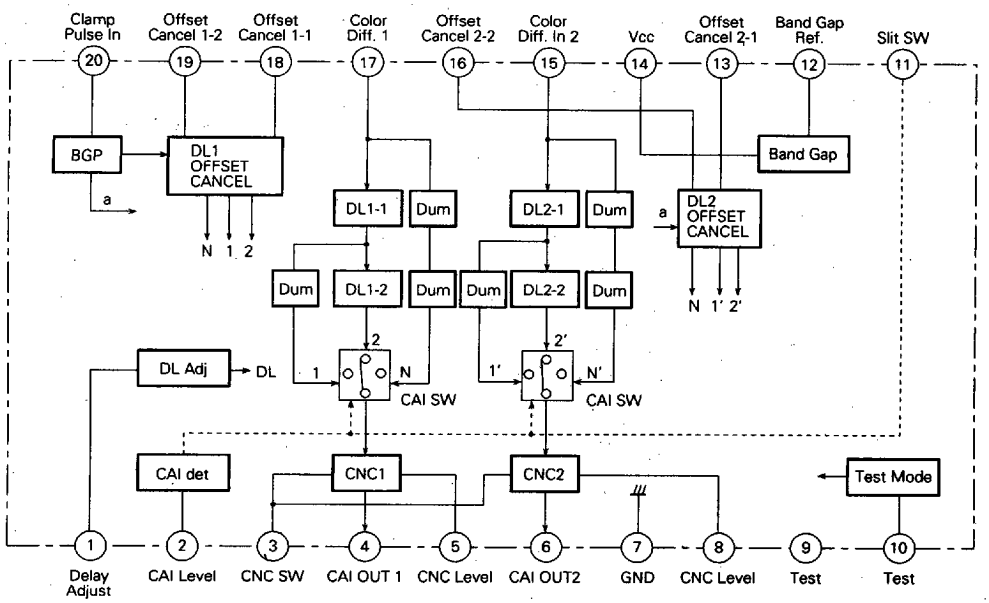
Supply Power Range ..... 8.5~13V
Rated Supply Voltage 12V

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13.5	V
P_d	Power dissipation	1000	mW
T_{opr}	Operating temperature	−20~65	°C
T_{stg}	Storage temperature	−40~125	°C
K_θ	Thermal derating (Ta≧25°C)	10	mW/°C
S_{urge}	Electrostatic discharge	±200	V

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5.000V unless otherwise noted)

Symbol	Parameter	Test point	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Circuit current	⑭	⑯ ⑰ with no input applied ① R=30KΩ ② OPEN ③ E_2=2V	25	40	55	mA
V_{12}	Pin 12 voltage	⑫	⑯ ⑰ with no input applied ① R=30KΩ ② OPEN ③ E_2=2V	4.2	6.1	8.0	V_{DC}
(delay)							
DL_{GN}	Gain N	④ ⑥	⑯ ⑰ 1kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF Nodelay mode	−1.5	−0.5	+1.0	dB
DL_{G1}	Gain 1	④ ⑥	⑯ ⑰ 1kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF 1delay mode	−1.5	−0.5	+1.0	dB
DL_{G2}	Gain 2	④ ⑥	⑯ ⑰ 1kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF 2delay mode	−1.5	−0.5	+1.0	dB
DL_{G3}	500kHz gain N	④ ⑥	⑯ ⑰ 500kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF Nodelay mode	−1.5	−0.5	+1.0	dB
DL_{G4}	500kHz gain 1	④ ⑥	⑯ ⑰ 500kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF 1delay mode	−2.7	−1.2	+0.3	dB
DL_{G5}	500kHz gain 2	④ ⑥	⑯ ⑰ 500kHz, 1.0V_{P-P} SG1 ① R=30KΩ CNC OFF 2delay mode	−3.7	−2.2	−0.7	dB
DL_{DN}	Low-range delay N	④ ⑥	⑯ ⑰ 100kHz, 1.0V_{P-P} SG1 ① R=30KΩ Rectangular wave CNC OFF Nodelay mode	30	80	130	nsec
DL_{D1}	Low-range delay 1	④ ⑥	⑯ ⑰ 100kHz, 1.0V_{P-P} SG1 ① R=30KΩ Rectangular wave CNC OFF 1delay mode	300	400	500	nsec
DL_{D2}	Low-range delay 2	④ ⑥	⑯ ⑰ 100kHz, 1.0V_{P-P} SG1 ① R=30KΩ Rectangular wave CNC OFF 2delay mode	550	750	950	nsec
DL_{DR}	Input dynamic range	④ ⑥	⑯ ⑰ 100kHz, SG1 ① R=30KΩ CNC OFF 1delay mode	1.2	1.7		V_{P-P}
V_{ON}	Output DC voltage N	④ ⑥	⑯ ⑰ with no input applied ① R=30KΩ CNC OFF Nodelay mode	2.1	3.1	4.1	V_{DC}
V_{01}	Output DC voltage 1	④ ⑥	⑯ ⑰ with no input applied ① R=30KΩ CNC OFF 1delay mode	2.1	3.1	4.1	V_{DC}
V_{02}	Output DC voltage 2	④ ⑥	⑯ ⑰ with no input applied ① R=30KΩ CNC OFF 2delay mode	2.1	3.1	4.1	V_{DC}
D_{OF1}	DC offset 1	④ ⑥	V_{ON}–V_{01}	−8	0	+8	mV_{DC}
D_{OF2}	DC offset 2	④ ⑥	V_{ON}–V_{02}	−8	0	+8	mV_{DC}
A_{OF1}	AC offset 1	④ ⑥	DL_{G1}–DL_{G2}	−0.2	0	+0.2	dB
A_{OF2}	AC offset 2	④ ⑥	DL_{G1}–DL_{G2}	−0.2	0	+0.2	dB
D_{OF1T}	DC offset 1 temperature dependency	④ ⑥	⑯ ⑰ with no input applied ① R=30KΩ CNC OFF Nodelay mode	−0.3	−0.1	+0.3	mV/°C
D_{OF2T}	DC offset 2 temperature dependency	④ ⑥	⑯ ⑰ with no input applied ① R=30KΩ CNC OFF 1delay mode	−0.3	−0.1	+0.3	mV/°C
(CAI det)							
CA_{RTT}	Rise improvement (Typ)	④ ⑥	⑯ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② OPEN CNC OFF	60	90	–	%

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
C_{ARTH}	Rise improvement (Max.)	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② 6V CNC OFF	65	95	–	%
C_{ARTL}	Rise improvement (Min.)	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② 1.2V CNC OFF	35	50	–	%
C_{AFTT}	Fall improvement (Typ)	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② OPEN	60	90	–	%
C_{AFTH}	Fall improvement (Max.)	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② 6V CNC OFF	65	95	–	%
C_{AFTL}	Fall improvement (Min.)	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② 1.2V CNC OFF	35	50	–	%
C_{AOFF}	CAI OFF mode	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② GND CNC OFF	–20	–	–	%
V_{CAMAX}	CAI Level Maximum threshold voltage	② ④ ⑥	⑲ ⑰ 1.0V_{P-P} SG3 ① R=30KΩ ② Variable CNC OFF	3.5	5.1	6.6	V_{DC}
CLP	Color fading prevention circuit operation	④ ⑥	⑲ ⑰ 1.0V_{P-P} SG4 ① R=30KΩ ② OPEN CNC OFF	–	2.5	3.3	μsec
(CNC)							
C_{G1}	Gain 1	④ ⑥	⑲ ⑰ 100kHz, 1.0V_{P-P} SG1 ① 30KΩ ③ 2V ⑤ ⑧ 150pF Nodelay mode	–1.5	–0.5	+1.0	dB
C_{G2}	Gain 2	④ ⑥	⑲ ⑰ 100kHz, 30mV_{P-P} SG1 ① 30KΩ ③ 2V ⑤ ⑧ 150pF Nodelay mode	–1.6	–0.6	+1.0	dB
C_{D1}	Depth 1	④ ⑥	⑲ ⑰ 800kHz, 1.0V_{P-P} SG1 ① R=30KΩ ③ 2V ⑤ ⑧ 150pF Nodelay mode	–1.6	–0.6	+1.0	dB
C_{D2}	Depth 2	④ ⑥	⑲ ⑰ 800kHz, 30mV_{P-P} SG1 ① R=30KΩ ③ 2V ⑤ ⑧ 150pF Nodelay mode	–6.4	–4.8	–3.3	dB
C_{OFF}	CNC OFF mode check	④ ⑥	⑲ ⑰ 800kHz, 30mV_{P-P} SG1 ① R=30KΩ ③ GND ⑤ ⑧ 150pF Nodelay mode	–1.5	–0.5	+1.0	dB
(Others)							
V_{BG}	BGP slice level	④ ⑥	⑲ ⑰ 100kHz, 1.0V_{P-P} SG1 ① R=30KΩ ③ GND ⑳ Voltage increase from 0V 1delay mode	1.5	2.4	5.0	V_{0-P}

SWITCH (SW) SETTING CONDITIONS

Symbol	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
I_{CC}	2	1	3	1	2	2	2	2	2
V_{12}	2	1	3	1	2	1	2	2	2
DLG_N	2	2	1	2	1	1	1	1	1
DLG_1	3	2	3	2	1	1	1	1	1
DLG_2	2	2	2	2	1	1	1	1	1
DLG_3	2	2	1	2	1	1	1	1	1
DLG_4	3	2	3	2	1	1	1	1	1
DLG_5	2	2	2	2	1	1	1	1	1
DL_{DN}	2	2	1	2	1	1	1	1	1
DL_{D1}	3	2	3	2	1	1	1	1	1
DL_{D2}	2	2	2	2	1	1	1	1	1
DL_{DR}	3	2	3	1	1	1	1	1	1
V_{ON}	2	2	1	1	2	1	2	2	2
V_{O1}	3	2	3	1	2	1	2	2	2
V_{O2}	2	2	2	1	2	1	2	2	2
D_{OF1}	2/3	2	1/3	1	2	1	2	2	2
D_{OF2}	2	2	1/2	1	2	1	2	2	2
A_{OF1}	2/3	2	1/3	2	2	1	2	2	2
A_{OF2}	2	2	1/2	2	2	1	2	2	2
D_{OF1T}	2/3	2	1/3	1	2	1	2	2	2
D_{OF2T}	2	2	1/2	1	2	1	2	2	2
CA_{RTT}	2	2	3	1	2	1	2	2	2
CA_{RTH}	1	2	3	1	2	1	2	2	2
CA_{RTL}	1	2	3	1	2	1	2	2	2
CA_{FTT}	2	2	3	1	2	1	2	2	2
CA_{FTH}	1	2	3	1	2	1	2	2	2
CA_{FTL}	2	2	3	1	2	1	2	2	2
CA_{OFF}	3	2	3	1	2	1	2	2	2
V_{CAMAX}	1	2	3	1	2	1	2	2	2
CLP	2	2	3	1	2	1	2	2	2
C_{G1}	2	1	1	1	2	1	2	2	2
C_{G2}	2	1	1	1	2	1	2	2	2
C_{D1}	2	1	1	1	2	1	2	2	2
C_{D2}	2	1	1	1	2	1	2	2	2
C_{OFF}	2	1	2	2	2	1	2	2	2
V_{BG}	3	2	3	1	2	1	2	2	2

ELECTRICAL CHARACTERISTICS TEST METHOD

Icc Measure current Icc flowing into pin ⑭ at no signal.

V_{12} Measure output DC voltage V_{12} on pin ⑫ at no signal.

DL_{GN} Measure 1kHz element V_3 at pin ⑥ (④) when pin ⑮ (⑰) input signal level is $1.0V_{P-P}$, and calculate DL_{GN} according to the following equation:

$$DL_{GN}=20 \log \frac{V_3}{1.0V_{P-P}} \text{ (dB)}$$

For Test Nos. 4 and 5, follow the above procedure in the same manner.

DL_{G3} Measure 500kHz element V_6 at pin ⑥ (④) when pin ⑮ (⑰) input signal level is $1.0V_{P-P}$, and calculate DL_{G3} according to the following equation.

$$DL_{G3}=20 \log \frac{V_6}{1.0V_{P-P}} \text{ (dB)}$$

For Test Nos. 7 and 8, follow the above procedure in the same manner.

DL_{DN} Measure the delay time $DL_{DN\ (nsec)}$ of 100kHz element at pin ⑥ (④) when pin ⑮ (⑰) input signal level is $1.0V_{P-P}$.
For Test Nos. 10 and 11, follow the above procedure in the same manner.

DL_{DR} The SG1 level when the output waveform at pin ⑥ (④) starts to be distorted with pin ⑮ (⑰) input signal SG1 level changed should be taken as DL_{DR}.

D_{OF1} Measure pin ④(⑥) DC voltage V_{on} in the No Delay mode and pin ④(⑥) DC voltage V_{01} in the 1-Delay mode at no signal, and calculate D_{OF1} according to the following equation.

$$D_{OF1}=V_{ON}-V_{01}(mV)$$

D_{OF2} Measure pin ④ (⑥) DC voltage V_{ON} in the No Delay mode and pin ④(⑥) DC voltage V_{02} in the 2-Delay mode at no signal, and calculate D_{OF2} according to the following equation.

$$D_{OF2}=V_{ON}-V_{02}(mV)$$

A_{OF1} Calculate A_{OF1} according to the following equation.

$$A_{OF1}=D_{G1}-D_{GN}(dB)$$

A_{OF2} Calculate A_{OF2} according to the following equation.

$$A_{OF2}=D_{G1}-D_{G2}(dB)$$

CA_{RTT} Measure 10 to 90% rise time $T_{22\text{-}1}$ at pin ④ (⑥) when pin ② is grounded and 10 to 90% rise time $T_{22\text{-}2}$ at pin ④ (⑥) when pin ② is open, and calculate CA_{RTT} according to the following equation.

$$CA_{RTT}=\frac{T_{22\text{-}1}-T_{22\text{-}2}}{T_{22\text{-}1}} \times 100 \ (\%)$$

CA_{RTH} Measure 10 to 90% rise time $T_{23\text{-}1}$ at pin ④ (⑥) when pin ② is grounded and 10 to 90% rise time $T_{23\text{-}2}$ at pin ④ (⑥)when pin ② voltage is 6V, and calculate CA_{RTH} according to the following equation.

$$CA_{RTH}=\frac{T_{23\text{-}1}-T_{23\text{-}2}}{T_{23\text{-}1}} \times 100 \ (\%)$$

CA_{RTL} Measure 10 to 90% rise time $T_{24\text{-}1}$ at pin ④(⑥) when pin ② is grounded and 10 to 90% rise time $T_{24\text{-}2}$ at pin ④ (⑥) when pin ② voltage is 1.2V, and calculate CA_{RTL} according to the following equation.

$$CA_{RTL}=\frac{T_{24\text{-}1}-T_{24\text{-}2}}{T_{24\text{-}1}} \times 100 \ (\%)$$

CA_{FTT} Measure 10 to 90% fall time $T_{25\text{-}1}$ at pin ④ (⑥) when pin ② is grounded and 10 to 90% fall time $T_{25\text{-}2}$ at pin ④ (⑥) when pin ② is open, and calculate CA_{FTT} according to the following equation.

$$CA_{FTT}=\frac{T_{25\text{-}1}-T_{25\text{-}2}}{T_{25\text{-}1}} \times 100 \ (\%)$$

CA_{FTH} Measure 10 to 90% fall time $T_{26\text{-}1}$ at pin ④ (⑥) when pin ② is grounded and 10 to 90% fall time $T_{26\text{-}2}$ at pin ④ (⑥) when pin ② voltage is 6V, and calculate CA_{FTH} according to the following equation.

$$CA_{FTH}=\frac{T_{26\text{-}1}-T_{26\text{-}2}}{T_{26\text{-}1}} \times 100 \ (\%)$$

COLOR APERTURE IMPROVEMENT

CA_{FTL} Measure 10 to 90% fall time $T_{27\text{-}1}$ at pin ④ (⑥) when pin ② is grounded and 10 to 90% fall time $T_{27\text{-}2}$ at pin ④ (⑥) when pin ② voltage is 1.2V, and calculate CA_{FTL} according to the following equation.

$$CA_{FTL}=\frac{T_{27\text{-}1}-T_{27\text{-}2}}{T_{27\text{-}1}}\times 100\ (\%)$$

CA_{OFF} Measure 10 to 90% rise time $T_{28\text{-}1}$ at pin ⑮ (⑰) when pin ② is grounded and 10 to 90% rise time $T_{28\text{-}2}$ at pin ④ (⑥), and calculate CA_{OFF} according to the following equation.

$$CA_{OFF}=\frac{T_{28\text{-}1}-T_{28\text{-}2}}{T_{28\text{-}1}}\times 100\ (\%)$$

V_{CAMAX} Increase pin ② voltage from the open voltage until the rise improvement becomes maximum.

CLP Reduce the SG4 time T_1 from 40μs: the time from rise to fall of SG4 when the color fading prevention circuit starts to operate should be taken as T_2.

C_{G1} Measure 100kHz element V_{31} at pin ⑥(④) when pin ⑮(⑰) input signal level is $1.0V_{P\text{-}P}$, and calculate C_{G1} according to the following equation.

$$C_{G1}=20\log\frac{V_{31}}{1.0V_{p\text{-}p}}\ (dB)$$

C_{G2} Measure 100kHz element V_{32} at pin ⑥(④) when pin ⑮(⑰) input signal level is $30mV_{P\text{-}P}$, and calculate C_{G2} according to the following equation.

$$C_{G2}=20\log\frac{V_{32}}{30mV_{p\text{-}p}}\ (dB)$$

C_{D1} Measure 800kHz element V_{33} at pin ⑥(④) when pin ⑮(⑰) input signal level is $1.0V_{P\text{-}P}$, and calculate C_{G3} according to the following equation.

$$C_{G3}=20\log\frac{V_{33}}{1.0V_{p\text{-}p}}\ (dB)$$

C_{D2} Measure 800kHz element V34 at pin ⑥ (④) when pin ⑮ (⑰) input signal level is $30mV_{P\text{-}P}$, and calculate C_{G4} according to the following equation.

$$C_{G4}=20\log\frac{V_{34}}{30mV_{p\text{-}p}}\ (dB)$$

C_{OFF} Measure 800kHz element V_{35} at pin ⑥(④) when pin ⑮(⑰) input signal level is $30mV_{P\text{-}P}$, and calculate C_{OFF} according to the following equation.

$$C_{OFF}=20\log\frac{V_{35}}{30mV_{p\text{-}p}}\ (dB)$$

V_{BG} Pin ㉑ voltage when the waveform at pin ⑥ (④) is outputted with SG2 increased from $0V_{P\text{-}P}$ should be taken as V_{BG}.

PRECAUTIONS FOR APPLICATION

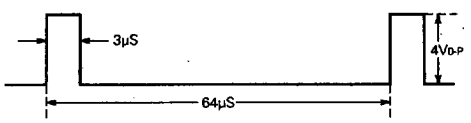
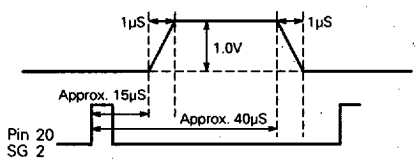
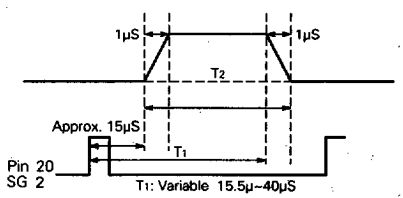
1. Pin ① delay adjusting resistor used should be less subjected to temperature changes and secular distortion.
2. Pins ⑬, ⑯, ⑱ and ⑲ are feedback terminals of the clamping circuit for canceling delay line I/O DC offset. Note leakage with other terminals and wiring.
3. Pin ① delay adjusting resistor is 30kΩ standard, but it should be adjusted for the optimum delay (1-delay: approx. 300~400nsec).
4. In this IC, there may occur a switching step difference by DC offset and AC offset.
   Noise may also occur in the edge near the sensor threshold. Before use, therefore, study this point carefully.

TEST CONDITIONS

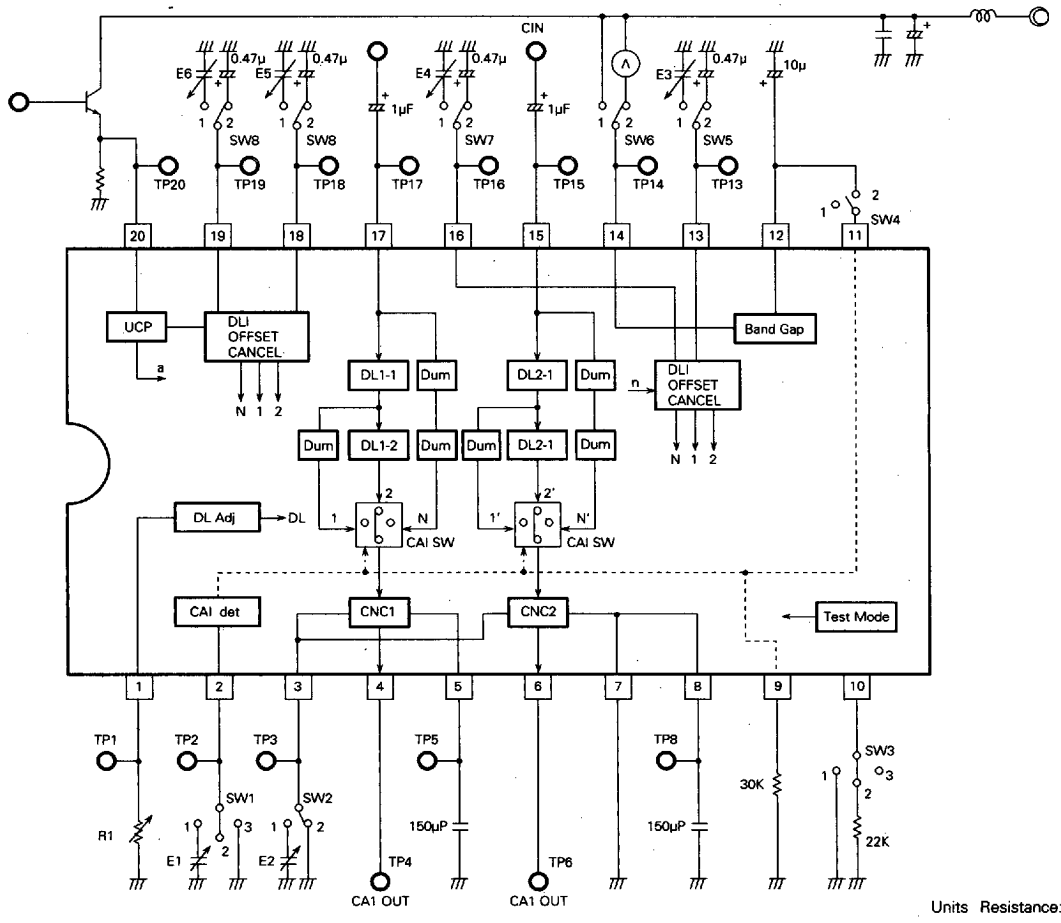
Nodelay mode	⑳ SG2, ② OPEN, ⑩ GND ⑪ V_{12}		
1delay mode	⑳ SG2, ② GND, ⑩ OPEN ⑪ OPEN		
2delay mode	⑳ SG2, ② GND, ⑩ 20KΩ ⑪ V_{12}		
CNC OFF mode	③ GND	CNC ON mode	③ 1.5V
E_3	Pin 13 voltage when pin 13 C=0.47μF and pin 20 SG2 are input		
E_4	Pin 16 voltage when pin 16 C=0.47μF and pin 20 SG2 are input		
E_5	Pin 18 voltage when pin 18 C=0.47μF and pin 20 SG2 are input		
E_6	Pin 19 voltage when pin 19 C=0.47μF and pin 20 SG2 are input		

NOTE 1: Each parameter should be the specified value at ambient temperature 25°C and supply voltage 12.0V DC.
NOTE 2: The direction of current flowing into the IC should be plus (+).
NOTE 3: Unless otherwise specified, SG2 at pin 20 is normally input.

INPUT SIGNAL

SG No.	Signals (50Ω termination)
SG1	Frequency: 1kHz to 1MHz Input level: 10mV$_{P-P}$ to 2.5V$_{P-P}$, sine and rectangular waves
SG2	
SG3	Input a waveform synchronous with SG2 into pins 15, 17. 
SG4	Input a waveform synchronous with SG2 into pins 15, 17. 

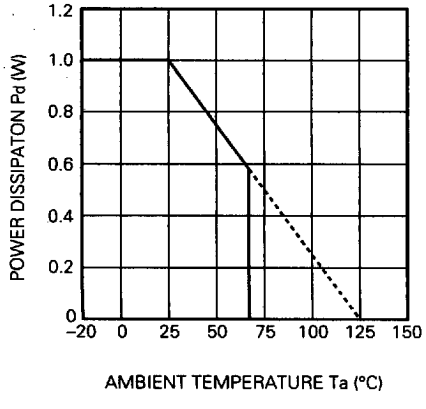
TEST CIRCUIT



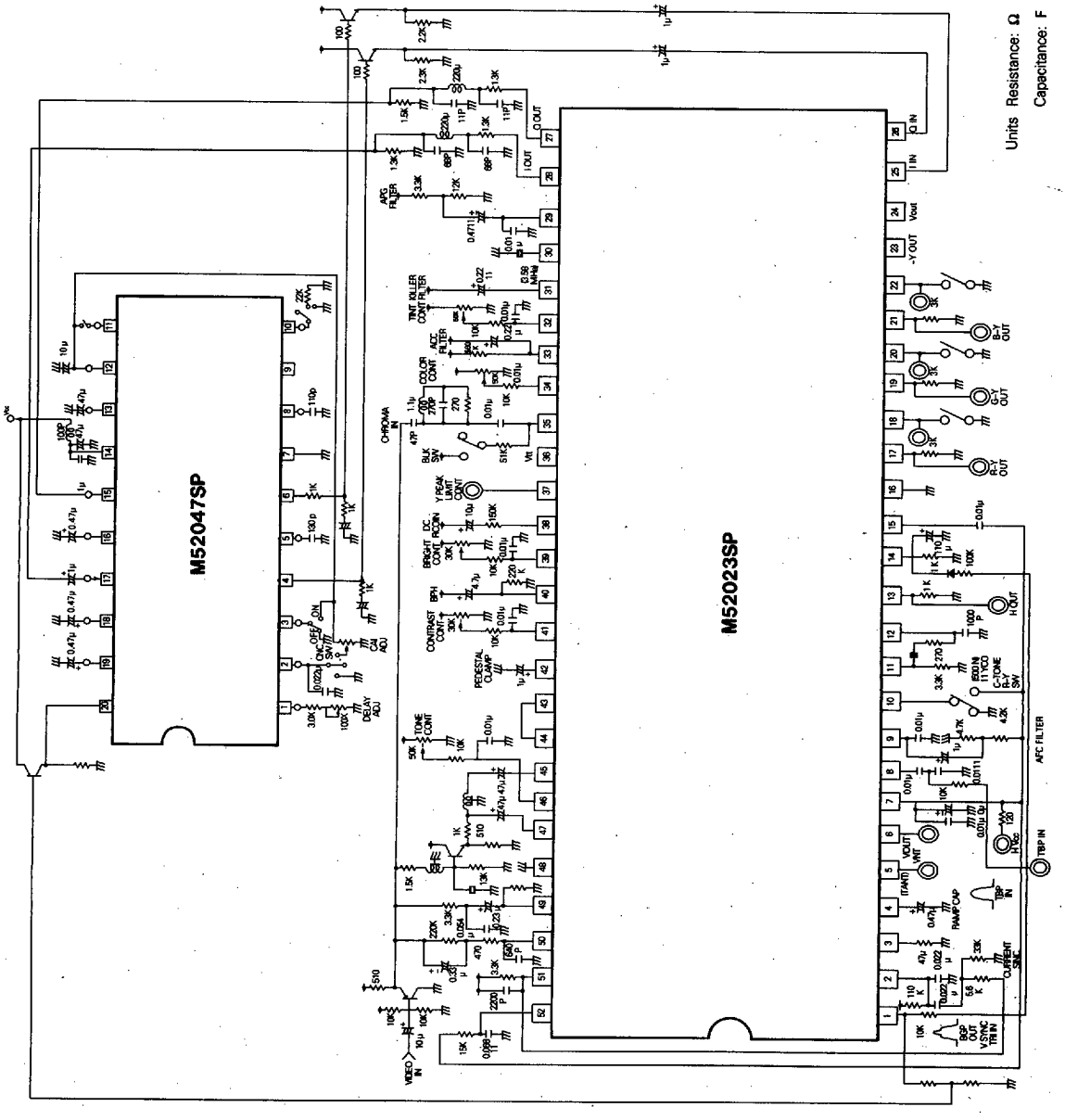
Units Resistance: Ω
Capacitance: F

TYPICAL CHARACTERISTICS

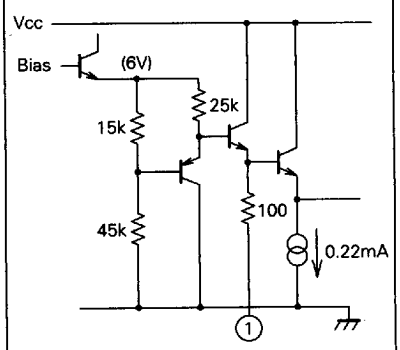
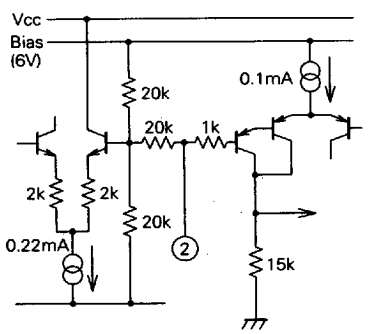
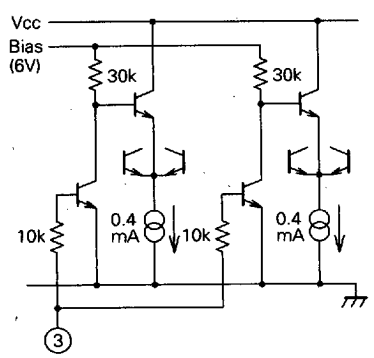
THERMAL DERATING (MAXIMUM RATING)



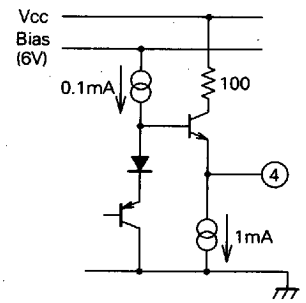
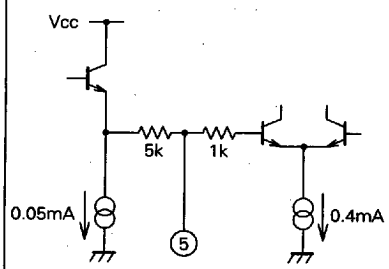
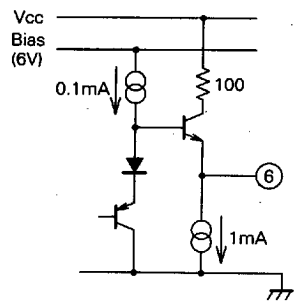
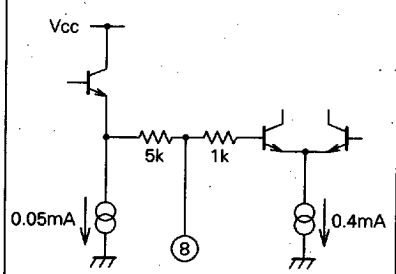
APPLICATION EXAMPLE



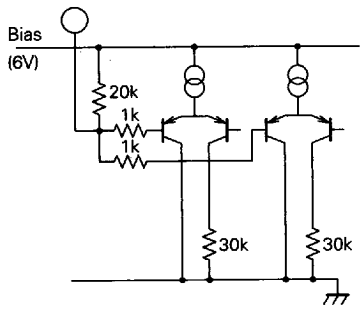
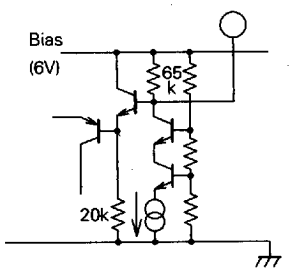
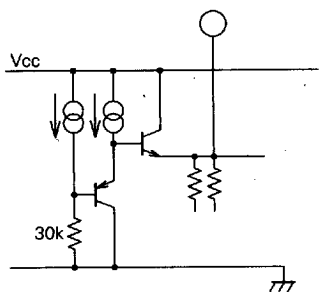
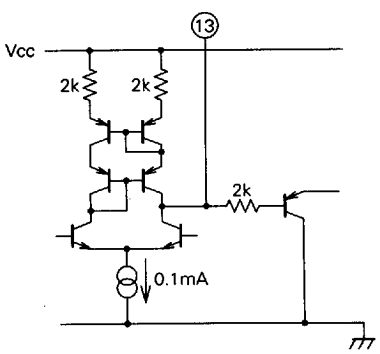
DESCRIPTION OF PIN

Pin No.	Name	Peripheral circuit of pins	Description of function
①	DLY Adj (4.5VDC)		Delay line fc and delay adjusting pin: Adjustment is required for 30kΩ standard.
②	CAI SW CAI Adj (4.3VDC) at OPEN		CAI effectiveness is adjusted. CAI is OFF at control voltage 0V to 6VDC, 0V. When "Hi" is selected, the CAI effect is enhanced.
③	CNC SW (open base input)		In "Hi" state (0.7V or more), CNC should be ON.

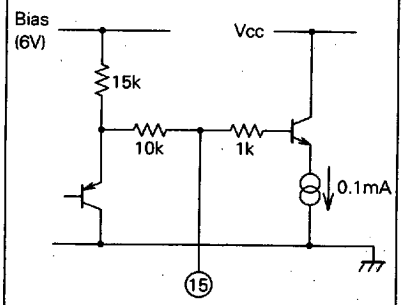
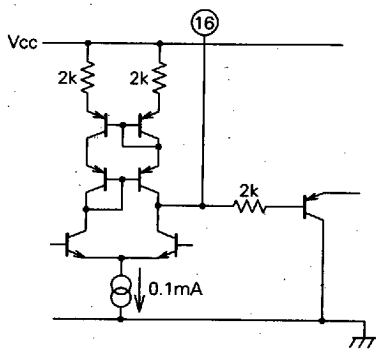
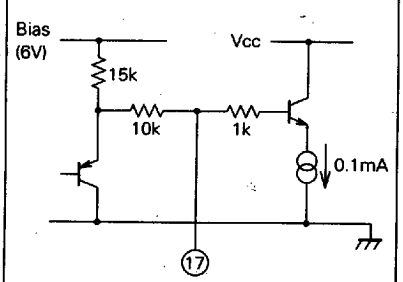
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Description of function
④	CAI Out 1 (3 VDC)		Chroma difference output
⑤	CNC Cap. (2.3VDC)		LPF fc adjusting pin: 150pF standard
⑥	CAI Out 2 (3VDC)		Chroma difference output
⑦	GND (0V)	——	Earth terminal
⑧	CNC Cap. (2.3VDC)		LPF fc adjusting pin: 150pF standard

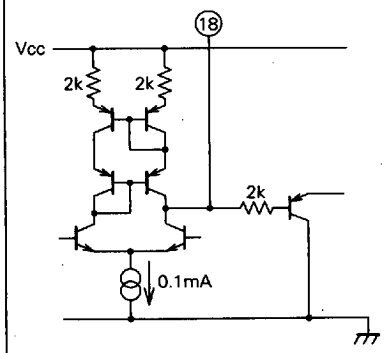
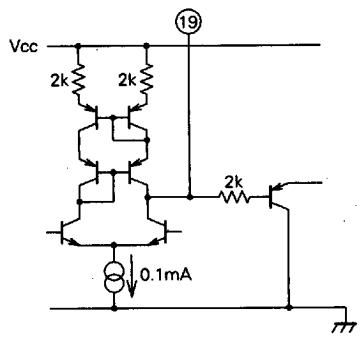
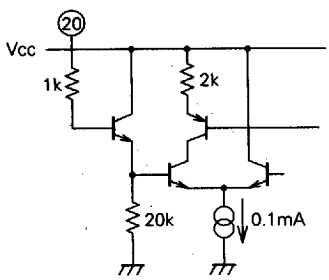
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Description of function
⑨	NC	——	Not connected
⑩	TEST (6VDC)		TEST mode setting Vth: 1/3V12; 2/3V12 L: nodelay M: 2 delay H: CAI ON
⑪	Slit Bias (5.4VDC)		OFF when high-frequency signal bias in the color fading prevention circuit is 6V
⑫	Band Gap (6VDC)		Regulated supply voltage pin
⑬	Offset Cancel 2–1 (4.1VDC)		Feedback pin of clamping circuit for canceling delay line I/O DC offset: Note leakage with other pins and wiring.

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Description of function
⑭	Vcc	———	Power supply 12V Supply voltage range 8.5 to 13.0V
⑮	Color Diff In 2 (3.0VDC)		Color difference input pin 0.8Vp-p (Typ.) Vp-p (Max.)
⑯	Offset Cancel 2–1 (4.1VDC)		Feedback pin of clamping circuit for canceling delay line I/O DC offset: Note leakage with other pins and wiring.
⑰	Color Diff In 1 (3.0VDC)		Color difference input pin 0.8Vp-p (Typ.) Vp-p (Max.)

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Description of function
⑱	Offset Cancel 1–1 (4.1VDC)		Feedback pin of clamping circuit for canceling delay line I/O DC offset: Note leakage with other pins and wiring.
⑲	Offset Cancel 1–2 (4.1VDC)		Feedback pin of clamping circuit for canceling delay line I/O DC offset: Note leakage with other pins and wiring.
⑳	BGP In (OPEN E base input)		BGP input pin 4Vo-p