M54927P

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

DESCRIPTION

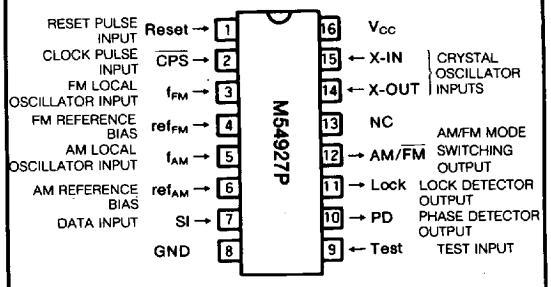
The M54927P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in AM/FM electronically tuned radio receivers. It makes use of ECL-IIL process to enable high density and low power consumption. It contains an FM Prescaler allowing the direct input of the local oscillator frequency signal.

The base frequency is provided by a 4.5MHz crystal oscillator.

FEATURES

- Built-in FM high-speed prescaler (f_{max}=130MHz)
- Low power consumption (I_{CC} = 20mA, typical at V_{CC} = 5V)
- Reference frequency selectable from eight values (100K, 50K, 25K, 12.5K, 10K, 9K, 5K, 1K)
- Modulo-2 swallow counter in FM mode (prescaler ratio 1/32, 1/33)
- Wide range of division ratios (FM=1024~65535, AM=32~2047, binary coded)
- Built-in 4.5MHz crystal oscillator (only two external components required)
- PLL lock/unlock status output
- AM/FM mode control output
- High sensitivity AM/FM local oscillator frequency input with built-in amplifier (FM: 160mV$_{P-P}$ at 130MHz, AM: 100mV$_{P-P}$ at 4MHz)
- Serial data input

PIN CONFIGURATION (TOP VIEW)



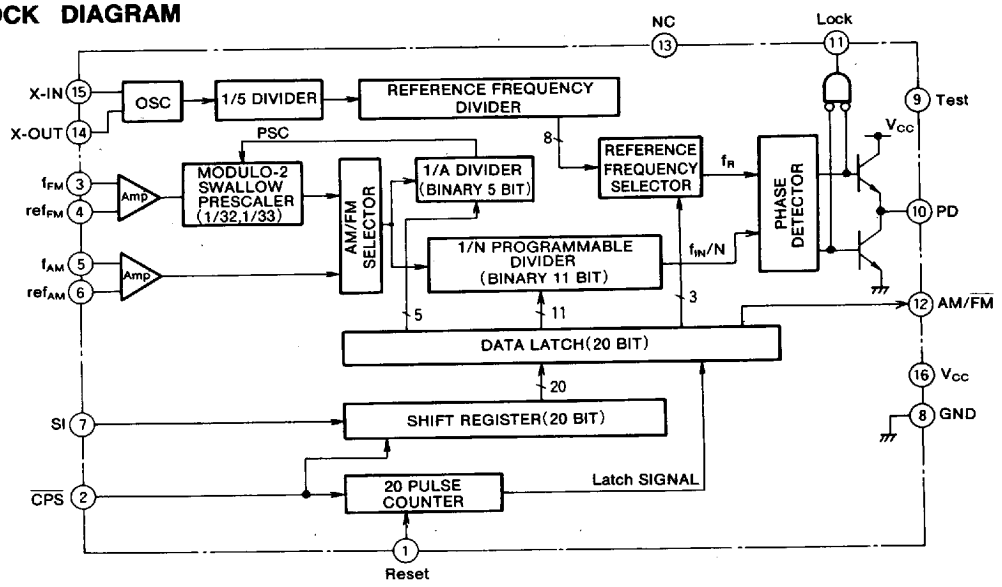
Outline 16P4

NC : No connection

APPLICATION

AM/FM Radios

BLOCK DIAGRAM



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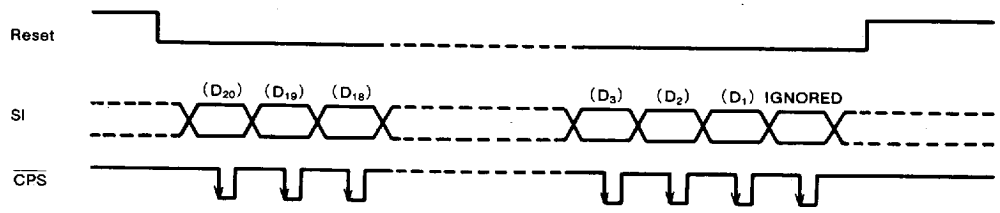
PIN DESCRIPTION

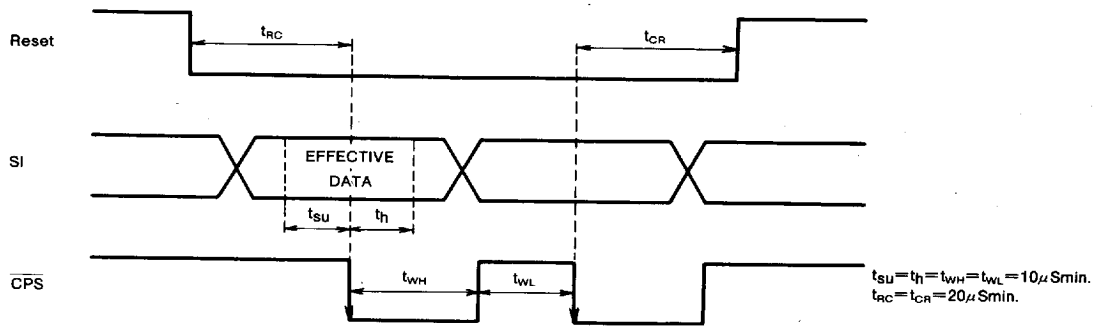
No.	Symbol	Name	Description
1	Reset	Reset pulse input	20 pulse counter reset pulse input
2	$\overline{CPS}$	Clock pulse input	Shift register clock pulse input
3	f_{FM}	FM local oscillator input	Direct input enable (f_{max}=130MHz) Built-in amplifier (input sensitivity 160mV_{P-P})
4	ref_{FM}	FM reference bias	Grounded through 1000pF capacitor
5	f_{AM}	AM local oscillator input	Built-in amplifier (input sensitivity 100mV_{P-P})
6	ref_{AM}	AM reference bias	Grounded through 10000pF capacitor
7	SI	Data input	Serial data input
8	GND	Ground	0V
9	Test	Test input	Normally, set to the low-state. When it is in the high-state, pin 10 (PD) becomes the reference frequency output and pin 11 (Lock) is the programmable divider output.
10	PD	Phase detector output	Tri-state output. High-state for phase lead, low state for phase lag and phase coincidence for high-Z.
11	Lock	Lock detector output	High-state when PD is high-Z. Low-state when PD is high or low state. Open collector output
12	AM/$\overline{FM}$	AM/FM mode switching output	Low for FM and High for AM. Open collector output
13	NC		No connection
14	X-OUT	Crystal oscillator inputs	4.5MHz Crystal
15	X-IN		
16	V_{CC}	Power supply	4.5~5.5V

DESCRIPTION OF OPERATION

1. Data Input

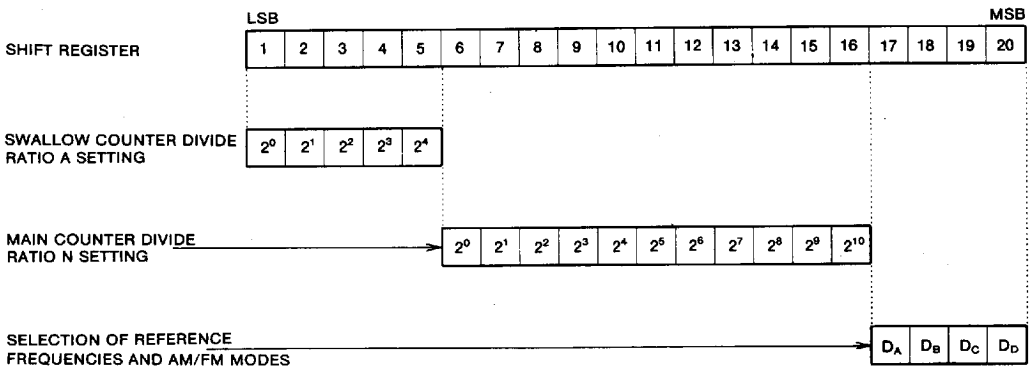


Note 1 : After the reset input goes low, 20 bits of data are read by means of 20 $\overline{CPS}$ input pulses (negative edge triggered).
2 : When the reset input is high, $\overline{CPS}$ input pulses and SI input data are ignored.
3 : After the twentieth $\overline{CPS}$ input pulse goes low, all date(Divide ratio, Mode and Reference frequency)are simultaneously set. Date for the 21 and following $\overline{CPS}$ input pulses are ignored.



PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

2. Data Coding



Note 4 : For FM mode, the programmable divider acts as a Modulo-2 swallow counter. The divide ratio is determined by the main counter divide ratio N (binary 11 bit) and the swallow counter divide ratio A (binary 5 bit). Overall divide ratio M is determined by M=A+32N.
5 : For AM mode, the programmable divider acts as a normal presettable counter. The divide ratio is given by N (binary 11 bit). For this mode, the swallow counter divide ratio A is ignored.
6 : The selection of reference frequencies and AM/FM modes is as described in Table 1.

Table 1. Reference frequency and AM/FM mode selection

Data				Mode	Reference	Test="H" (Note 7)	
D_A	D_B	D_C	D_D		frequency	PD	Lock
L	L	L	L	FM	100k	100k	f_{FM}/M
H	L	L	L	FM	50k	50k	f_{FM}/M
L	H	L	L	FM	25k	25k	f_{FM}/M
H	H	L	L	FM	12.5k	12.5k	f_{FM}/M
L	L	H	L	FM	10k	10k	f_{FM}/M
H	L	H	L	FM	9k	9k	f_{FM}/M
L	H	H	L	FM	5k	5k	f_{FM}/M
H	H	H	L	FM	1k	1k	f_{FM}/M
L	L	L	H	AM	100k	100k	f_{AM}/N
H	L	L	H	AM	50k	50k	f_{AM}/N
L	H	L	H	AM	25k	25k	f_{AM}/N
H	H	L	H	AM	12.5k	12.5k	f_{AM}/N
L	L	H	H	AM	10k	High	f_{AM}/N
H	L	H	H	AM	9k	Low	f_{AM}/N
L	H	H	H	AM	5k	High-Z	f_{AM}/N
H	H	H	H	AM	1k	High-Z	900kHz/N

Note 7 : When pin 9 (Test) is set to high-state, pin 10 (PD) is the reference frequency output and pin 11 (Lock) is the programmable divider output.

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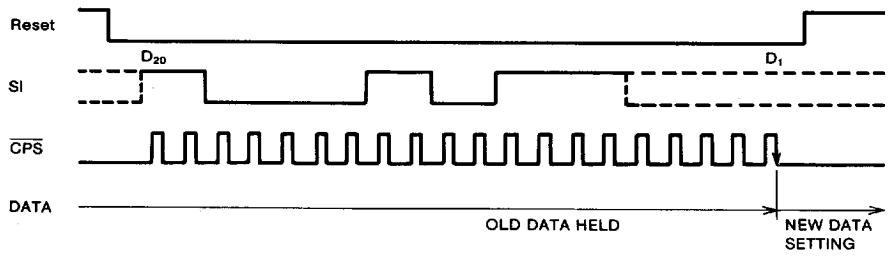
3. Data Coding Example

(1) AM mode, Reference frequency 10KHz, N=207

SHIFT REGISTER DATA

	LSB																		MSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	X	X	X	X	X	H	H	H	H	L	L	H	H	L	L	L	L	L	H	H
	SWALLOW COUNTER DIVIDE RATIO A IGNORED X : "H" or "L"					MAIN COUNTER DIVIDE RATIO N SETTING $N=2^0+2^1+2^2+2^3+2^6+2^7=207$											AM MODE REFERENCE FREQUENCY 10KHz IS SELECTED.			

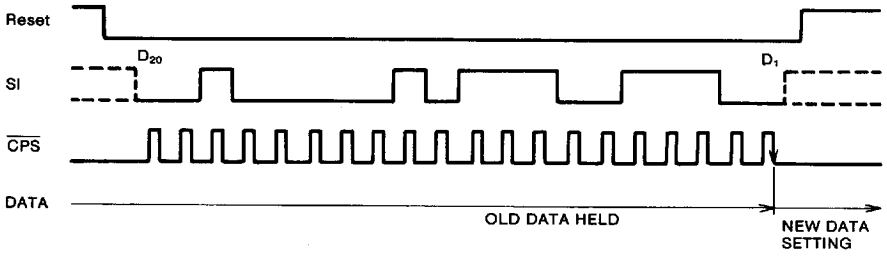


Note 8 : If the PLL goes into lock, $f_{AM}=10\times207=2070$KHz.

(2) FM Mode, Reference frequency 25KHz, N=2972

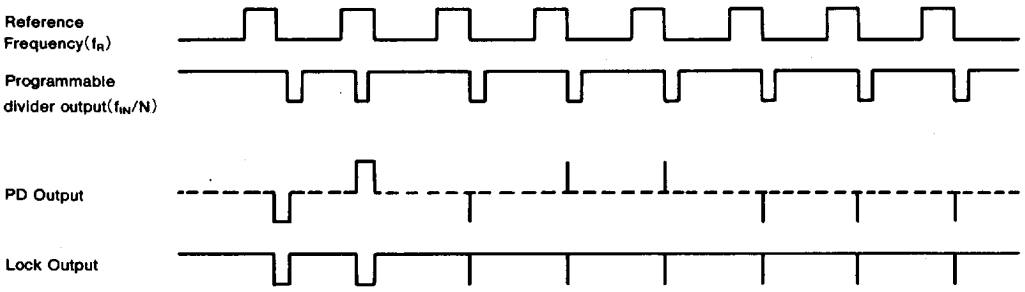
SHIFT REGISTER DATA

	LSB																		MSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	L	L	H	H	H	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	SWALLOW COUNTER DIVIDE RATIO A SETTING $A=2^2+2^3+2^4=28$					MAIN COUNTER DIVIDE RATIO N SETTING $N=2^2+2^3+2^4+2^6=92$											FM MODE REFERENCE FREQUENCY 25KHz IS SELECTED.			



Note 9 : Overall divide ratio M is given by $M=A+32N=28+32\times92=2972$.
10 : If the PLL goes into lock, $f_{FM}=25\times2972=74300$MHz
$=74.3$MHz.

4. PD and Lock signal Output



Note 11 : When the programmable divider output($f_{IN} \div N$) lags the reference frequency(f_R), the PD output is low. When it leads, the PD output becomes high.
12 : The broken line indicates the high impedance state.
13 : When PD is high or low state, Lock output becomes low.

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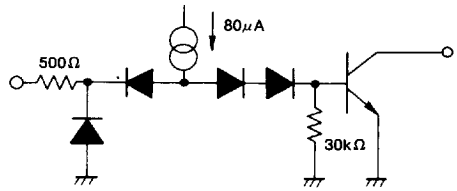
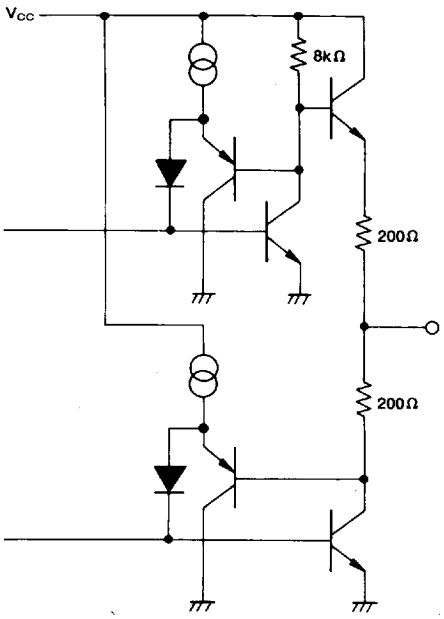
INPUT/OUTPUT CIRCUITS

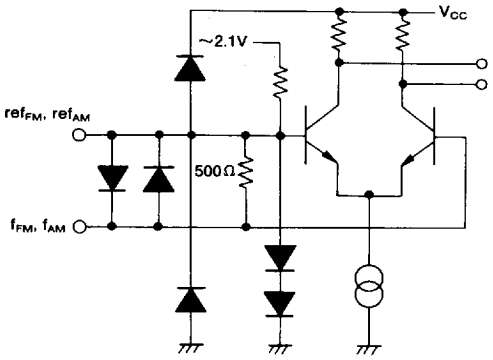
1 Reset, $\overline{CPS}$, SI, Test Inputs



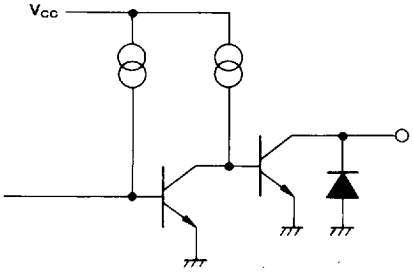
2 PO Output



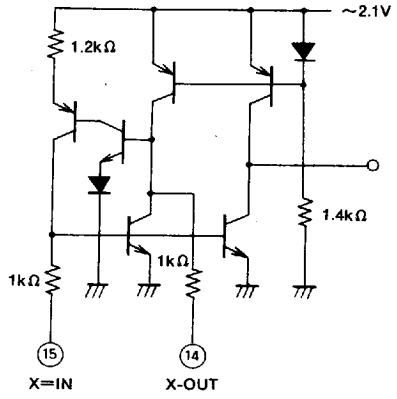
3 f_{FM}, f_{AM} Inputs



4 AM/$\overline{FM}$, Lock, 500Hz Outputs



5 OSC Circuit



Note 14 : Resistance and current values are typical values for Ta=25℃.

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ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

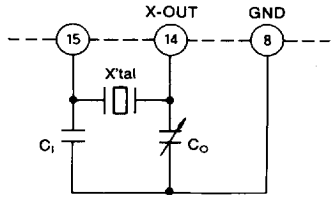
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+6	V
V_I	Input voltage		−0.5∼+6	V
V_O	Output voltage		−0.5∼+6	V
P_d	Power dissipation	T_a=75℃	300	mW
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5∼5.5V, T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.5 (3)*	5	5.5	V
f_{Local}	Input frequency	f_{AM} sinewave		0.5	—	4	MHz
		f_{FM} sinewave		8	—	130	
V_{Local}	Input amplitude	f_{AM}	0.5∼2MHz	200		800	mV_{P-P}
			2∼4MHz	100		800	
		f_{FM}	8∼60MHz	400		800	
			60∼130MHz	160		800	
I_{OL}	Low-level output current	Pin 12, 13 outputs			1	5	mA
f_{OSC}	Reference oscillator frequency				4.5		MHz

* : 3V, T_a=25℃

CRYSTAL ELEMENT CONNECTION CIRCUIT



Note 15 : Crystal specifications
Resonant frequency 4.5MHz±30ppm
Load capacitance 20pF
Effective resistance 100Ω max.
16 : Capacitance values
C_I=56pF
C_O=30pF(trimmer)

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	1, 2, 7, 9	V_{CC}=5.5V	2			V
V_{IL}	Low-level input voltage	1, 2, 7, 9	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	1, 2, 7, 9	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	1, 2, 7, 9	V_{CC}=4.5V, V_{IL}=0V		−80	−160	μA
V_{OL}	Low-level output voltage	11, 12	V_{CC}=4.5V, I_{OL}=5mA			0.5	V
V_{OHP1}	PD high-level output voltage	10	V_{CC}=4.5V, I_{OH}=−1mA	3			V
V_{OHP2}	PD high-level output voltage	10	V_{CC}=5V, I_{OH}=−0.1mA	4			V
V_{OLP1}	PD low-level output voltage	10	V_{CC}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output voltage	10	V_{CC}=5V, I_{OL}=0.1mA			1	V
I_{PD1}	PD leakage current	10	V_{CC}=5.5V, V_O=0.8∼4.7V			±1	μA
I_{PD2}	PD leakage current	10	V_{CC}=5V, V_O=2.5V			±100	nA
I_{CC}	Circuit current		V_{CC}=5.5V		20	35	mA
I_{OIK}	Output leakage current	11, 12	V_{CC}=5.5V, V_{OH}=5.5V			30	μA

Note 17 : All voltages are measured with respect to circuit ground (pin 8) at 0V.
18 : Currents are taken to be positive when flowing into the circuit and negative when flowing out of the circuit, the minimum and maximum values taken to be absolute values.
* : A Typical value at T_a=25℃.

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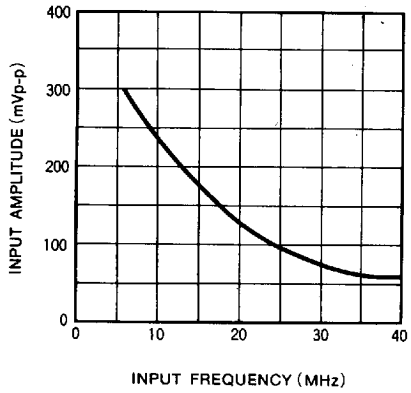
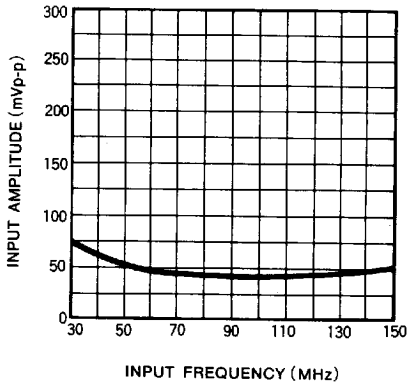
AC CHARACTERISTICS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{FM1}	FM input sensitivity	3	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=60\sim130MHz$			160	mV_{P-P}
V_{FM2}	FM input sensitivity	3	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=8\sim60MHz$			400	mV_{P-P}
V_{AM1}	AM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=2\sim4MHz$			100	mV_{P-P}
V_{AM2}	AM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=0.5\sim2MHz$			200	mV_{P-P}

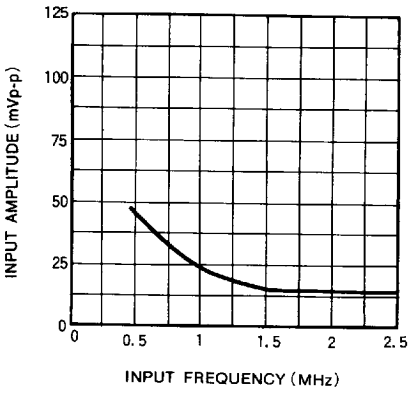
TYPICAL INPUT SENSITIVITY CHARACTERISTICS ($V_{CC1}=V_{CC2}=5V$, Ta=25℃)

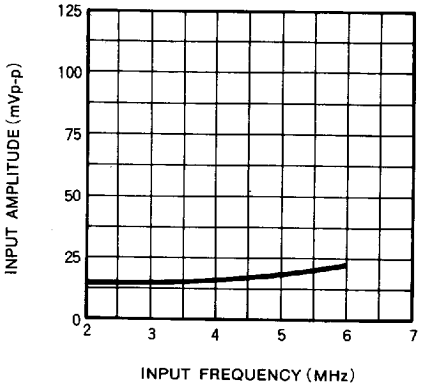
(1) MINIMUM FM INPUT AMPLITUDE VS INPUT FREQUENCY





(2) MINIMUM AM INPUT AMPLITUDE VS INPUT FREQUENCY





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APPLICATION EXAMPLE