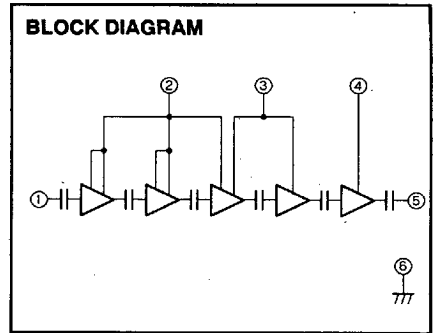
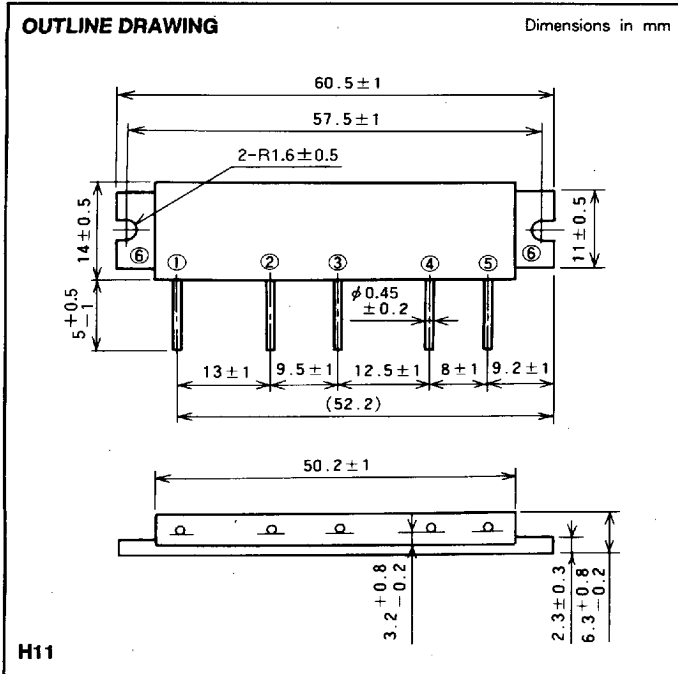


M57791

890-915MHz, 12.5V, 7W, FM MOBILE RADIO



- PIN :
- ① Pin : RF INPUT
 - ② Vcc1 : 1st. DC SUPPLY
 - ③ Vcc2 : 2nd. DC SUPPLY
 - ④ Vcc3 : 3rd. DC SUPPLY
 - ⑤ Po : RF OUTPUT
 - ⑥ GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1,2	Supply voltage		9	V
Vcc3		17	V	
Icc	Total current	ZG = ZL = 50 Ω	4	A
Pin(max)	Input power	ZG = ZL = 50 Ω, Vcc1 ≤ 8V	7	mW
Po(max)	Output power	ZG = ZL = 50 Ω	10	W
Tc(OP)	Operation case temperature		-30 to 110	°C
Tstg	Storage temperature		-40 to 110	°C

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

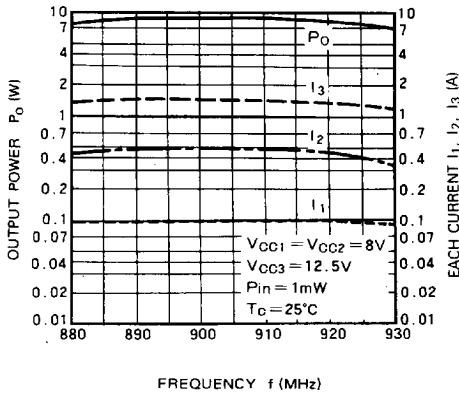
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range		890	915	MHz
Po	Output power	Vcc1 = Vcc2 = 8V, Vcc3 = 12.5V	7		W
ηT	Total efficiency	Pin = 1mW	35		%
2fo	2nd. harmonic	ZG = ZL = 50 Ω		-30	dBc
ρin	Input VSWR			2.8	-
-	Load VSWR tolerance	Vcc1 = Vcc2 = 8V, Vcc3 = 15.2V Po = 7W (Pin : controlled), ZG = 50Ω Load VSWR=20:1 (All phase), 5sec.	No degradation or destroy		-

Note. Above parameters, ratings, limits and conditions are subject to change.

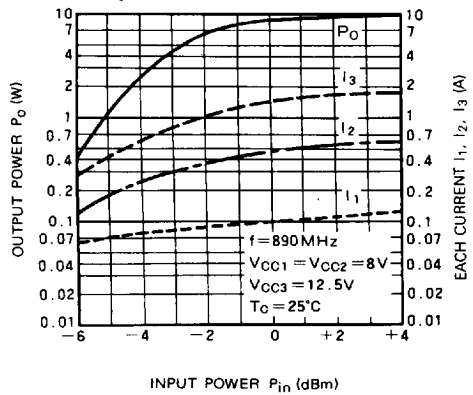


TYPICAL PERFORMANCE DATA

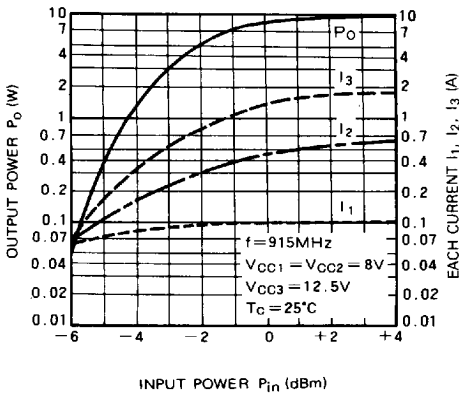
OUTPUT POWER, EACH CURRENT VS. FREQUENCY



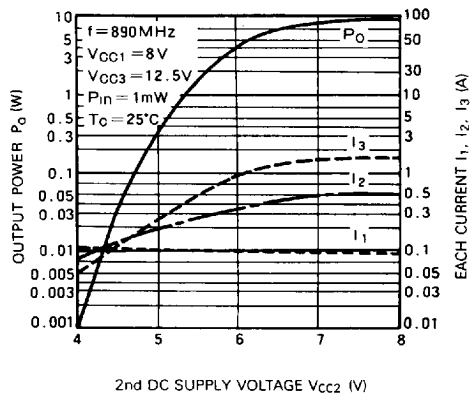
OUTPUT POWER, EACH CURRENT VS. INPUT POWER



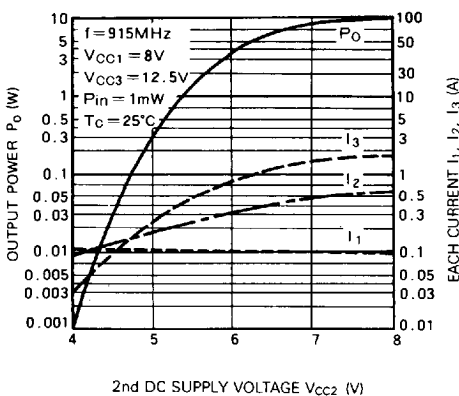
OUTPUT POWER, EACH CURRENT VS. INPUT POWER



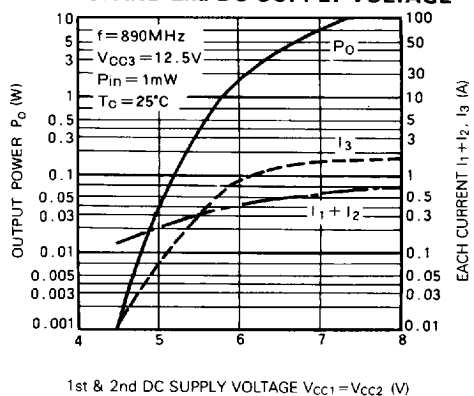
OUTPUT POWER, EACH CURRENT VS. 2nd DC SUPPLY VOLTAGE



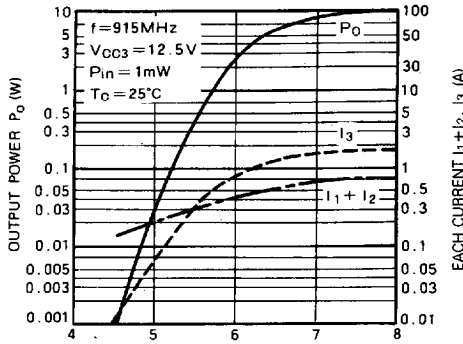
OUTPUT POWER, EACH CURRENT VS. 2nd DC SUPPLY VOLTAGE



OUTPUT POWER, EACH CURRENT VS. 1st AND 2nd DC SUPPLY VOLTAGE



OUTPUT POWER, EACH CURRENT VS. 1st AND 2nd DC SUPPLY VOLTAGE



1st & 2nd DC SUPPLY VOLTAGE $V_{cc1}=V_{cc2}$ (V)

Table 1: The conditions at standard operation

Stage	Vcc (V)	I_T (mA)	P_{in} (mW)	P_o (mW)
1st	8	45	1	20
2nd	8	80	20	200
3rd	8	160	200	500
4th	8	496	500	2000
5th	12.5	1100	2000	7000

DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to the following consideration when designing a heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistances between junction of incorporated transistors and case are shown in the followings.

- a) First stage transistor
 $R_{th(j-c)1} = 20^\circ\text{C/W}$ (Typ.)
- b) Second stage transistor
 $R_{th(j-c)2} = 17.5^\circ\text{C/W}$ (Typ.)
- c) Third stage transistor
 $R_{th(j-c)3} = 16^\circ\text{C/W}$ (Typ.)
- d) Fourth stage transistor
 $R_{th(j-c)4} = 9^\circ\text{C/W}$ (Typ.)
- e) Final stage transistor
 $R_{th(j-c)5} = 6.5^\circ\text{C/W}$ (Typ.)

(2) V_{CC} , I_T , RF input & output power conditions at standard operation for each stage transistors are estimated as follows.

$P_o = 7\text{W}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{CC3} = 12.5\text{V}$, $P_{in} = 1\text{mW}$, $\eta_T = 35\%$ (minimum ratings),

$I_{1+2} = 0.781\text{A}$ (Total current from 1st stage to 4th stage)

$I_3 = 1.1\text{A}$ (Current of 5th stage)

The conditions at standard operation for each stage transistors are shown in Table 1.

- Junction temperature of the first stage transistor
 $T_{j1} = (V_{CC1} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_c$ (Note 1)
 $= (8 \times 0.045 - 0.02 + 0.001) \times 20 + T_c$
 $= 6.8 + T_c$ ($^\circ\text{C}$)

Note 1: Case temperature of device

- Junction temperature of the second stage transistor
 $T_{j2} = (V_{CC1} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_c$
 $= (8 \times 0.08 - 0.2 + 0.02) \times 17.5 + T_c$

$= 8.1 + T_c$ ($^\circ\text{C}$)

- Junction temperature of the third stage transistor
 $T_{j3} = (V_{CC2} \times I_{T3} - P_{O3} + P_{O2}) \times R_{th(j-c)3} + T_c$
 $= (8 \times 0.16 - 0.5 + 0.2) \times 16 + T_c$
 $= 15.7 + T_c$ ($^\circ\text{C}$)
- Junction temperature of the fourth stage transistor
 $T_{j4} = (V_{CC2} \times I_{T4} - P_{O4} + P_{O3}) \times R_{th(j-c)4} + T_c$
 $= (8 \times 0.496 - 2 + 0.5) \times 9 + T_c$
 $= 22.2 + T_c$ ($^\circ\text{C}$)
- Junction temperature of the final stage transistor
 $T_{j5} = (V_{CC3} \times I_{T5} - P_o + P_{O4}) \times R_{th(j-c)5} + T_c$
 $= (12.5 \times 1.1 - 7 + 2) \times 6.5 + T_c$
 $= 56.9 + T_c$ ($^\circ\text{C}$)

2. Heat sink design

In thermal design of heat sink, keep the case temperature below 90°C at output power $P_o = 7\text{W}$ and ambient temperature = 60°C .

The thermal resistance $R_{th(c-a)}$ (Note 2) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_c - T_a}{(P_o/\eta_T) - P_o + P_{in}} = \frac{90 - 60}{(7/0.35) - 7 + 0.001} = 2.31$$

$(^\circ\text{C/W})$

Note 2: Including the contact thermal resistance between device and heat sink

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistor become;
 $T_{j1} = 97^\circ\text{C}$, $T_{j2} = 99^\circ\text{C}$, $T_{j3} = 106^\circ\text{C}$, $T_{j4} = 113^\circ\text{C}$, $T_{j5} = 147^\circ\text{C}$ at $T_a = 60^\circ\text{C}$, $T_c = 90^\circ\text{C}$.

Since the annual average of ambient temperature is 30°C , junction temperatures of each transistor become;

$T_{j1} = 67^\circ\text{C}$, $T_{j2} = 69^\circ\text{C}$, $T_{j3} = 76^\circ\text{C}$, $T_{j4} = 76^\circ\text{C}$, $T_{j5} = 117^\circ\text{C}$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensured.

