

M5M4256AP, J, L-85, -10, -12, -15

PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 18-pin plastic leaded chip carrier configuration and an increase in system densities. In addition to the $\overline{\text{RAS}}$ only refresh mode, the Hidden refresh mode and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode are available.

FEATURES

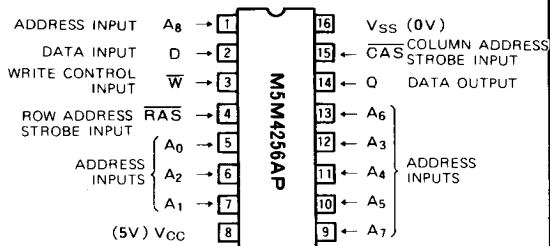
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4256AP, J, L-85	85	160	300
M5M4256AP, J, L-10	100	190	260
M5M4256AP, J, L-12	120	220	230
M5M4256AP, J, L-15	150	260	200

- Standard 16 pin DIP, 18 pin PLCC, 16 pin ZIP
- Single $5V \pm 10\%$ supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
 - M5M4256AP, J, L-85 385mW (max)
 - M5M4256AP, J, L-10 360mW (max)
 - M5M4256AP, J, L-12 330mW (max)
 - M5M4256AP, J, L-15 305mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, RAS-only-refresh, Page-mode capabilities
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms
- $\overline{\text{CAS}}$ controlled output allows hidden refresh

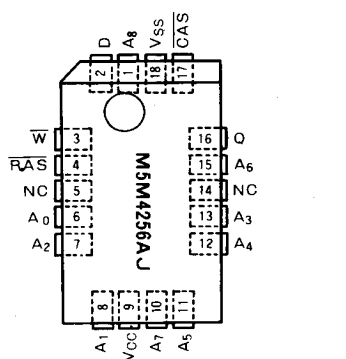
APPLICATION

Main memory unit for computers, Microcomputer

PIN CONFIGURATION (TOP VIEW)

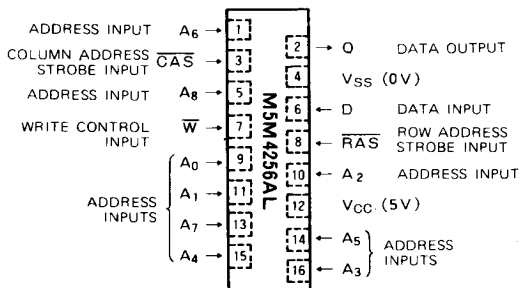


Outline 16P4H(DIP)



NC: NO CONNECTION

Outline 18P0A (PLCC)



Outline 16P5A (ZIP)

M5M4256AP, J, L-85, -10, -12, -15

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FUNCTION

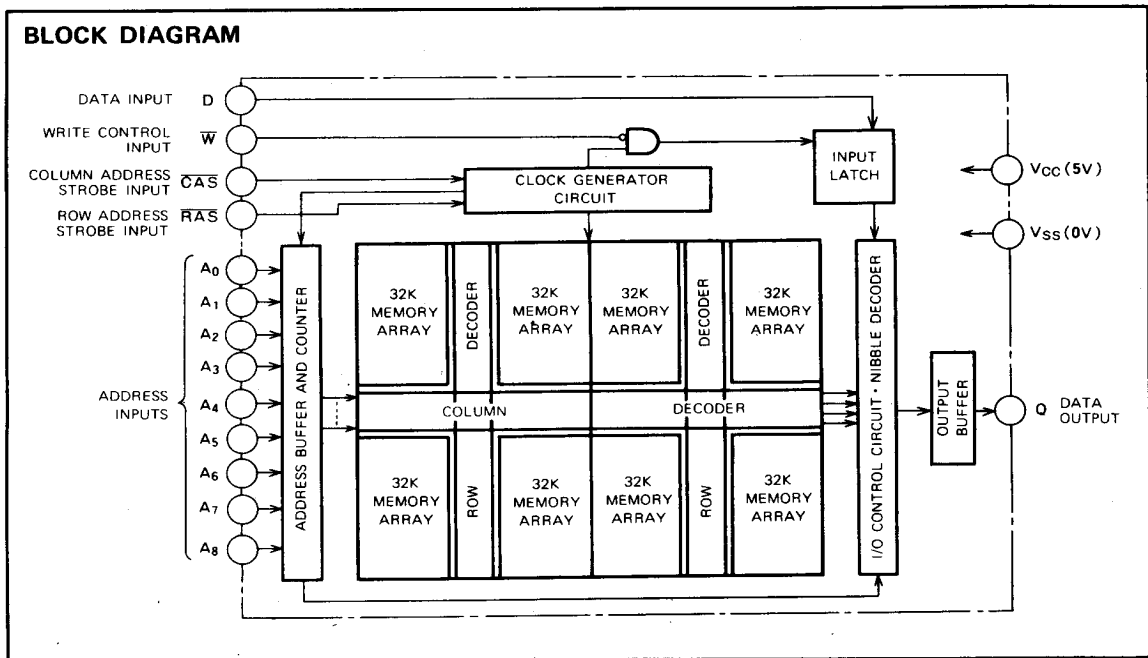
The M5M4256AP, J, L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

BLOCK DIAGRAM



PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current	$T_a = 25^\circ\text{C}$	50	mA
P_d	Power dissipation		1000	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65 ~ 150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	-2		0.8	V

Note 1: All voltage values are with respect to V_{SS} .

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	$I_{OH} = -5\text{mA}$	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2\text{mA}$	0		0.4	V
I_{OZ}	Off-state output current	Q floating $0\text{V} \leq V_{OUT} \leq 5.5\text{V}$	-10		10	μA
I_I	Input current	$0\text{V} \leq V_{IN} \leq V_{CC}$, Other input pins = 0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} , operating (Note 3, 4)	M5M4256AP, J, L-85			70	mA
		M5M4256AP, J, L-10			65	
		M5M4256AP, J, L-12			60	
		M5M4256AP, J, L-15			55	
I_{CC2}	Supply current from V_{CC} , standby	$\overline{RAS} = \overline{CAS} = V_{IH}$			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC} , refreshing (Note 3)	M5M4256AP, J, L-85			60	mA
		M5M4256AP, J, L-10			55	
		M5M4256AP, J, L-12			50	
		M5M4256AP, J, L-15			45	
$I_{CC4(AV)}$	Average supply current from V_{CC} , page mode (Note 3, 4)	M5M4256AP, J, L-85			55	mA
		M5M4256AP, J, L-10			50	
		M5M4256AP, J, L-12			45	
		M5M4256AP, J, L-15			40	
$I_{CC6(AV)}$	Average supply current from V_{CC} , $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4256AP, J, L-85			65	mA
		M5M4256AP, J, L-10			60	
		M5M4256AP, J, L-12			55	
		M5M4256AP, J, L-15			50	
$C_i(A)$	Input capacitance, address inputs	$V_I = V_{SS}$ $f = 1\text{MHz}$ $V_I = 25\text{mVrms}$			5	pF
$C_i(D)$	Input capacitance, data input				5	pF
$C_i(W)$	Input capacitance, write control input				7	pF
$C_i(RAS)$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_i(CAS)$	Input capacitance, $\overline{CAS}$ input				10	pF
C_o	Output capacitance	$V_O = V_{SS}$, $f = 1\text{MHz}$, $V_I = 25\text{mVrms}$			7	pF

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

M5M4256AP, J, L-85, -10, -12, -15**PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM****TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)**(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CRF}	Refresh cycle time	t _{REF}		4		4		4		4	ms
t _w (RASH)	RAS high pulse width	t _{RP}	65		80		90		100		ns
t _w (RASL)	RAS low pulse width	t _{RAS}	85	10000	100	10000	120	10000	150	10000	ns
t _w (CASL)	CAS low pulse width	t _{CAS}	45	10000	50	10000	60	10000	75	10000	ns
t _w (CASH)	CAS high pulse width (Note 8)	t _{CPN}	20		20		25		25		ns
t _h (RAS-CAS)	CAS hold time after RAS	t _{CSH}	85		100		120		150		ns
t _h (CAS-RAS)	RAS hold time after CAS	t _{RSR}	45		50		60		75		ns
t _d (CAS-RAS)	Delay time, CAS to RAS (Note 9)	t _{CRP}	10		10		10		10		ns
t _d (RAS-CAS)	Delay time, RAS to CAS (Note 10)	t _{RCD}	15	40	15	50	20	60	25	75	ns
t _{su} (RA-RAS)	Row address setup time before RAS	t _{ASR}	0		0		0		0		ns
t _{su} (CA-CAS)	Column address setup time before CAS	t _{ASC}	-5		-5		-5		-5		ns
t _h (RAS-RA)	Row address hold time after RAS	t _{RAH}	10		10		15		20		ns
t _h (CAS-CA)	Column address hold time after CAS	t _{CAH}	15		15		20		25		ns
t _h (RAS-CA)	Column address hold time after RAS	t _{AR}	55		65		80		100		ns
t _{THL}	Transition time	t _T	3	50	3	50	3	50	3	50	ns
t _{TLH}			3	50	3	50	3	50	3	50	ns

Note 5 An initial pause of 500μs is required after power-up followed by any eight RAS or RAS/CAS cycles before proper device operation is achieved.

6 The switching characteristics are defined as t_{THL} = t_{TLH} = 5ns.7 Reference levels of input signals are V_{IH min} and V_{IL max}. Reference levels for transition time are also between V_{IH} and V_{IL}.

8 Except for page-mode.

9 t_d(CAS-RAS) requirement is applicable for all RAS/CAS cycles.10 Operation within the t_d(RAS-CAS) max limit insures that t_a(RAS) max can be met. t_d(RAS-CAS) max is specified reference point only, ift_d(RAS-CAS) is greater than the specified t_d(RAS-CAS) max limit, then access time is controlled exclusively by t_a(CAS).t_d(RAS-CAS) min = t_h(RAS-RA) min + 2t_{THL}(t_{THL}) + t_{su}(CA-CAS) min.**SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)****Read Cycle**

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	t _{RC}	160		190		220		260		ns
t _{SU(R-CAS)}	Read setup time before CAS	t _{RCS}	0		0		0		0		ns
t _{H(CAS-R)}	Read hold time after CAS (Note 11)	t _{RCH}	0		0		0		0		ns
t _{H(RAS-R)}	Read hold time after RAS (Note 11)	t _{RRH}	10		10		10		10		ns
t _{DIS(CAS)}	Output disable time (Note 12)	t _{OFF}	0	20	0	25	0	30	0	35	ns
t _{A(CAS)}	CAS access time (Note 13)	t _{CAC}		45		50		60		75	ns
t _{A(RAS)}	RAS access time (Note 14)	t _{RAC}		85		100		120		150	ns

Note 11 Either t_h(RAS-R) or t_h(CAS-R) must be satisfied for a read cycle.12 t_{dis}(CAS) max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.13 This is the value when t_d(RAS-CAS) ≥ t_d(RAS-CAS) max. Test conditions, Load = 2TTL, C_L = 100pF.14 This is the value when t_d(RAS-CAS) < t_d(RAS-CAS) max. When t_d(RAS-CAS) ≥ t_d(RAS-CAS) max, t_a(RAS) will increase by the amount that t_d(RAS-CAS) exceeds the value shown. Test conditions, Load = 2TTL, C_L = 100pF.**Write Cycle**

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CW}	Write cycle time	t _{RC}	160		190		220		260		ns
t _{SU(W-CAS)}	Write setup time before $\overline{\text{CAS}}$ (Note 17)	t _{WCS}	−10		−10		−10		−10		ns
t _{H(CAS-W)}	Write hold time after $\overline{\text{CAS}}$	t _{WCH}	15		20		25		30		ns
t _{H(RAS-W)}	Write hold time after $\overline{\text{RAS}}$	t _{WCR}	55		70		85		105		ns
t _{H(W-RAS)}	$\overline{\text{RAS}}$ hold time after write	t _{RWL}	30		35		40		45		ns
t _{H(W-CAS)}	$\overline{\text{CAS}}$ hold time after write	t _{CWL}	30		35		40		45		ns
t _{W(W)}	Write pulse width	t _{WP}	15		20		25		30		ns
t _{SU(D-CAS)}	Data-in setup time before $\overline{\text{CAS}}$	t _{DS}	0		0		0		0		ns
t _{H(CAS-D)}	Data-in hold time after $\overline{\text{CAS}}$	t _{DH}	15		20		25		30		ns
t _{H(RAS-D)}	Data-in hold time after $\overline{\text{RAS}}$	t _{DHR}	55		70		85		105		ns



MITSUBISHI LSIs
M5M4256AP, J, L-85, -10, -12, -15

PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CRW}	Read-write cycle time (Note 15)	t _{RWC}	185		220		255		295		ns
t _{CRMW}	Read-modify-write cycle time (Note 16)	t _{RMWC}	195		235		265		310		ns
t _{h(W-RAS)}	RAS hold time after write	t _{RWL}	30		35		40		45		ns
t _{h(W-CAS)}	CAS hold time after write	t _{CWL}	30		35		40		45		ns
t _{W(W)}	Write pulse width	t _{WP}	15		20		25		30		ns
t _{SU(R-CAS)}	Read setup time before CAS	t _{RCS}	0		0		0		0		ns
t _{d(RAS-W)}	Delay time, RAS to write (Note 17)	t _{RWD}	70		90		110		135		ns
t _{d(CAS-W)}	Delay time, CAS to write (Note 17)	t _{CWD}	30		40		50		60		ns
t _{SU(D-W)}	Data-in setup time before write	t _{DS}	0		0		0		0		ns
t _{h(W-D)}	Data-in hold time after write	t _{DH}	15		20		25		30		ns
t _{dis(CAS)}	Output disable time	t _{OFF}	0	20	0	25	0	30	0	35	ns
t _{a(CAS)}	CAS access time (Note 13)	t _{CAC}		45		50		60		75	ns
t _{a(RAS)}	RAS access time (Note 14)	t _{RAC}		85		100		120		150	ns

Note 15: t_{CRW} min is defined as t_{CRW} min = $t_d(RAS-W)$ max + $t_d(CAS-W)$ min + $t_h(W-RAS)$ + $t_w(RASH)$ + $3t_{TLH}(t_{THL})$.

16: t_{CRMW} min is defined as t_{CRMW} min = $t_d(RAS)$ max + $t_h(W-RAS)$ + $t_w(RASH)$ + $3t_{TLH}(t_{THL})$.

17: $t_{su(W-CAS)}$, $t_d(RAS-W)$, and $t_d(CAS-W)$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_d(RAS-W) \geq t_d(RAS-W)$ min and $t_d(CAS-W) \geq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above (delayed write), the condition of data output (at access time and until CAS goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbo	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CPG}	Page-mode cycle time	t _{PC}	80		100		120		145		ns
t _{W(CASH)}	CAS high pulse width	t _{CP}	25		40		50		60		ns
t _{CPGRW}	Page-mode read-write cycle time	—	105		130		155		180		ns
t _{CPGRMW}	Page mode read-modify write cycle time	—	115		140		165		195		ns

CAS before RAS Refresh Cycle (Note 18)

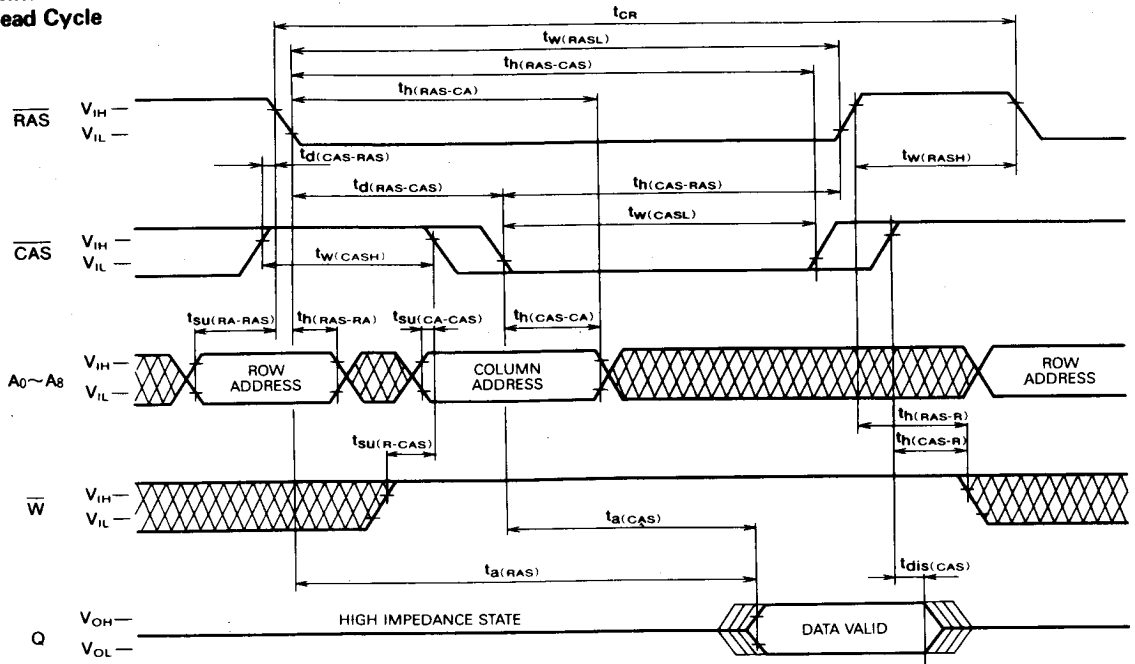
Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4256A-85		M5M4256A-10		M5M4256A-12		M5M4256A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{SUR(CAS-RAS)}	CAS setup time for auto refresh	t _{CSR}	10		10		10		10		ns
t _{HR(RAS-CAS)}	CAS hold time for auto refresh	t _{CHR}	15		20		25		30		ns
t _{dR(RAS-CAS)}	Precharge to CAS active time	t _{RPC}	0		0		0		0		ns

Note 18: Eight or more CAS before RAS cycles is necessary for proper operation of CAS before RAS refresh mode.

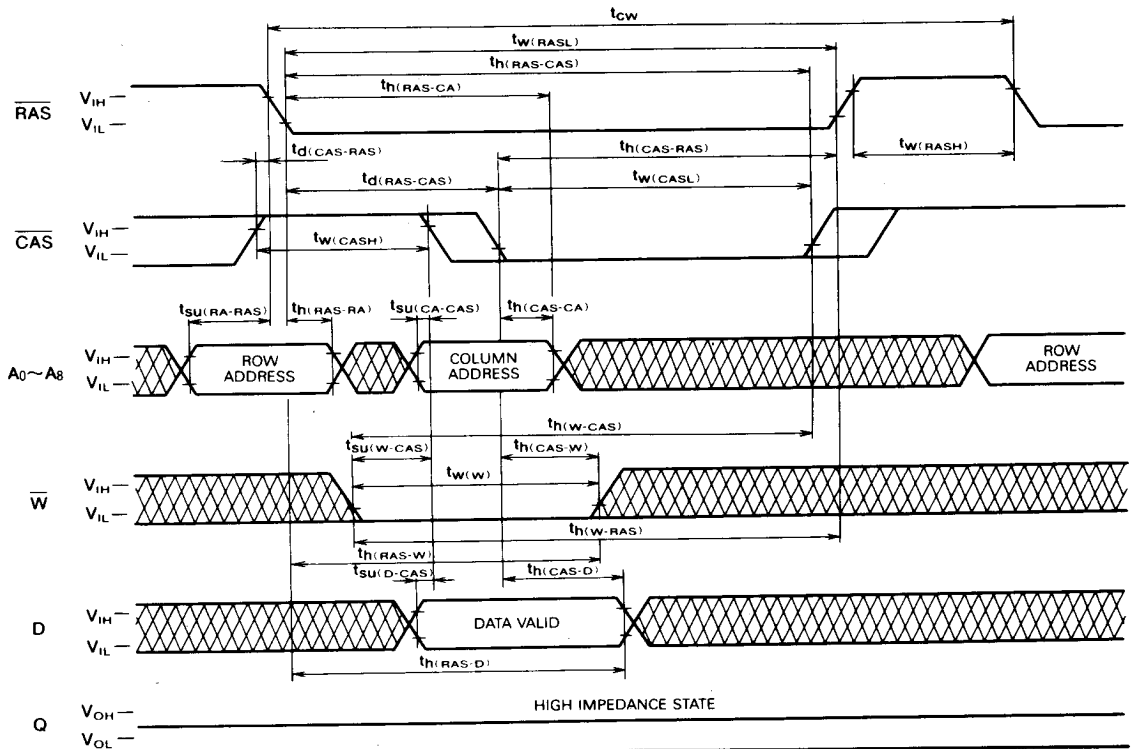
PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TIMING DIAGRAMS (Note 19)

Read Cycle

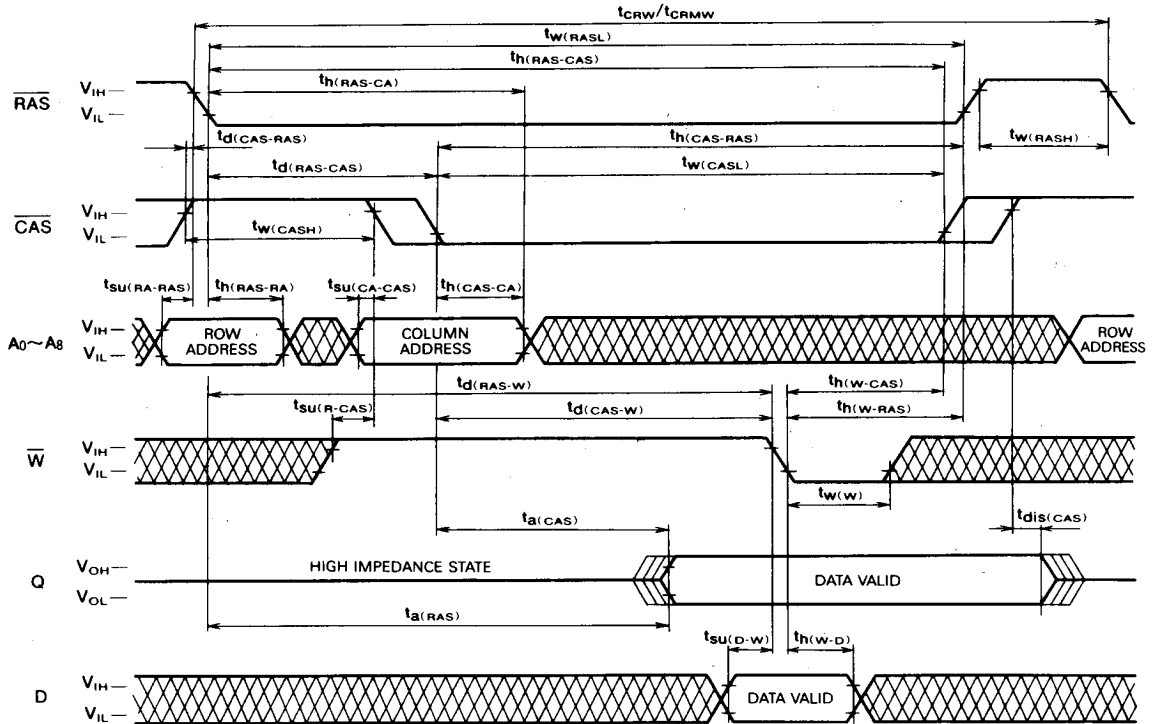


Write Cycle (Early Write)

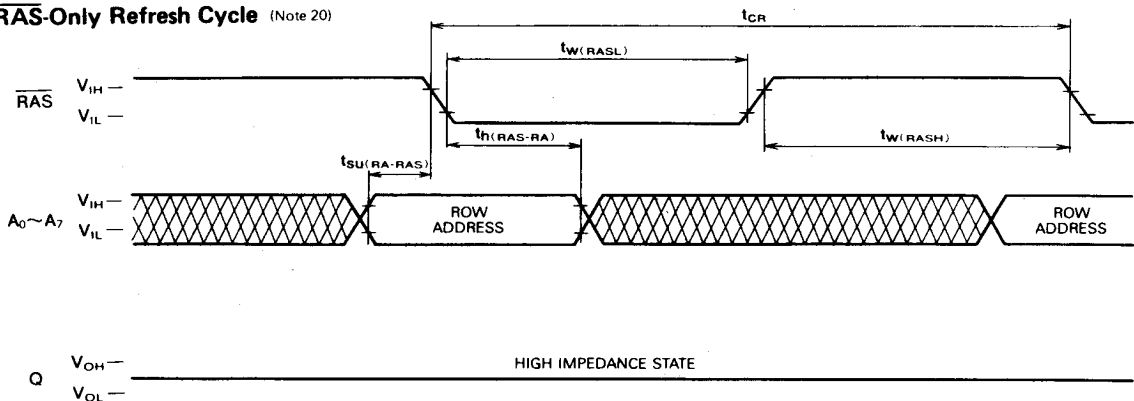


PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles



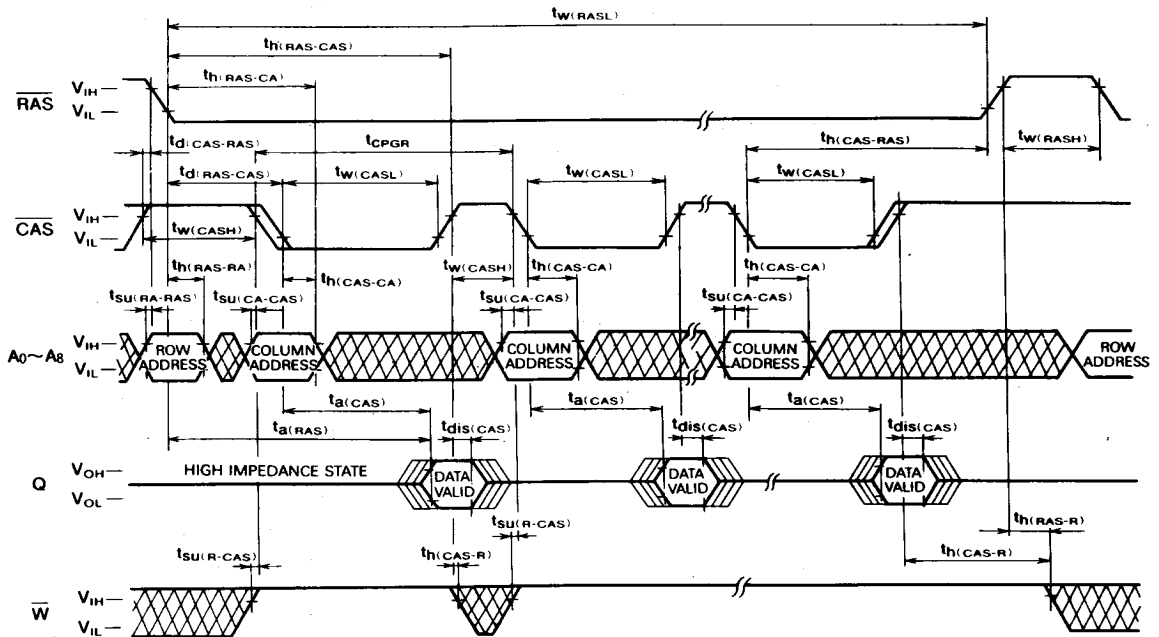
RAS-Only Refresh Cycle (Note 20)



Note 19. Indicates the don't care input.

The center-line indicates the high-impedance state.

Note 20. $\overline{CAS} = V_{IH}$, $\overline{W}$, $D =$ don't care.
 A_8 may be V_{IH} or V_{IL} .

PAGE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM**Page-Mode Read Cycle****Page-Mode Write Cycle**