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MITSUBISHI LSIs

M5M44256AP, J, L-8, -10, -12

T-45-23-17

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT) DYNAMIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{\text{RAS}}$ -only refresh mode, the hidden refresh mode and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode are available.

FEATURES

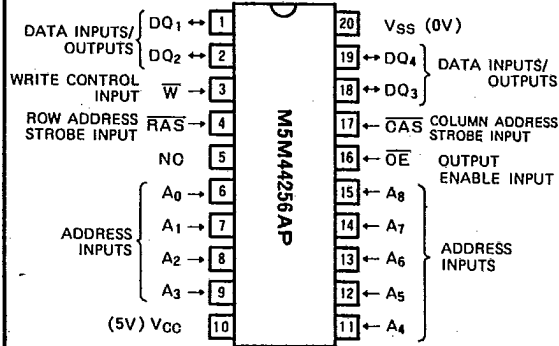
Type name	$\overline{\text{RAS}}$ access time (max. ns)	$\overline{\text{CAS}}$ access time (max. ns)	Address access time (max. ns)	$\overline{\text{OE}}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44256AJ-8 P L	80	20	40	20	160	200
M5M44256AJ-10 P L	100	25	50	25	190	175
M5M44256AJ-12 P L	120	30	60	30	220	150

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single $5V \pm 10\%$ supply
- Low standby power dissipation
2.75mW (Max) CMOS Input level
- Low operating power dissipation
M5M44256AP, J, L-8 385mW (Max)
M5M44256AP, J, L-10 330mW (Max)
M5M44256AP, J, L-12 275mW (Max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{\text{OE}}$ control output buffer impedance
- Read-Modify-write, $\overline{\text{RAS}}$ -only refresh, Fast-page mode capabilities
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode capability
- $\overline{\text{CAS}}$ controlled output allows hidden refresh
- Wide $\overline{\text{RAS}}$ low pulse width for Fast page mode . 50 μ s max

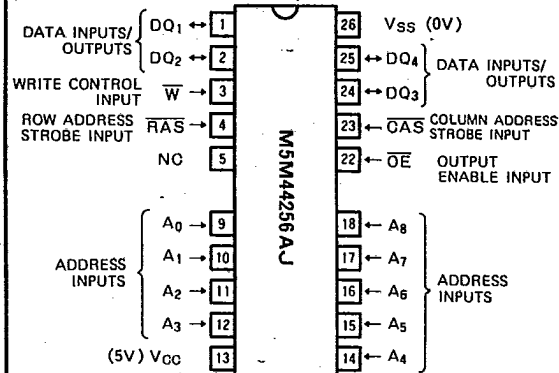
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

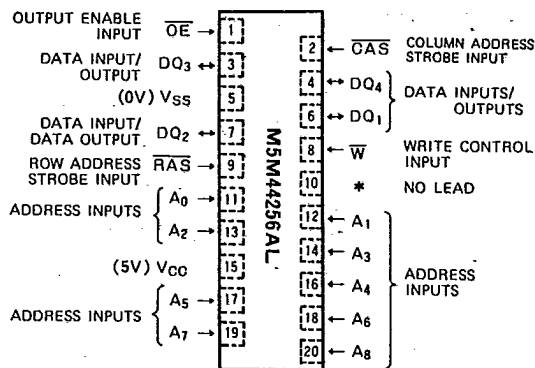
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L-A(ZIP)

NC: NO CONNECTION

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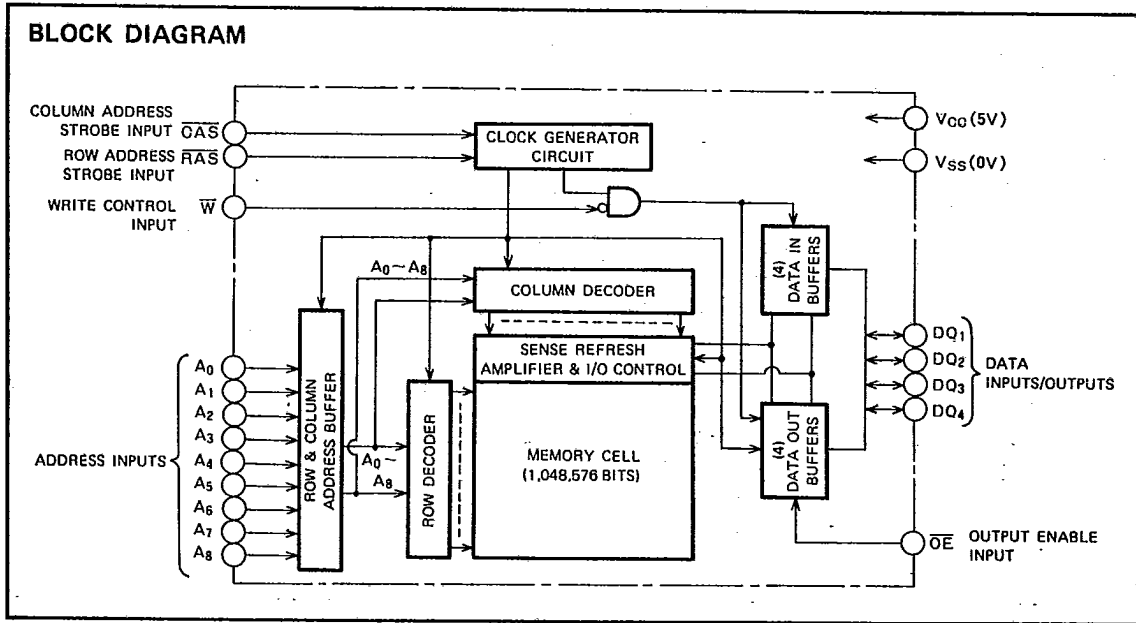
FUNCTION

The M5M44256AP, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	$\overline{\text{CAS}}$	W	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open



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FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}.**ELECTRICAL CHARACTERISTICS** (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current	0V ≤ V _{IN} ≤ 6.5V Other inputs pins = 0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} , operating (Note 3, 4)	M5M44256A-8	R _{AS} , C _{AS} cycling t _{RC} = t _{WC} = min, output open		70	mA
		M5M44256A-10			60	
		M5M44256A-12			50	
I _{CC2}	Supply current from V _{CC} , standby	R _{AS} = C _{AS} = V _{IH} , output open		2	mA	
		R _{AS} = C _{AS} = OE ≥ V _{CC} - 0.5, output open		0.5		
I _{CC3} (AV)	Average supply current from V _{CC} , refreshing (Note 3)	M5M44256A-8	R _{AS} cycling, C _{AS} = V _{IH} t _{RC} = min, output open		70	mA
		M5M44256A-10			60	
		M5M44256A-12			50	
I _{CC4} (AV)	Average supply current from V _{CC} , Fast-Page-Mode (Note 3, 4)	M5M44256A-8	R _{AS} = V _{IL} , C _{AS} cycling t _{PC} = min, output open		60	mA
		M5M44256A-10			50	
		M5M44256A-12			40	
I _{CC5} (AV)	Average supply current from V _{CC} , C _{AS} before R _{AS} refresh mode (Note 3)	M5M44256A-8	C _{AS} before R _{AS} refresh cycling t _{RC} = min, output open		70	mA
		M5M44256A-10			60	
		M5M44256A-12			50	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1}(AV), I_{CC3}(AV) and I_{CC4}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.**CAPACITANCE** (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs (Note 4')	V _I = V _{SS} f = 1MHz V _I = 25mVrms			5	pF
C _{I(OE)}	Input capacitance, OE input				7	pF
C _{I(W)}	Input capacitance, write control input				7	pF
C _{I(RAS)}	Input capacitance, R _{AS} input				7	pF
C _{I(CAS)}	Input capacitance, C _{AS} input				7	pF
C _{I/O}	Input/Output capacitance, data ports				7	pF

Note 4': C_{I(A)} of ZIP is 6pF (max).

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Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from \overline{CAS} (Note 6, 7)		20		25		30	ns
t_{RAO}	Access time from \overline{RAS} (Note 6, 8)		80		100		120	ns
t_{OAA}	Column Address access time (Note 6, 9)		40		50		60	ns
t_{CPA}	Access time from \overline{CAS} precharge (Note 6, 10)		45		55		65	ns
t_{OEA}	Access time from \overline{OE} (Note 6)		20		25		35	ns
t_{CLZ}	Output low impedance time from \overline{CAS} low (Note 6)	5		5		5		ns
t_{OFF}	Output disable time after \overline{CAS} high (Note 11)	0	20	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high (Note 11)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500 μ s is required after power-up followed by any 8 \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.

Note that \overline{RAS} may be cycled during the initial pause. And any 8 \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of \overline{RAS} inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assume that $t_{RCD(max)} \leq t_{RCD}$ and $t_{RAD(max)} \geq t_{RAD}$.

8: Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.

9: Assume that $t_{RCD} - t_{RAD} \leq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geq t_{RCD(max)}$.

10: Assume that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11: $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10\mu\text{A}$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, unless otherwise noted, See notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		8		8		8	ms
t_{RP}	\overline{RAS} high pulse width	70		80		90		ns
t_{RCD}	Delay time, \overline{RAS} low to \overline{CAS} low (Note 14)	25	60	25	75	25	90	ns
t_{CRP}	Delay time, \overline{CAS} high to \overline{RAS} low (Note 15)	10		10		10		ns
t_{CPN}	\overline{CAS} high pulse width (Note 16)	35		35		35		ns
t_{RAD}	Column address delay time from \overline{RAS} low (Note 17)	20	40	20	50	20	60	ns
t_{ASR}	Row address setup time before \overline{RAS} low	0		0		0		ns
t_{ASC}	Column address setup time before \overline{CAS} low (Note 18)	0	15	0	20	0	25	ns
t_{RAH}	Row address hold time after \overline{RAS} low	15		15		15		ns
t_{CAH}	Column address hold time after \overline{CAS} low or \overline{W} low	20		20		20		ns
t_T	Transition time (Note 19)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed $t_T = 5\text{ns}$.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 7, 9.

15: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for t_{CP} of fast page mode cycle.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.

18: $t_{ASC(max)}$ is specified as a reference point only of address access time.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

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Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	160		190		220		ns
t _{RAS}	RAS low pulse width	80	10000	100	10000	120	10000	ns
t _{CAS}	CAS low pulse width	20	10000	25	10000	30	10000	ns
t _{CSH}	CAS hold time after RAS low	80		100		120		ns
t _{RSH}	RAS hold time after CAS low	20		25		30		ns
t _{ROS}	Read Setup time before CAS low	0		0		0		ns
t _{RCH}	Read hold time after CAS high (Note 20)	0		0		0		ns
t _{RRH}	Read hold time after RAS high (Note 20)	10		10		10		ns
t _{RAL}	Column address to RAS setup time	40		50		60		ns
t _{RPC}	Precharge to CAS active time	0		0		0		ns
t _{h(OLOE)}	OE hold time after CAS low	20		25		30		ns
t _{h(RLOE)}	OE hold time after RAS low	80		100		120		ns
t _{DOEL}	Delay time, Data to OE low	0		0		0		ns
t _{OEHD}	Delay time, OE high to Data	15		20		25		ns
t _{h(OECH)}	CAS hold time after OE low	20		25		30		ns
t _{h(OERH)}	RAS hold time after OE low	20		25		30		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.**Write Cycle (Early Write and Delayed Write)**

Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	160		190		220		ns
t _{RAS}	RAS low pulse width	80	10000	100	10000	120	10000	ns
t _{CAS}	CAS low pulse width	20	10000	25	10000	30	10000	ns
t _{CSH}	CAS hold time after RAS low	80		100		120		ns
t _{RSH}	RAS hold time after CAS low	20		25		30		ns
t _{WCS}	Write setup time before CAS low (Note 22)	0		0		0		ns
t _{WCH}	Write hold time after CAS low	15		20		25		ns
t _{CWL}	CAS hold time after write low	20		25		30		ns
t _{RWL}	RAS hold time after write low	20		25		30		ns
t _{WP}	Write pulse width	15		20		25		ns
t _{DS}	Data setup time	0		0		0		ns
t _{DH}	Data hold time after CAS low	15		20		25		ns
t _{OEHD}	Delay time, OE high to data	15		20		25		ns
t _{h(WOE)}	OE hold time after write low	15		20		25		ns

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Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read write/read modify write cycle time (Note 21)	205		245		285		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	125	10000	155	10000	185	10000	ns
t _{CAS}	$\overline{\text{CAS}}$ low pulse width	65	10000	80	10000	95	10000	ns
t _{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	125		155		185		ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	65		80		95		ns
t _{RCS}	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWD}	Delay time, $\overline{\text{CAS}}$ low to write low (Note 22)	40		50		60		ns
t _{RWD}	Delay time, $\overline{\text{RAS}}$ low to write low (Note 22)	100		125		150		ns
t _{CWL}	$\overline{\text{CAS}}$ hold time after write low	20		25		30		ns
t _{RWL}	$\overline{\text{RAS}}$ hold time after write low	20		25		30		ns
t _{WP}	Write pulse width	15		20		25		ns
t _{DS}	Data setup time	0		0		0		ns
t _{DH}	Data hold time after write low	15		20		25		ns
t _{AWD}	Delay time, address to write low (Note 22)	60		75		90		ns
t _{h(OLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{CAS}}$ low	20		25		30		ns
t _{h(RLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{RAS}}$ low	80		100		120		ns
t _{DOEL}	Delay time, Data to $\overline{\text{OE}}$ low	0		0		0		ns
t _{OEHD}	Delay time, $\overline{\text{OE}}$ high to Data	15		20		25		ns
t _{h(WOE)}	$\overline{\text{OE}}$ hold time after write low	15		20		25		ns

Note 21: t_{RWC} is specified as t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_r.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS(min)} the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD(min)}, t_{RWD} ≥ t_{RWD(min)} and t_{AWD} ≥ t_{AWD(min)}, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t _{PO}	Read, Write cycle time	50		60		70		ns
t _{RWPC}	Read write/read modify write cycle time	100		115		135		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width for Read, write cycle	135	50000	160	50000	190	50000	ns
t _{CAS}	$\overline{\text{CAS}}$ low pulse width for read cycle	20	10000	25	10000	30	10000	ns
t _{CP}	$\overline{\text{CAS}}$ high pulse width (Note 23)	10	25	10	25	15	30	ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	20		25		30		ns

Note 23: t_{CP(max)} is specified as a reference point only. If t_{CP(max)} ≤ t_{CP}, access time is assumed by t_{CAC}.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44256A-8		M5M44256A-10		M5M44256A-12		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	10		10		10		ns
t _{CHR}	$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	15		20		25		ns
t _{RPC}	Precharge to $\overline{\text{CAS}}$ active time	0		0		0		ns

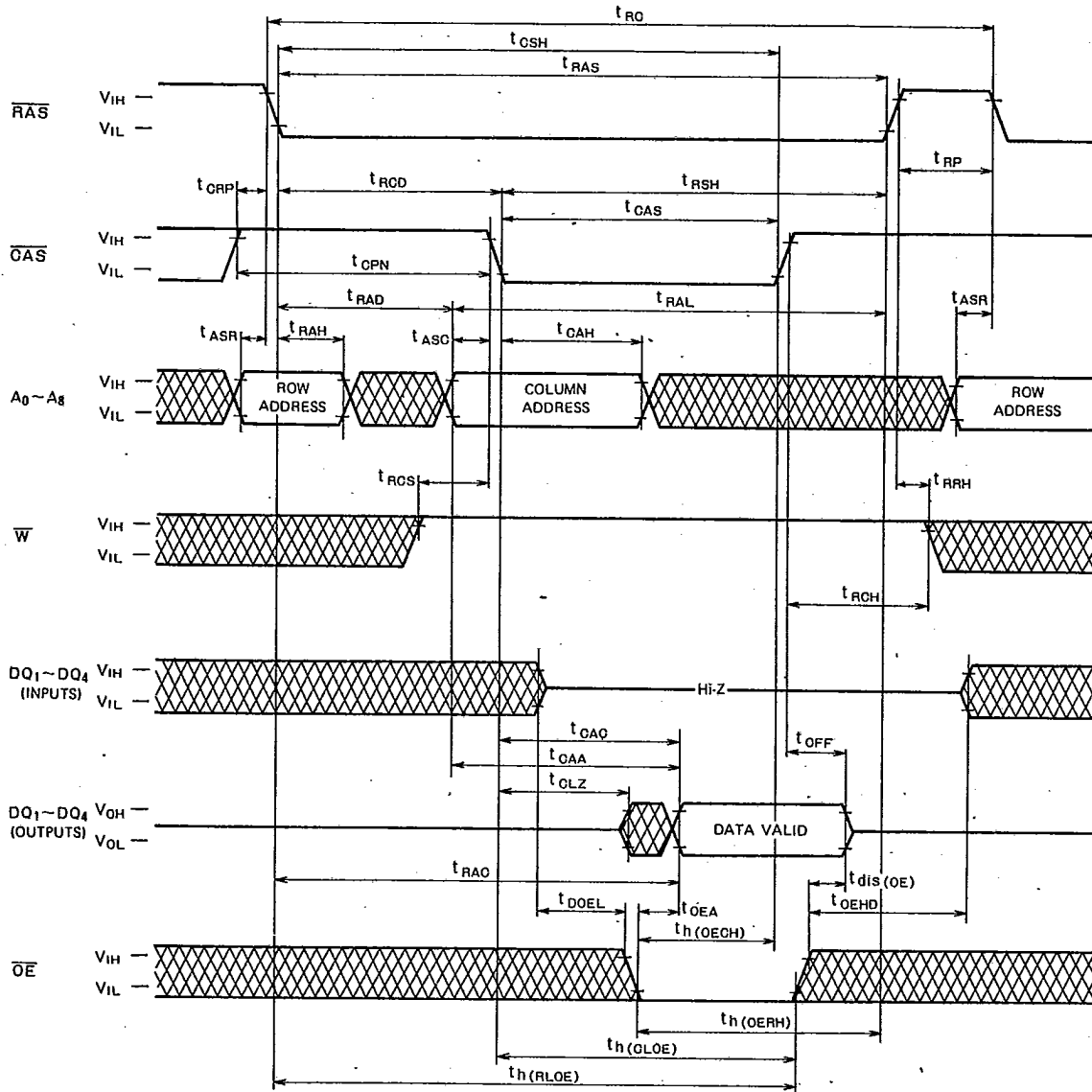
Note 24: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.


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Timing Diagrams (Note 25)

Read Cycle



Note 25  Indicates the don't care input.

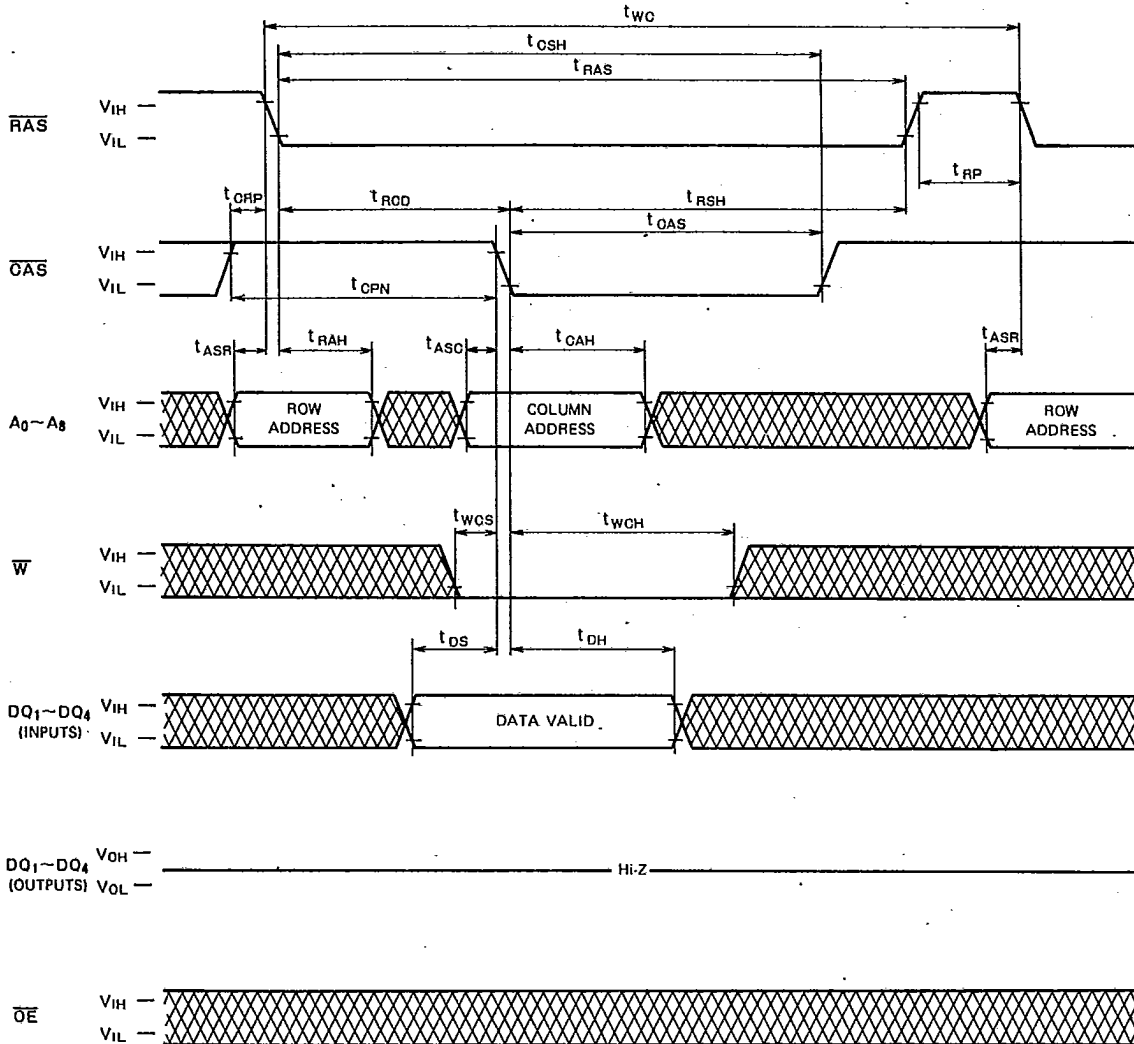
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Write Cycle (Early write)



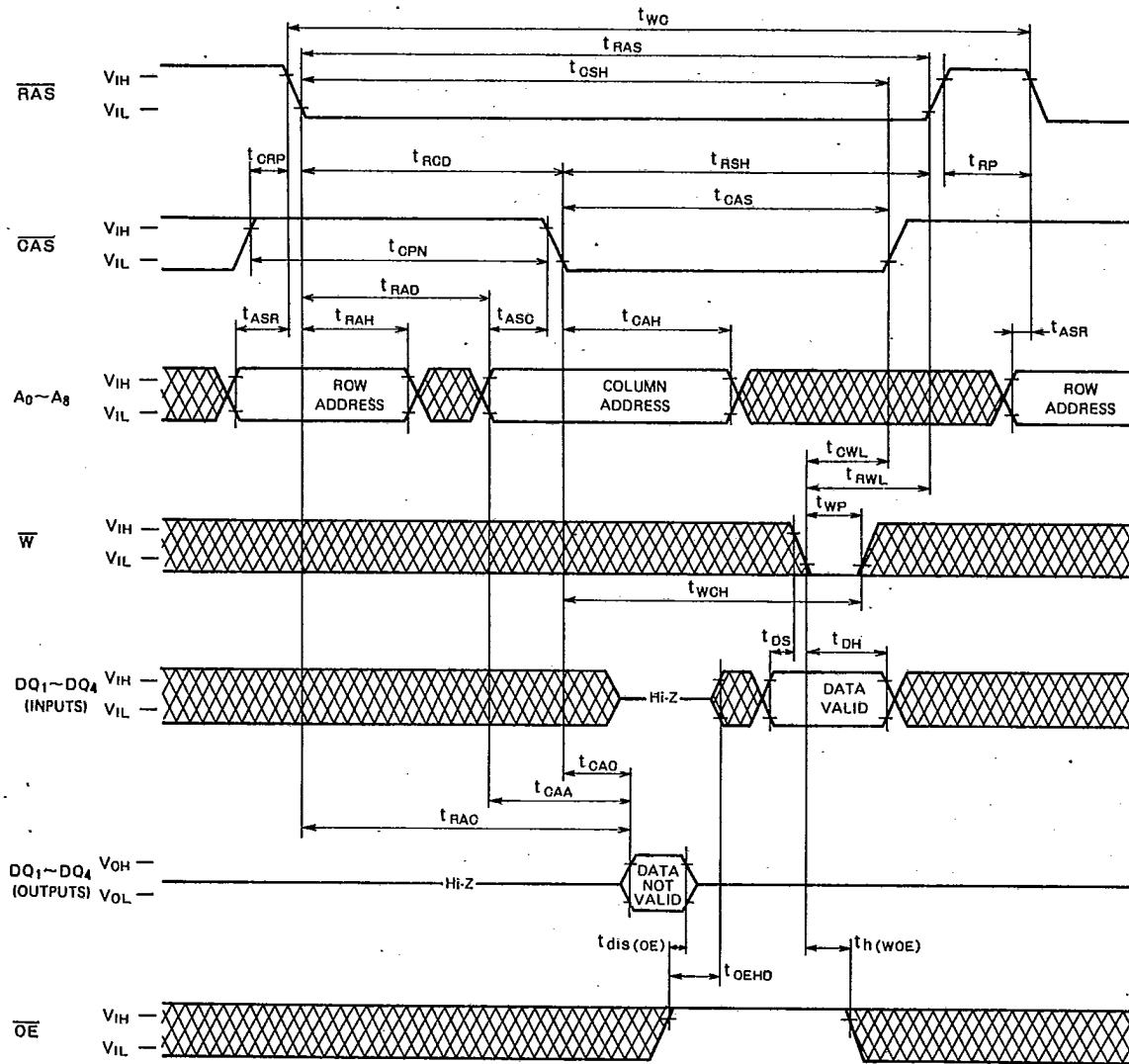
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Write Cycle (Delayed Write)



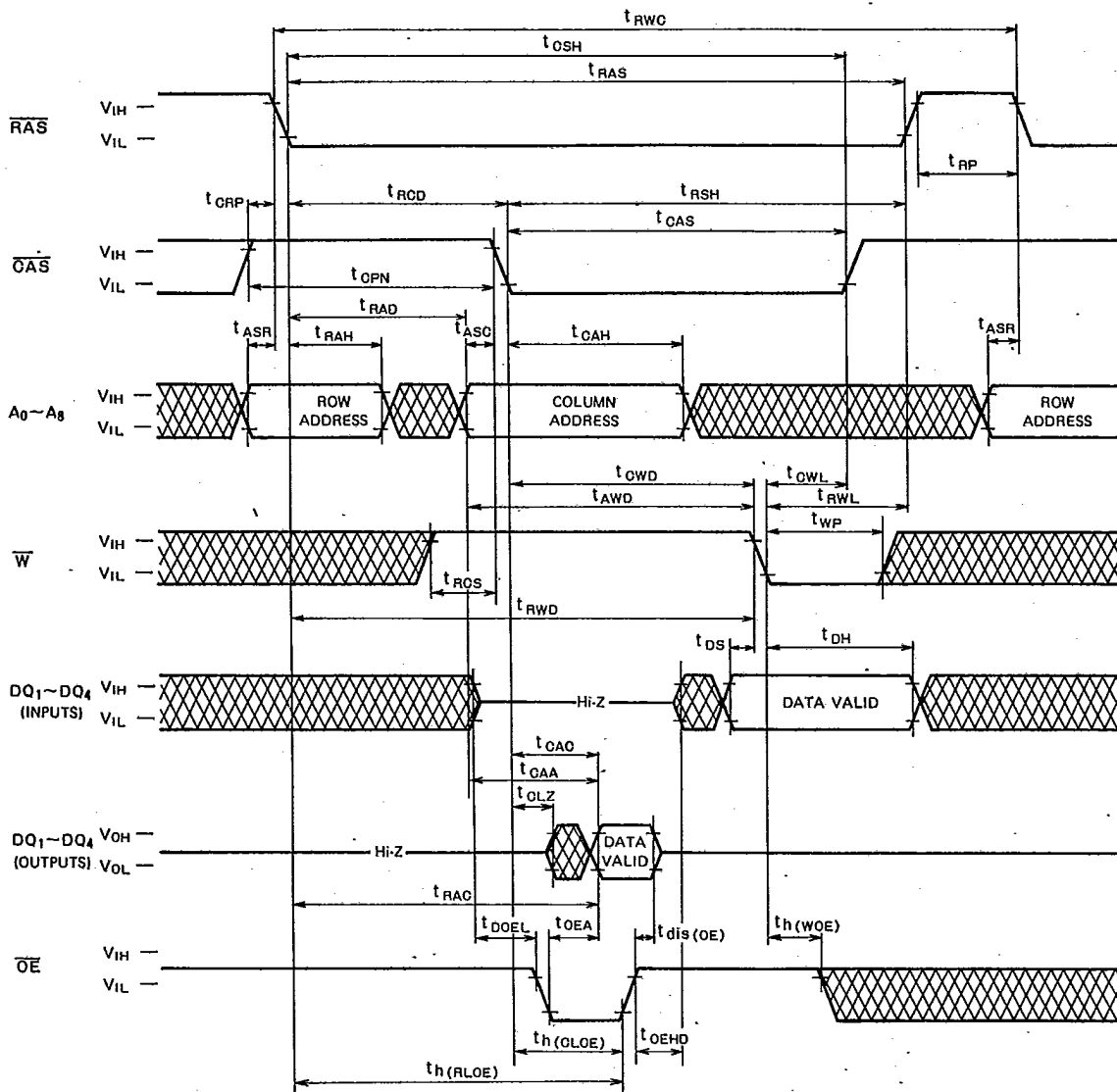
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Read-Write, Read-Modify-Write Cycle



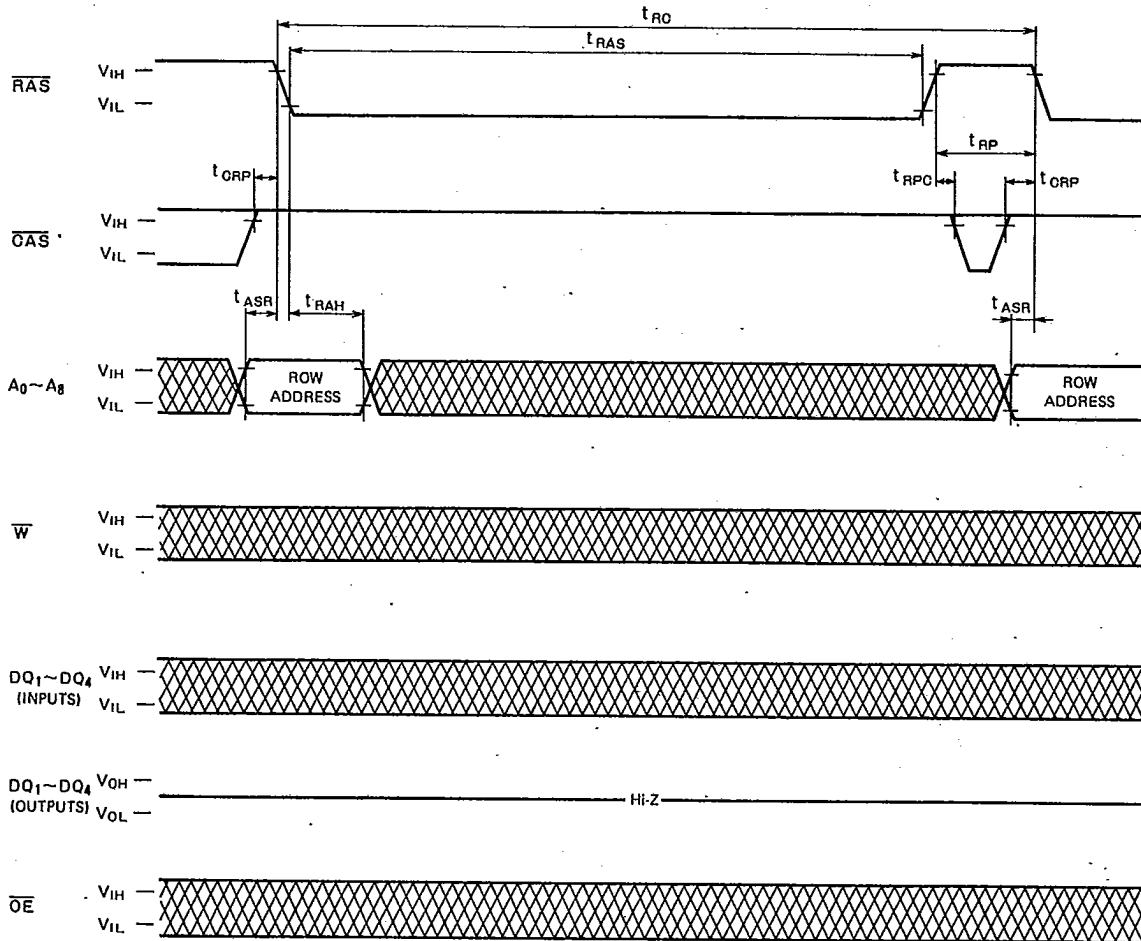
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RAS-only Refresh Cycle



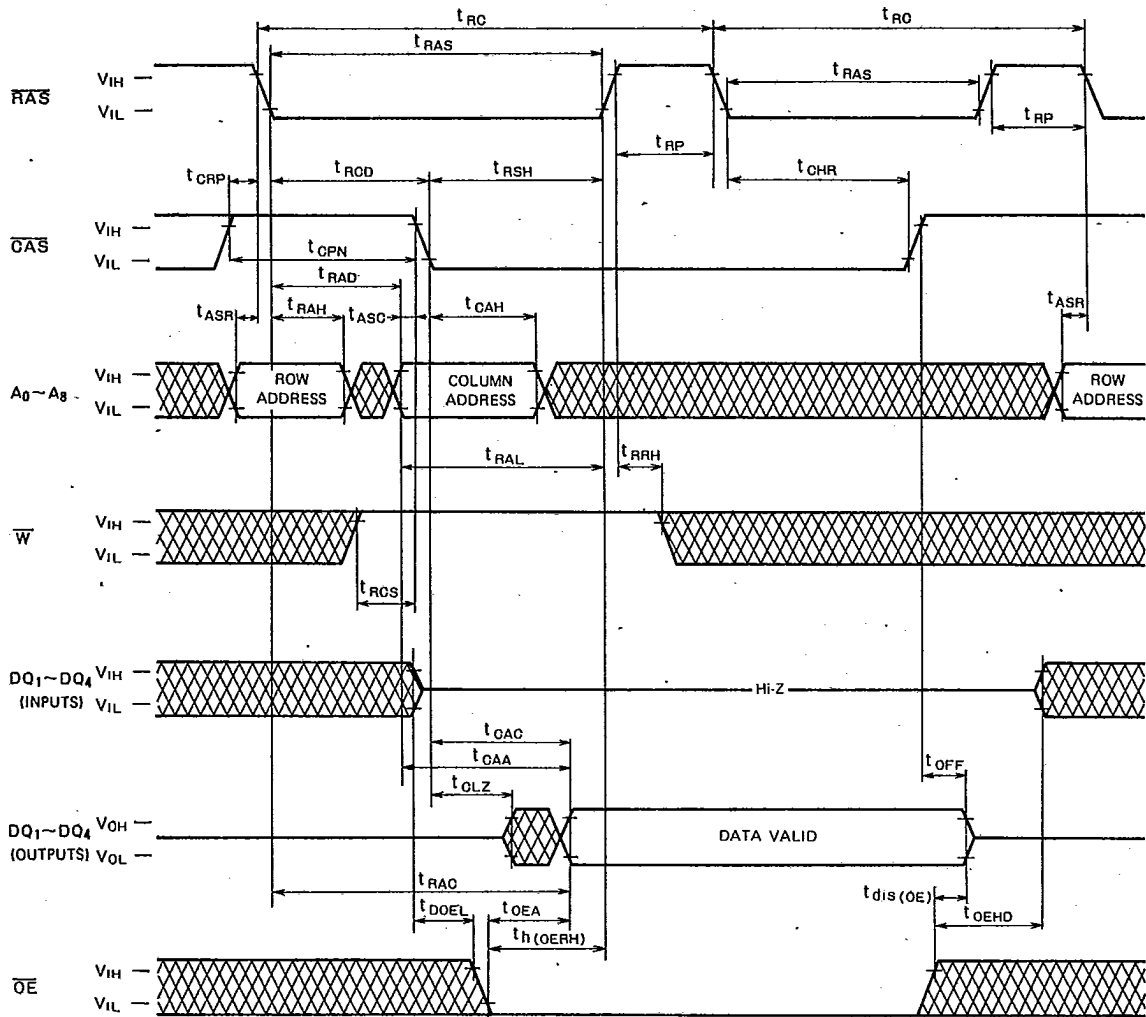
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FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Hidden Refresh Cycle



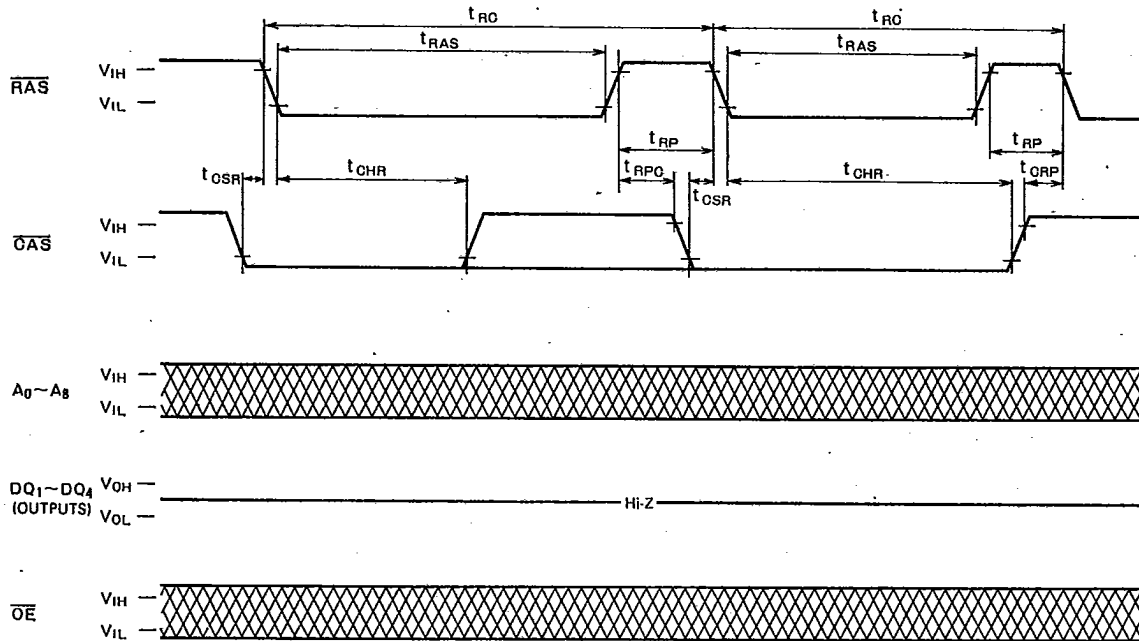
M5M44256AP, J, L-8, -10, -12

MITSUBISHI (MEMORY/ASIC)

T-45-23-17

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

CAS before RAS Refresh Cycle



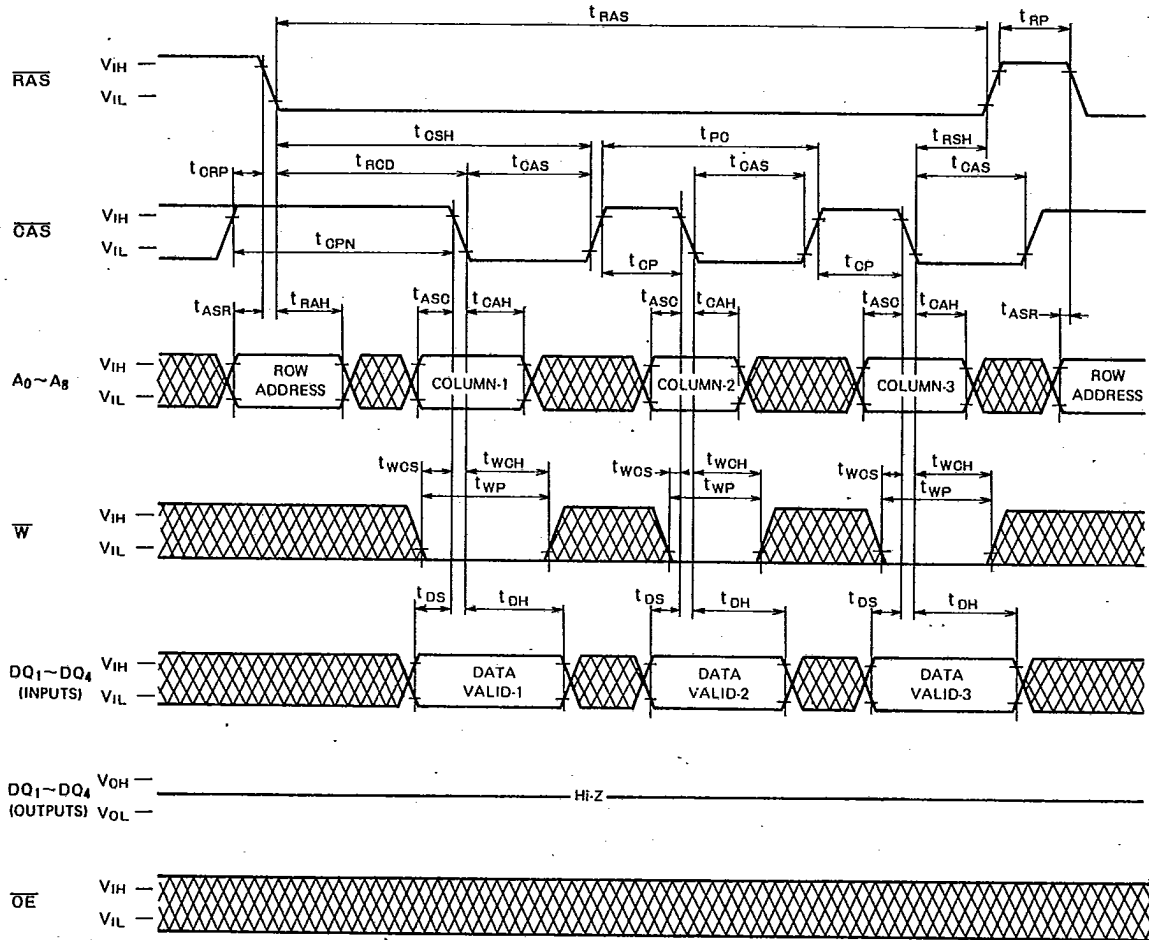
M5M44256AP, J, L-8, -10, -12

MITSUBISHI (MEMORY/ASIC)

T-45-23-17

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)



M5M44256AP, J, L-8, -10, -12

MITSUBISHI (MEMORY/ASIC)

T-45-23-17

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Fast Page Mode Read-Write, Read-Modify-Write Cycle

