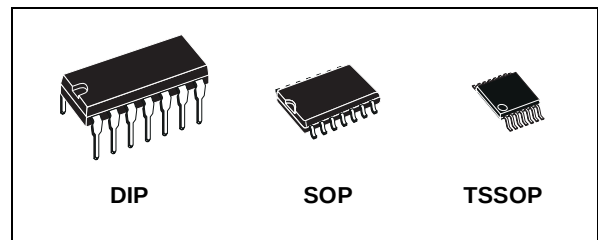


DUAL J-K FLIP FLOP WITH CLEAR

- HIGH SPEED :
 $f_{MAX} = 80\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = |I_{OL}| = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 107



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC107B1R	
SOP	M74HC107M1R	M74HC107RM13TR
TSSOP		M74HC107TTR

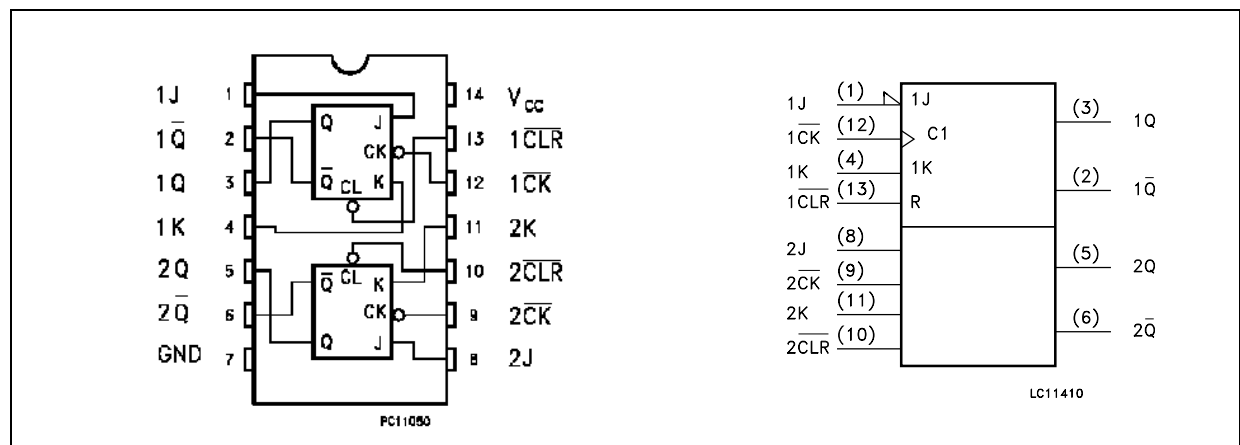
DESCRIPTION

The M74HC107 is an high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and

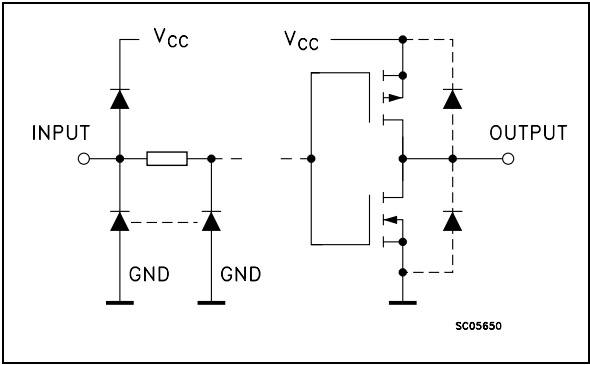
CLEAR input and Q and $\bar{Q}$ outputs. CLEAR is independent of the clock and accomplished by a logic low on the input.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

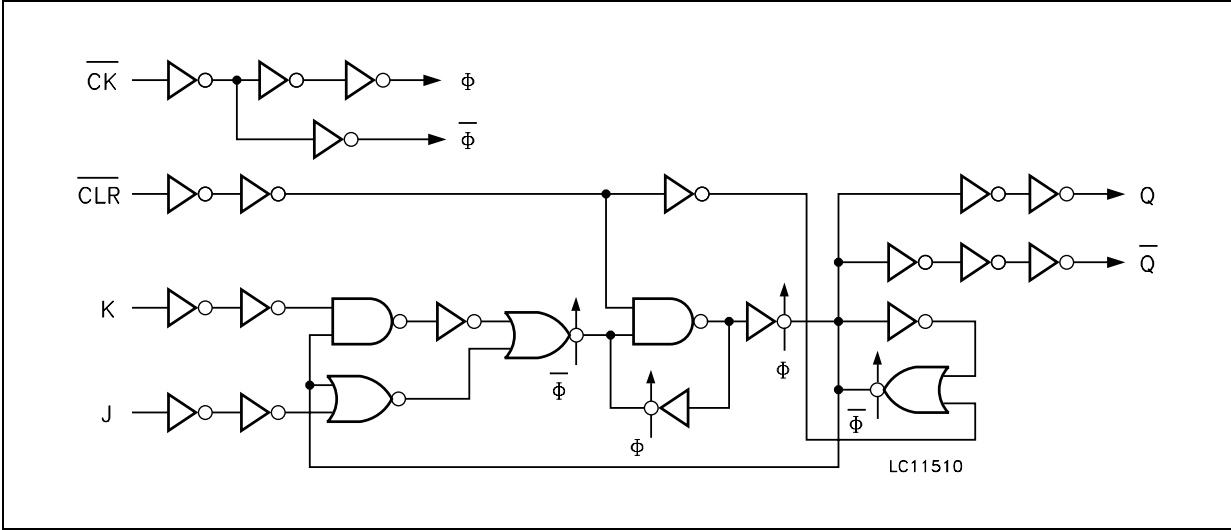
PIN No	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	Synchronous Inputs; Flip-Flop 1 And 2
2, 6	1Q̄, 2Q̄	Complement Flip-Flop Outputs
3, 5	1Q, 2Q	True Flip-Flop Outputs
12, 9	1CK, 2CK	Clock Input
13, 10	1CLR, 2CLR	Asynchronous Reset Inputs
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR̄	J	K	CK̄	Q	Q̄	
L	X	X	X	L	H	CLEAR
H	L	L	⌊	Q _n	Q̄ _n	NO CHANGE
H	L	H	⌊	L	H	----
H	H	L	⌊	H	L	----
H	H	H	⌊	Q̄ _n	Q _n	TOGGLE
H	X	X	⌋	Q _n	Q̄ _n	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V _{CC}	Supply Voltage		2 to 6	V
V _I	Input Voltage		0 to V _{CC}	V
V _O	Output Voltage		0 to V _{CC}	V
T _{op}	Operating Temperature		-55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0V	0 to 1000	ns
		V _{CC} = 4.5V	0 to 500	ns
		V _{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit		
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			2		20		40	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

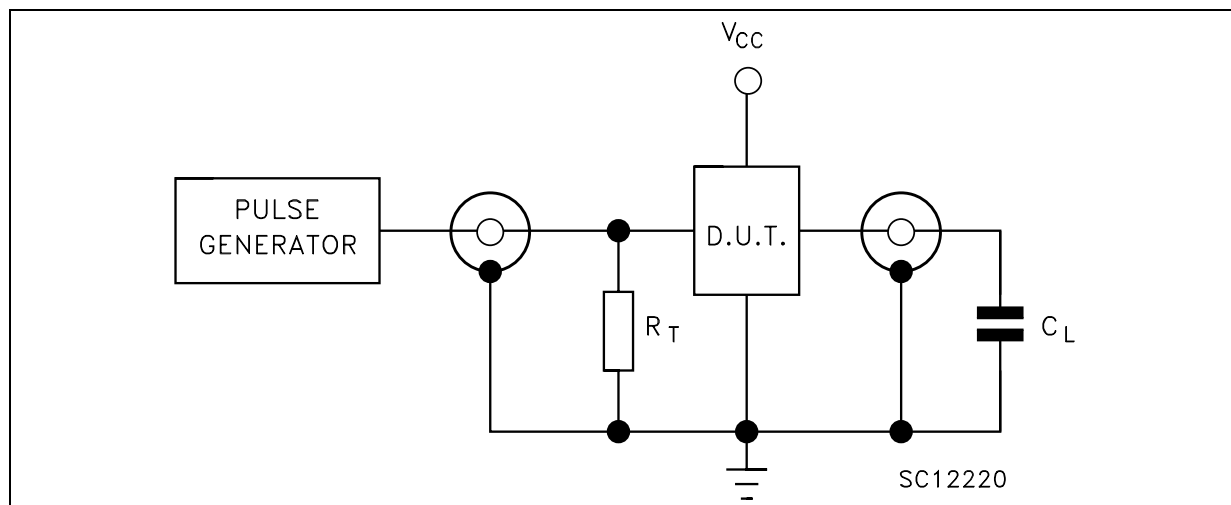
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay Time (CK - Q, Q)	2.0			48	125		155		190	ns
		4.5			14	25		31		38	
		6.0			12	21		26		32	
t _{PLH} t _{PHL}	Propagation Delay Time (CLR - Q, Q)	2.0			52	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
f _{MAX}	Maximum Clock Frequency	2.0		6.2	23		5.0		4.2		MHz
		4.5		31	70		25		21		
		6.0		37	80		30		25		
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t _{W(L)}	Minimum Pulse Width (CLR)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t _s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t _h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t _{REM}	Minimum Removal Time (CLR)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	

CAPACITIVE CHARACTERISTICS

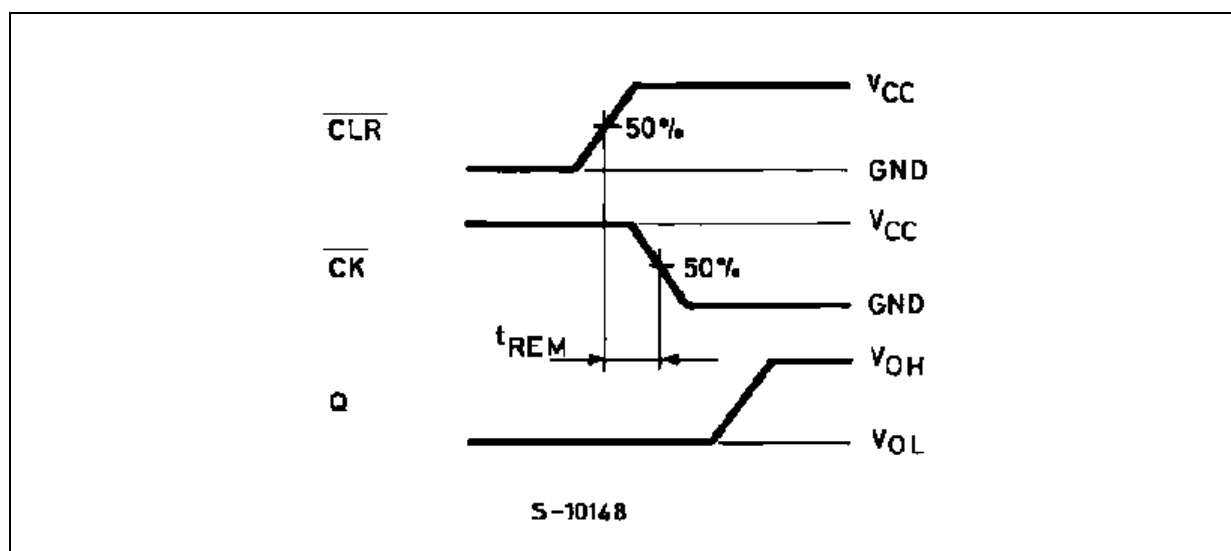
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			32						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

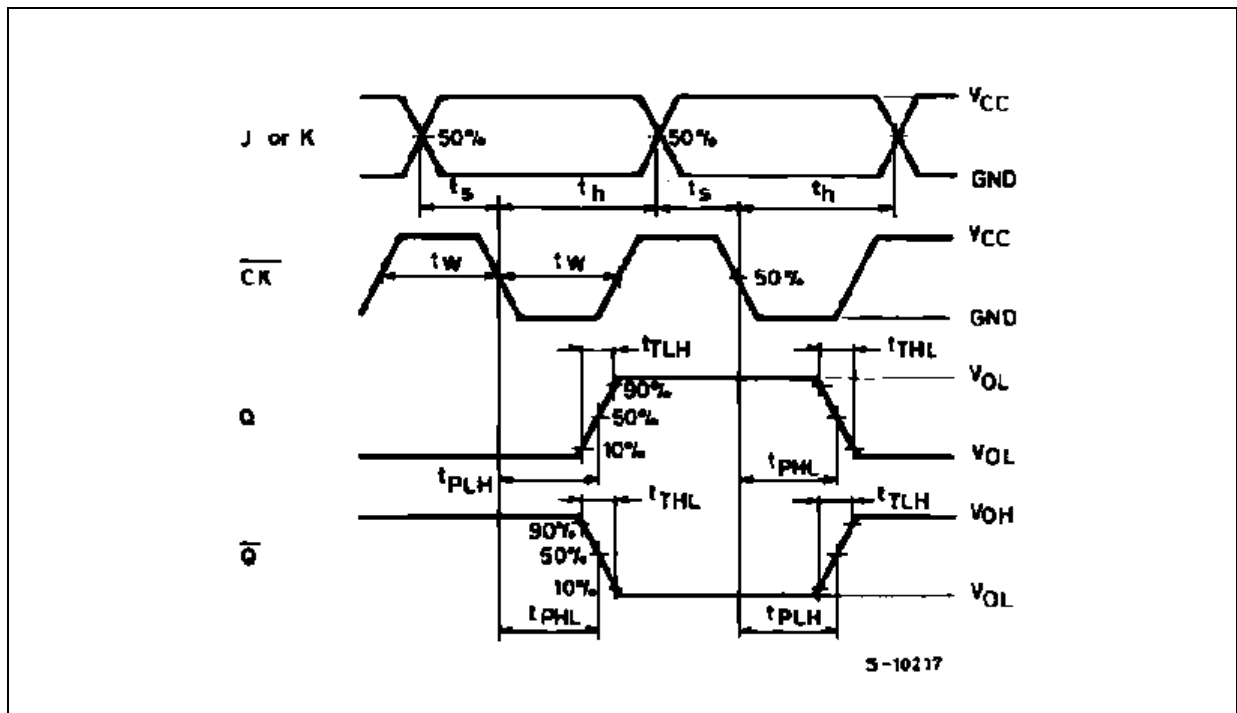
TEST CIRCUIT



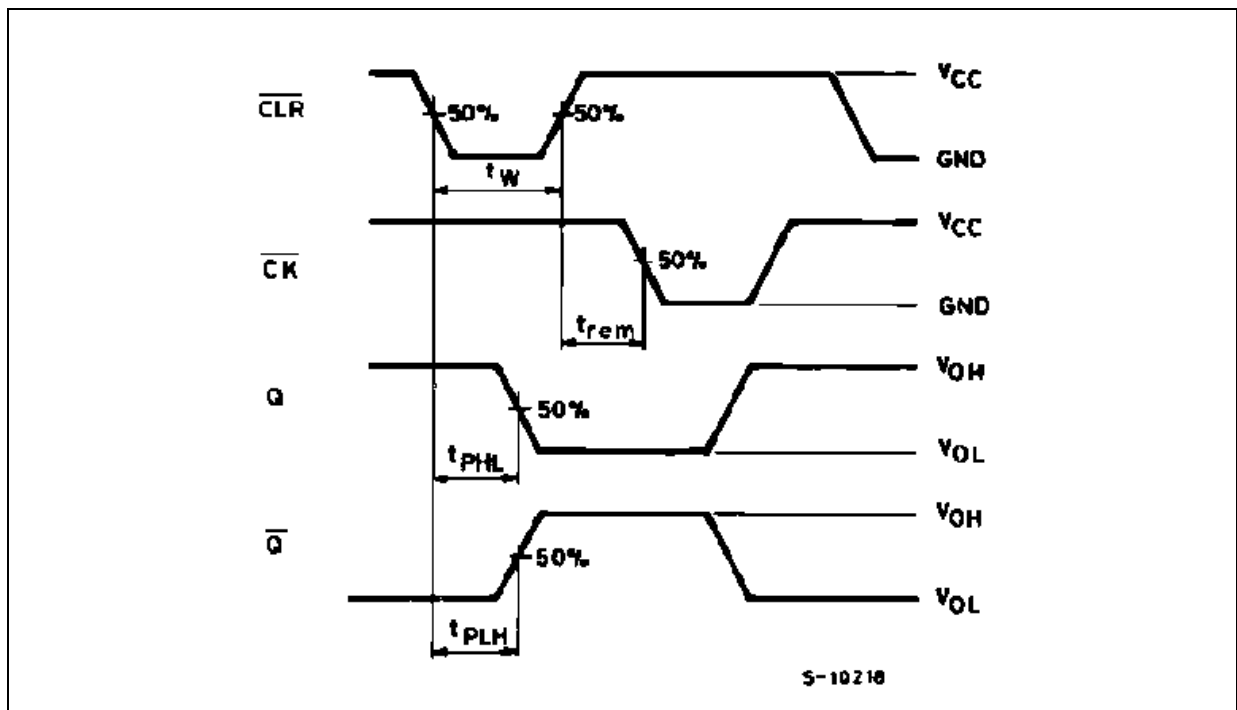
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: MINIMUM REMOVAL TIME ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH, SETUP AND HOLD TIME
(f=1MHz; 50% duty cycle)

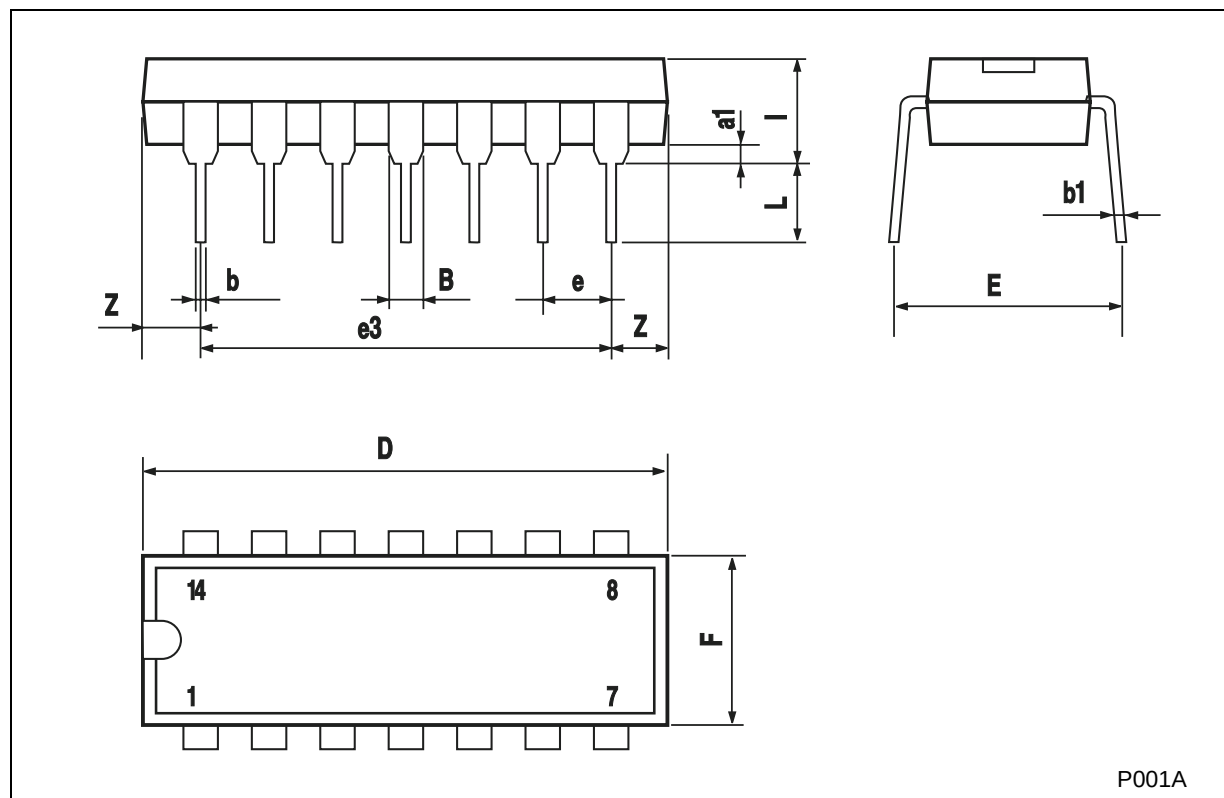


WAVEFORM 3 : MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



Plastic DIP-14 MECHANICAL DATA

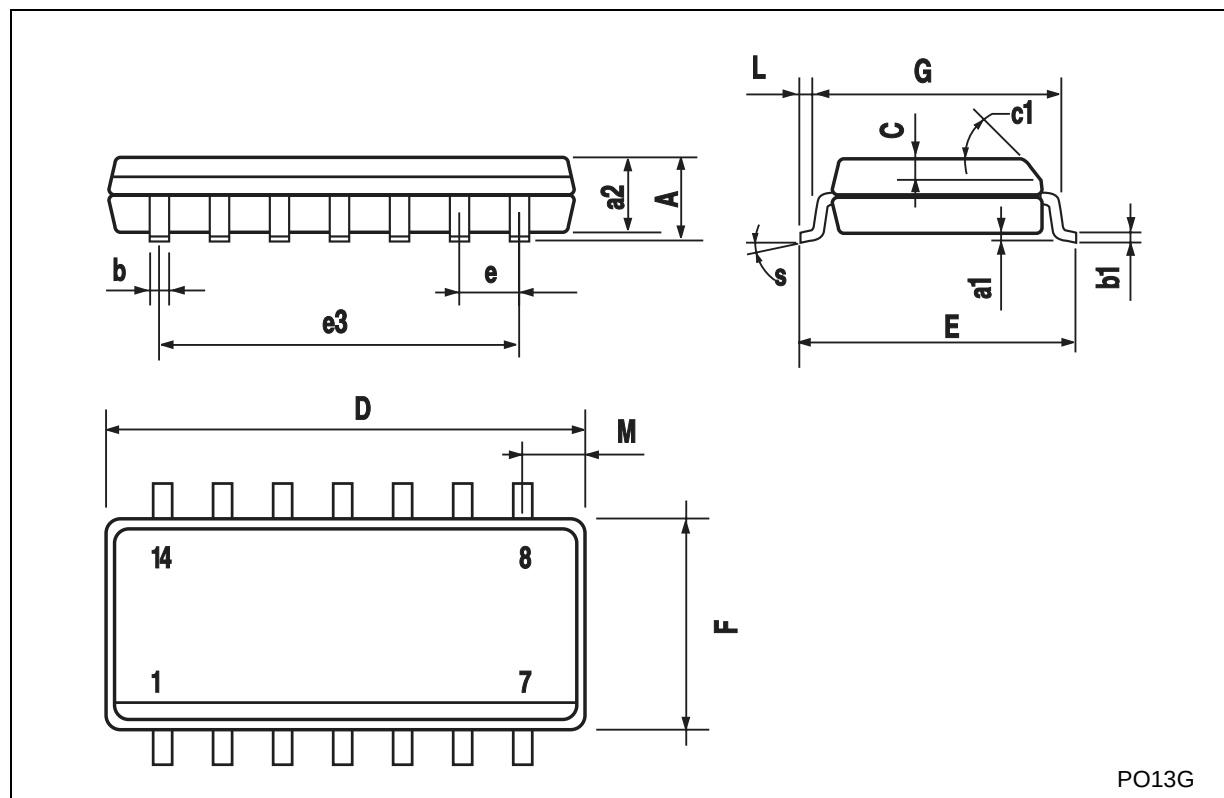
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

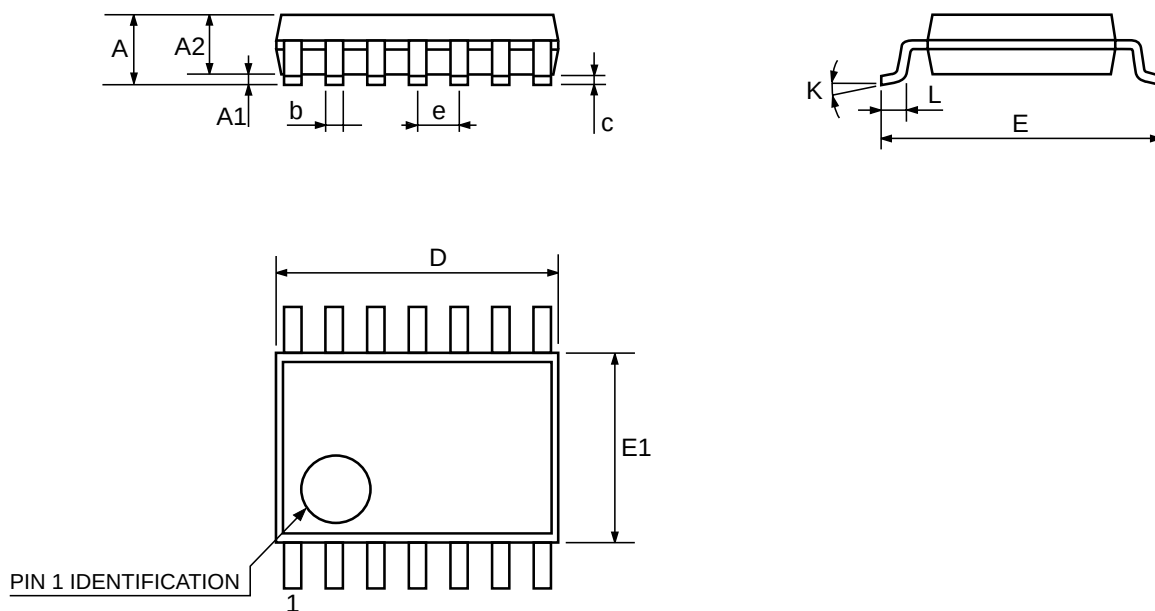
SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080337D

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

