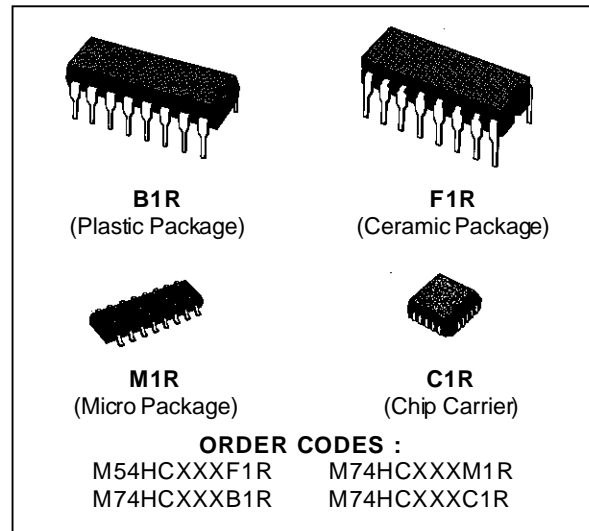


HEX BUS BUFFER (3-STATE) HC367 NON INVERTING, HC368 INVERTING

- HIGH SPEED
 $t_{PD} = 11 \text{ ns (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE WITH
 54/74LS367/368

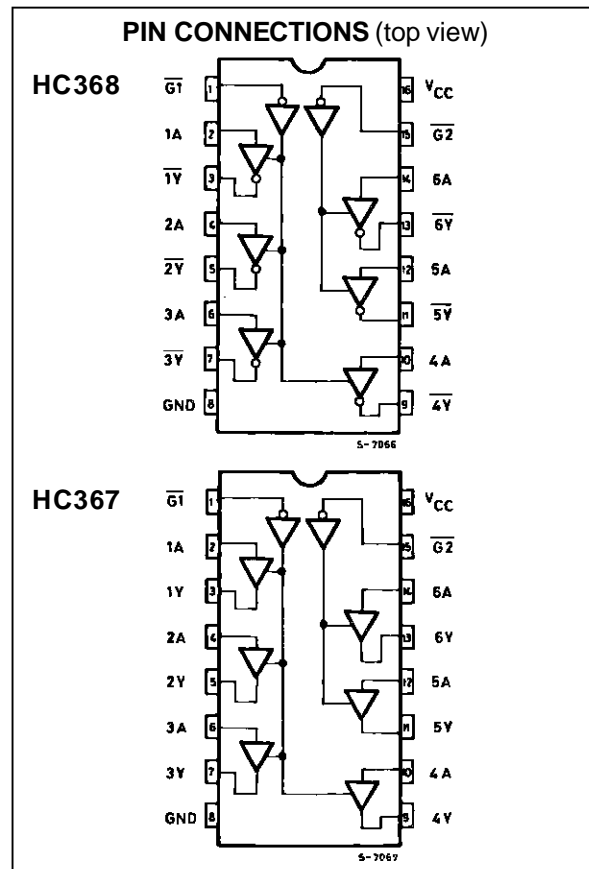


DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$); the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

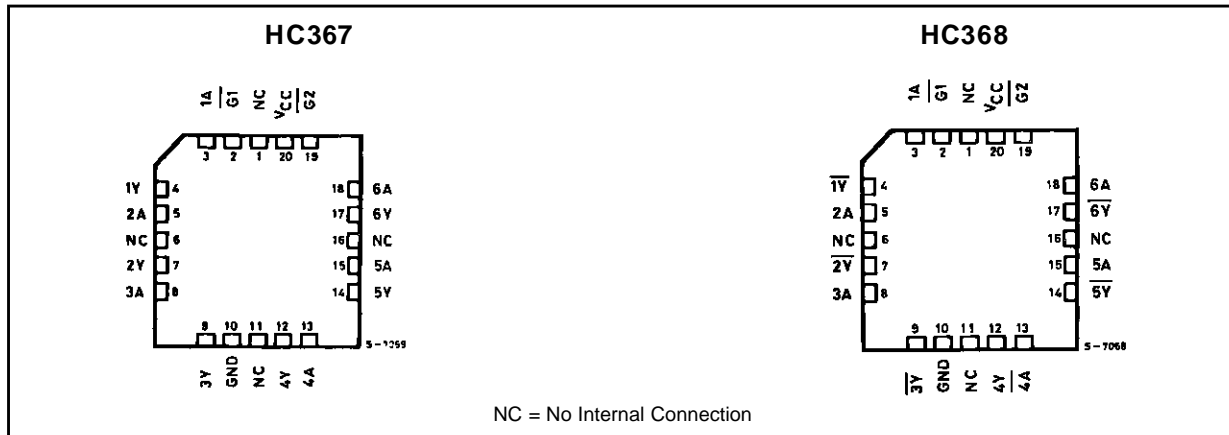


M54/M74HC367/368

INPUT AND OUTPUT EQUIVALENT CIRCUIT



CHIP CARRIER



TRUTH TABLE

INPUTS		OUTPUTS	
\overline{G}	A_n	Y_n (367)	\overline{Y}_n (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X = DONT CARE Z = HIGH IMPEDANCE

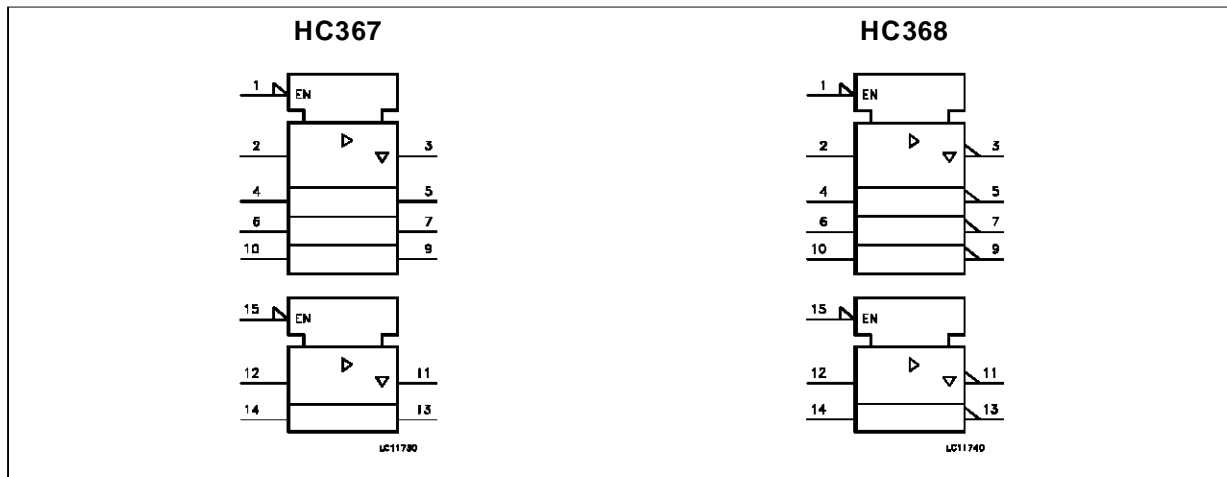
PIN DESCRIPTION (HC367)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}, \overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HC368)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}, \overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	$\overline{1Y}$ to $\overline{6Y}$	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ≙ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

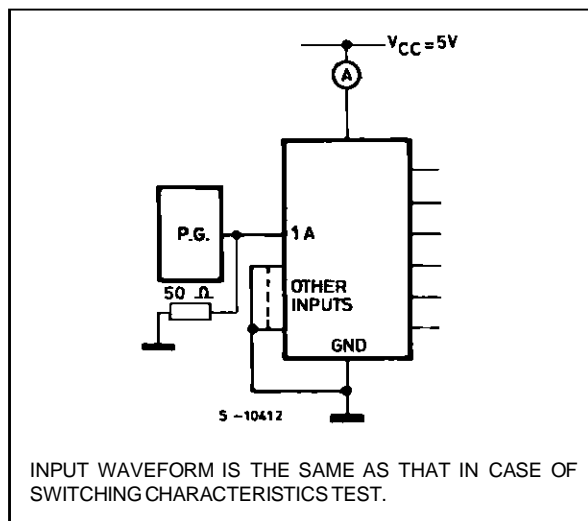
Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O = -6.0 mA	4.18	4.31		4.13		4.10		
		6.0			I _O = -7.8 mA	5.68	5.8		5.63			5.60
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		V	
		4.5				0.0	0.1		0.1			0.1
		6.0				0.0	0.1		0.1			0.1
		4.5		I _O = 6.0 mA		0.17	0.26		0.33			0.40
		6.0			I _O = 7.8 mA		0.18	0.26		0.33		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{OZ}	3 State Output Off State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.5		±5		±10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Test Conditions			Value						Unit	
		V_{CC} (V)	C_L (pF)		$T_A = 25 \text{ }^\circ\text{C}$ 54HC and 74HC			$-40 \text{ to } 85 \text{ }^\circ\text{C}$ 74HC		$-55 \text{ to } 125 \text{ }^\circ\text{C}$ 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			30	85		105		130	ns
		4.5				10	17		21		26	
		6.0				9	14		18		22	
		2.0	150			42	105		130		160	ns
		4.5				14	21		26		32	
		6.0				12	18		22		27	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	$R_L = 1 \text{ K}\Omega$		36	90		115		135	ns
		4.5				11	18		23		27	
		6.0				9	15		20		23	
		2.0	150	$R_L = 1 \text{ K}\Omega$		49	110		140		165	ns
		4.5				15	22		28		33	
		6.0				13	19		24		28	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	$R_L = 1 \text{ K}\Omega$		32	95		120		145	ns
		4.5				14	19		24		29	
		6.0				12	16		20		25	
C_{IN}	Input Capacitance					5	10		10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance					33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Channel)

TEST CIRCUIT I_{CC} (Opr.)



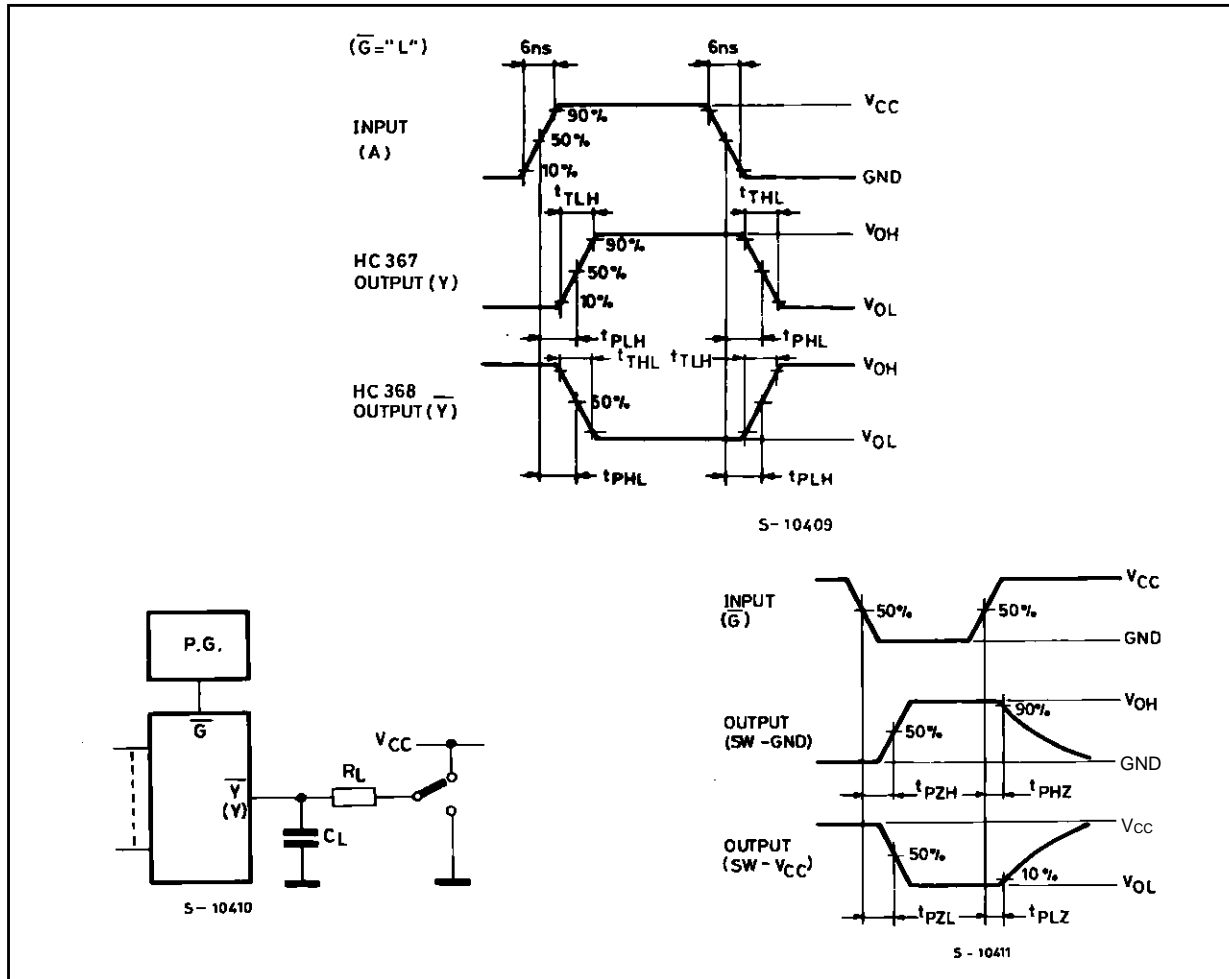
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of $I_{CC} (opr.)$ in the test circuit opposite.

$$C_{PD} = \frac{I_{CC} (opr)}{f_{IN} \times V_{CC}}$$

In determining the typical value of C_{PD} , a relatively high frequency of 1 MHz was applied to f_{IN} , in order to eliminate any error caused by the quiescent supply current.

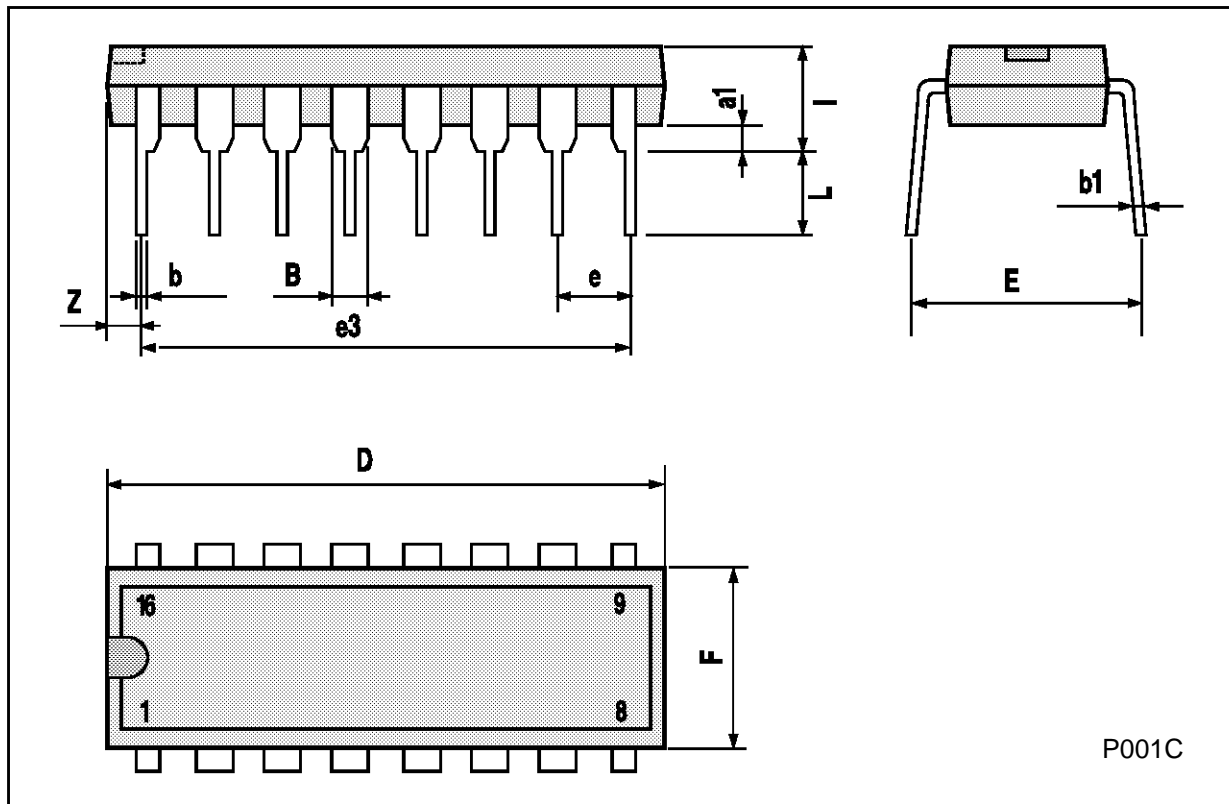
SWITCHING CHARACTERISTICS TEST WAVEFORM



Note : Such a logic level shall be applied to each input that the output voltage stays in the apposite side to the switch connection level, when the output is enable.

Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

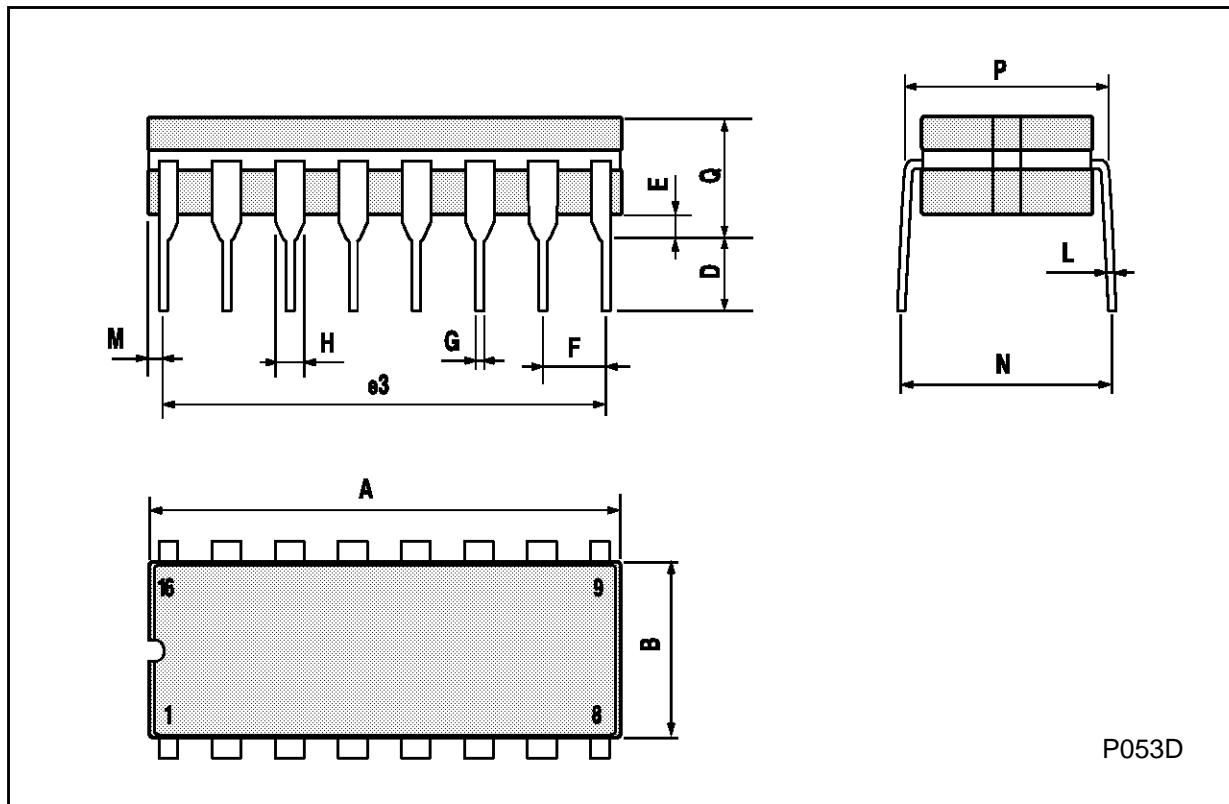


P001C

M54/M74HC367/368

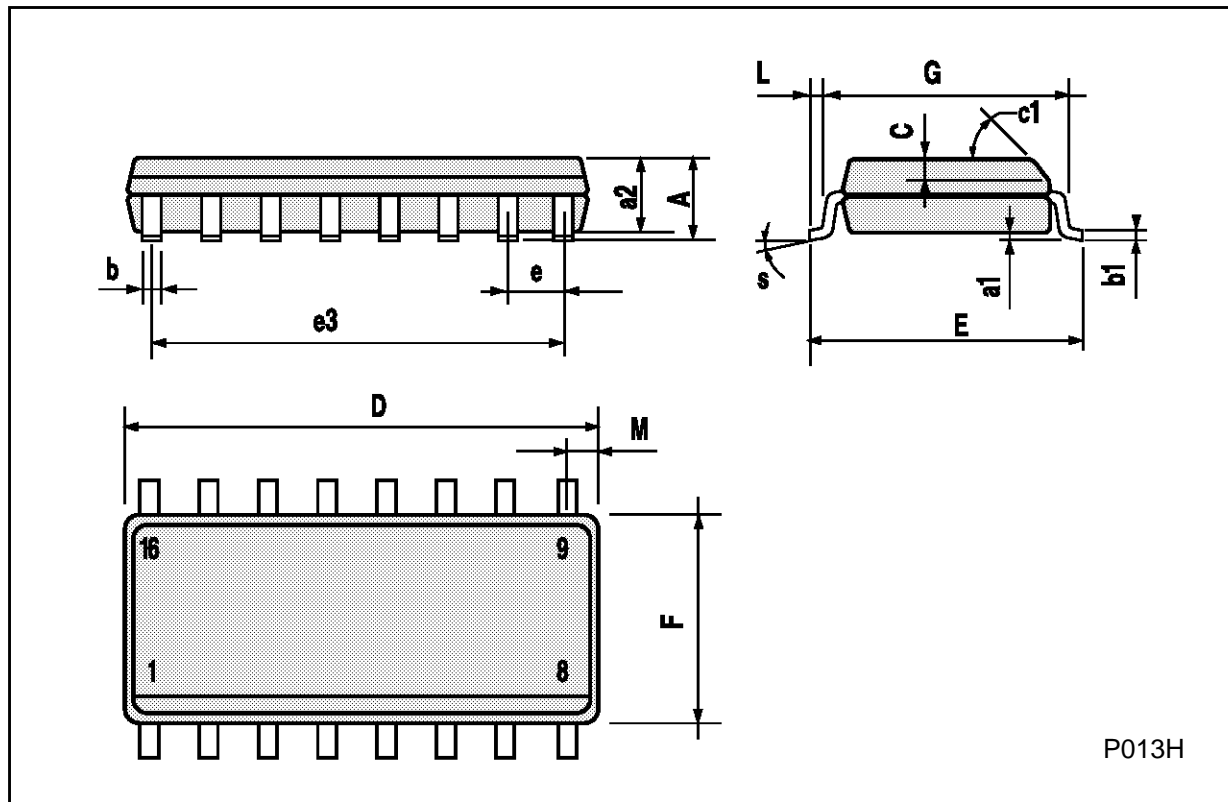
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

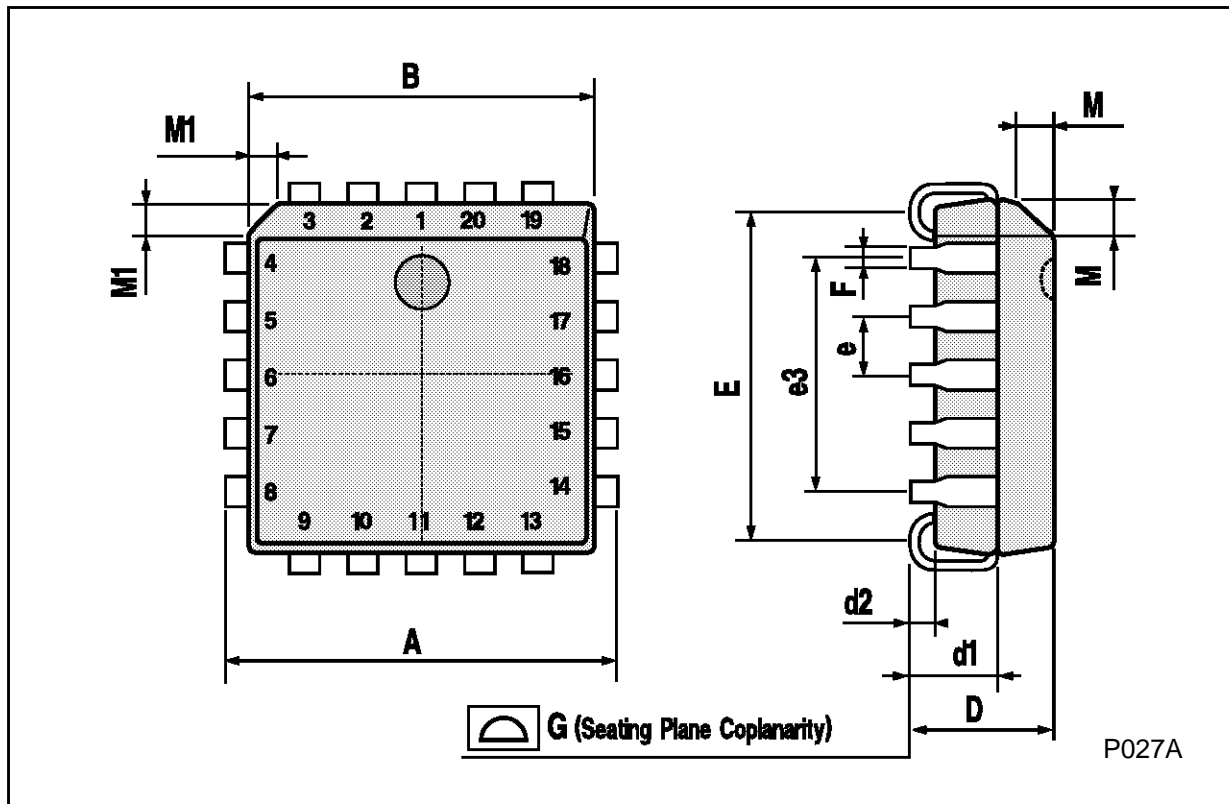
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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