

F-46-09-05



MC14094B

**8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS**

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q<sub>S</sub> output data is for use in high-speed cascaded systems. The Q<sub>S</sub> output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

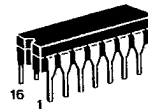
Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

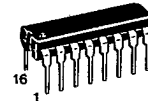
**CMOS MSI**

(LOW-POWER COMPLEMENTARY MOS)

**8-STAGE SHIFT/STORE REGISTER**



L SUFFIX CERAMIC PACKAGE CASE 620



P SUFFIX PLASTIC PACKAGE CASE 648

**ORDERING INFORMATION**

A Series: -55°C to +125°C  
MC14XXXBAL (Ceramic Package Only)

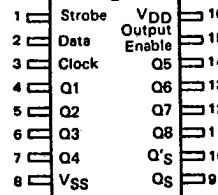
C Series: -40°C to +85°C  
MC14XXXBCP (Plastic Package)  
MC14XXXBCL (Ceramic Package)

**MAXIMUM RATINGS\*** (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.  
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C  
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

**PIN ASSIGNMENT**



Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q <sub>1</sub>	Q <sub>N</sub>	Q <sub>S</sub> *	Q' <sub>S</sub>
✓	0	X	X	Z	Z	Q <sub>7</sub>	No Chg.
✓	0	X	X	Z	Z	No Chg.	Q <sub>7</sub>
✓	1	0	X	No Chg.	No Chg.	Q <sub>7</sub>	No Chg.
✓	1	1	0	0	Q <sub>N</sub> -1	Q <sub>7</sub>	No Chg.
✓	1	1	1	1	Q <sub>N</sub> -1	Q <sub>7</sub>	No Chg.
✓	1	1	1	No Chg.	No Chg.	No Chg.	Q <sub>7</sub>

Z = High Impedance  
X = Don't Care  
\*At the positive clock edge, information in the 7th shift register stage is transferred to Q<sub>B</sub> and Q<sub>S</sub>.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

MC14094B

T-46-09-05

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> V <sub>dC</sub>	T <sub>low</sub> *		25°C			T <sub>high</sub> *		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V <sub>in</sub> =V <sub>DD</sub> or 0  V <sub>in</sub> =0 or V <sub>DD</sub>	VOL	5.0	—	0.05	—	0	0.05	—	0.05	V <sub>dC</sub>
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	V <sub>dC</sub>
10		9.95	—	9.95	10	—	9.95	—		
15		14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 V <sub>dC</sub> ) (V <sub>O</sub> = 9.0 or 1.0 V <sub>dC</sub> ) (V <sub>O</sub> = 13.5 or 1.5 V <sub>dC</sub> )  (V <sub>O</sub> = 0.5 or 4.5 V <sub>dC</sub> ) (V <sub>O</sub> = 1.0 or 9.0 V <sub>dC</sub> ) (V <sub>O</sub> = 1.5 or 13.5 V <sub>dC</sub> )	VIL	5.0	—	1.5	—	2.25	1.5	—	1.5	V <sub>dC</sub>
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	VIH	5.0	3.5	—	3.5	2.75	—	3.5	—	V <sub>dC</sub>
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current (AL Device) (V <sub>OH</sub> = 2.5 V <sub>dC</sub> ) (V <sub>OH</sub> = 4.6 V <sub>dC</sub> ) (V <sub>OH</sub> = 9.5 V <sub>dC</sub> ) (V <sub>OH</sub> = 13.5 V <sub>dC</sub> )  (V <sub>OL</sub> = 0.4 V <sub>dC</sub> ) (V <sub>OL</sub> = 0.5 V <sub>dC</sub> ) (V <sub>OL</sub> = 1.5 V <sub>dC</sub> )	IOH	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA <sub>dC</sub>
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	IOL	5.0	0.64	—	0.51	0.88	—	0.36	—	mA <sub>dC</sub>
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device) (V <sub>OH</sub> = 2.5 V <sub>dC</sub> ) (V <sub>OH</sub> = 4.6 V <sub>dC</sub> ) (V <sub>OH</sub> = 9.5 V <sub>dC</sub> ) (V <sub>OH</sub> = 13.5 V <sub>dC</sub> )  (V <sub>OL</sub> = 0.4 V <sub>dC</sub> ) (V <sub>OL</sub> = 0.5 V <sub>dC</sub> ) (V <sub>OL</sub> = 1.5 V <sub>dC</sub> )	IOH	5.0	-2.5	—	-2.1	-4.2	—	-1.7	—	mA <sub>dC</sub>
		10	-0.52	—	-0.44	-0.88	—	-0.36	—	
		15	-3.6	—	-3.0	-8.8	—	-2.4	—	
	IOL	5.0	0.52	—	0.44	0.88	—	0.36	—	mA <sub>dC</sub>
		10	1.3	—	1.1	2.25	—	0.9	—	
		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA <sub>dC</sub>
Input Current (CL/CP Device)	I <sub>in</sub>	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA <sub>dC</sub>
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μA <sub>dC</sub>
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current (CL/CP Device) (Per Package)	I <sub>DD</sub>	5.0	—	20	—	0.005	20	—	150	μA <sub>dC</sub>
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (4.1 μA/kHz) f + I <sub>DD</sub>							μA <sub>dC</sub>
		10	I <sub>T</sub> = (14 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (140 μA/kHz) f + I <sub>DD</sub>							
3-State Output Leakage Current (AL Device)	I <sub>TL</sub>	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μA
3-State Output Leakage Current (CL/CP Device)	I <sub>TL</sub>	15	—	±1.0	—	—	±1.0	—	±7.5	μA

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.  
T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{ik}$$

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

\*\*The formulas given are for the typical characteristics only at 25°C.



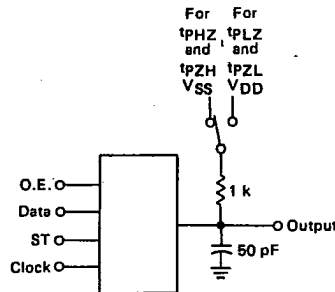
SWITCHING CHARACTERISTICS\* (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit		
Output Rise and Fall Time t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.6 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.4 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	—	100	200	ns		
		10	—	50	100			
		15	—	40	80			
Propagation Delay Time Clock to Serial out QS t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 305 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 107 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 82 ns Clock to Serial out Q'S t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 350 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 149 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 62 ns Clock to Parallel out t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 375 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 177 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 122 ns Strobe to Parallel out t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 245 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 127 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 87 ns Output Enable to Output t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.90 ns/pF) C <sub>L</sub> + 95 ns t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.36 ns/pF) C <sub>L</sub> + 57 ns t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.26 ns/pF) C <sub>L</sub> + 42 ns t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.90 ns/pF) C <sub>L</sub> + 180 ns t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.36 ns/pF) C <sub>L</sub> + 77 ns t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.26 ns/pF) C <sub>L</sub> + 57 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	—	350	600	ns		
		10	—	125	250			
		15	—	95	190			
		5.0	—	230	460			
		10	—	110	220			
		15	—	75	150			
		5.0	—	420	840			
		10	—	195	390			
		15	—	135	270			
		5.0	—	290	580			
		10	—	145	290			
		15	—	100	200			
		t <sub>PHZ</sub> , t <sub>PZL</sub>	5.0	—	140		280	ns
		10	—	75	150			
		15	—	55	110			
t <sub>PLZ</sub> , t <sub>PZH</sub>	5.0	—	225	450	ns			
10	—	95	190					
15	—	70	140					
Setup Time Data in to Clock	t <sub>su</sub>	5.0	125	60	—	ns		
		10	65	30	—			
		15	35	20	—			
Hold Time Clock to Data	t <sub>h</sub>	5.0	0	-40	—	ns		
		10	20	-10	—			
		15	20	0	—			
Clock Pulse Width, High	t <sub>WH</sub>	5.0	200	100	—	ns		
		10	100	50	—			
		15	83	40	—			
Clock Rise and Fall Time	t <sub>r</sub> (cl) t <sub>f</sub> (cl)	5	—	—	15	μs		
		10	—	—	5.0			
		15	—	—	4.0			
Clock Pulse Frequency	f <sub>cl</sub>	5.0	—	2.5	1.25	MHz		
		10	—	5.0	2.5			
		15	—	6.0	3.0			
Strobe Pulse Width	t <sub>WL</sub>	5.0	200	100	—	ns		
		10	80	40	—			
		15	70	35	—			

\*The formulae given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3-STATE TEST CIRCUIT



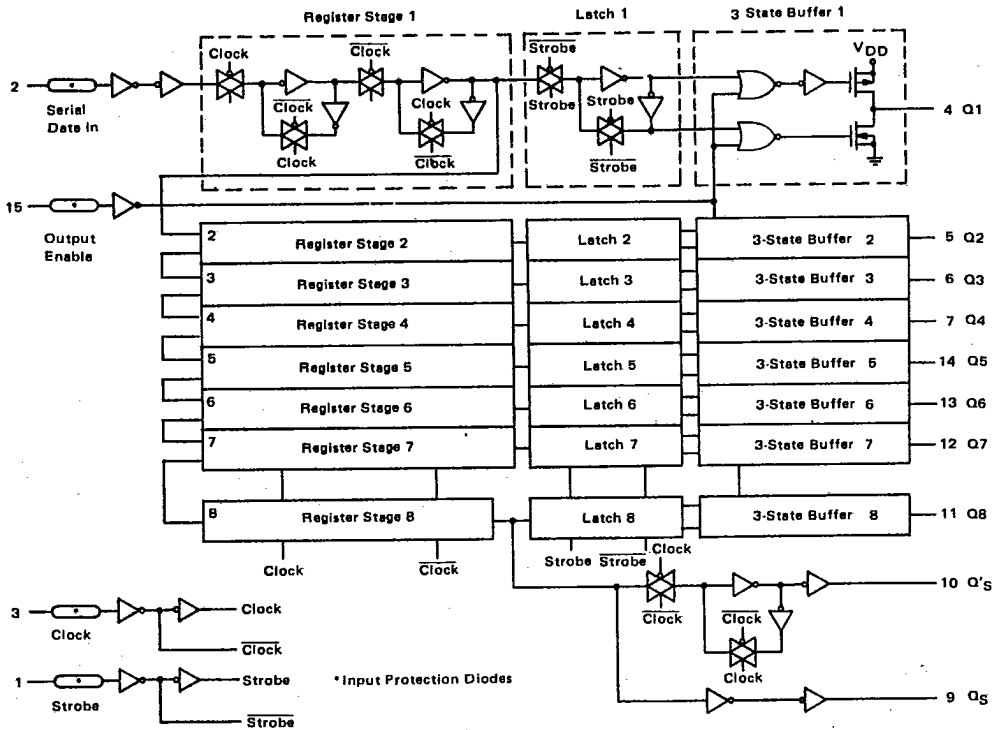
6367252 MOTOROLA SC (LOGIC)

98D 79593 D

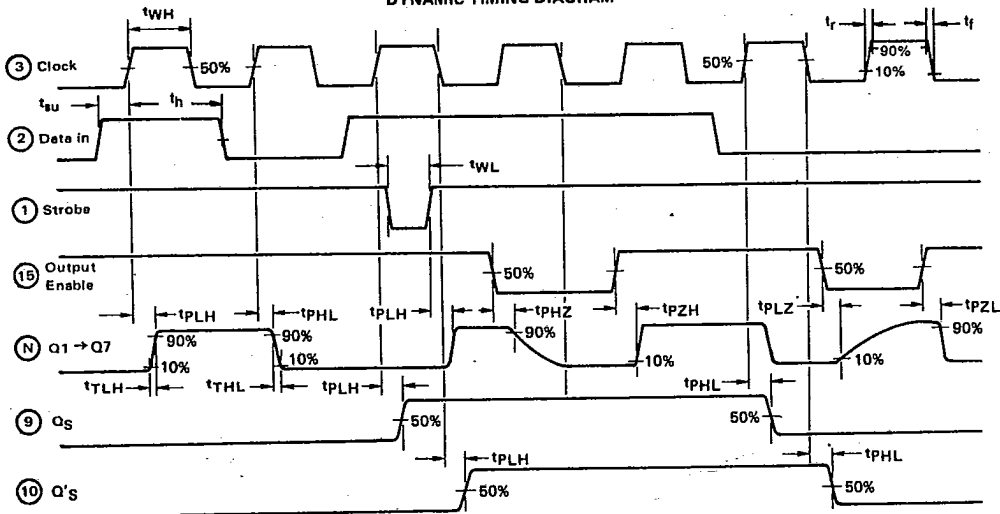
MC14094B

T-46-09-05

BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM



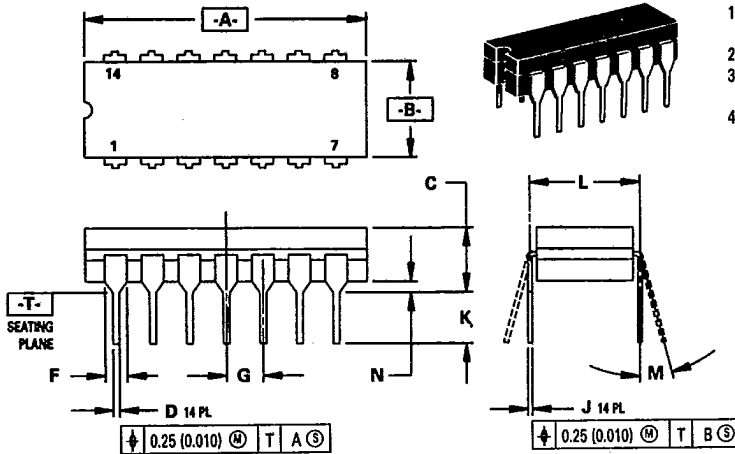
# PACKAGE DIMENSIONS

T-90-20

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BD.

## 14-PIN PACKAGE

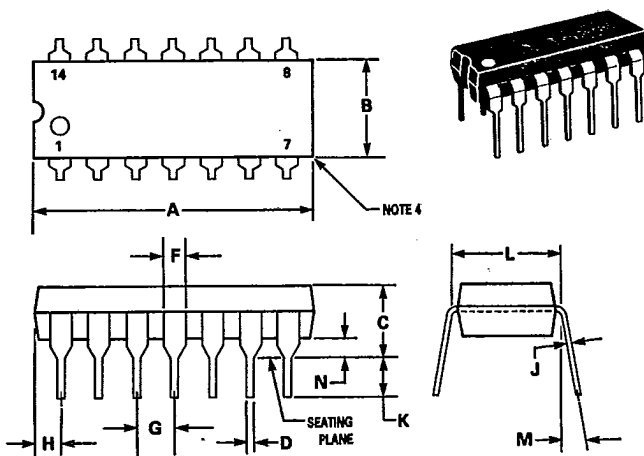
### CERAMIC PACKAGE CASE 632-08



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

### PLASTIC PACKAGE CASE 646-06



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

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0563

E-12

9-2

PACKAGE DIMENSIONS (Continued)

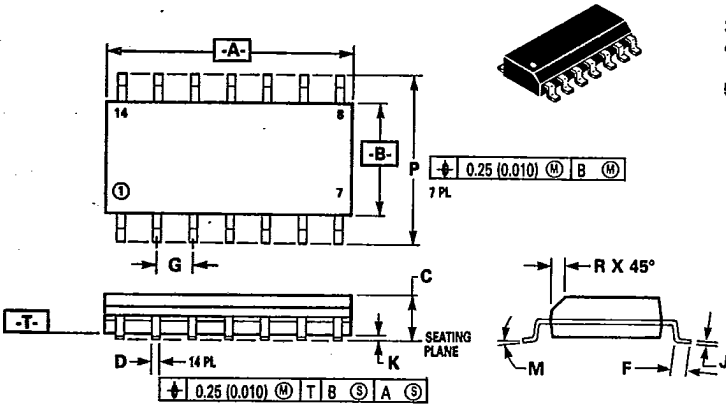
14-PIN PACKAGE

SOIC PACKAGE  
CASE 751A-02  
D SUFFIX

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

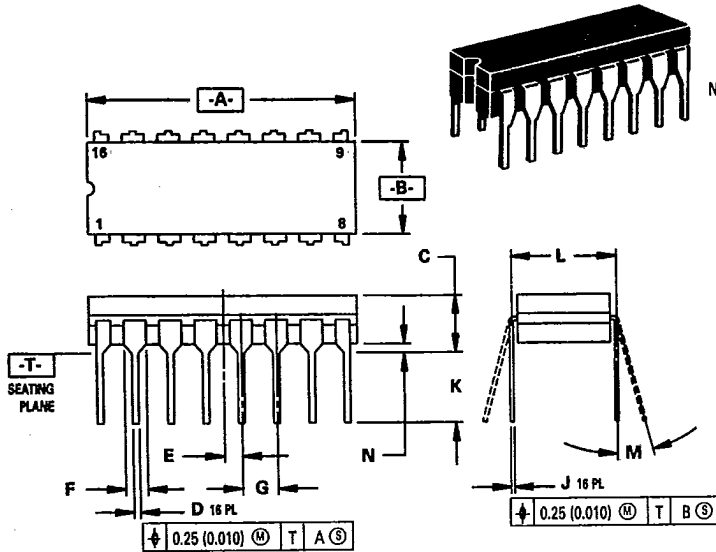
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

CERAMIC PACKAGE  
CASE 620-09

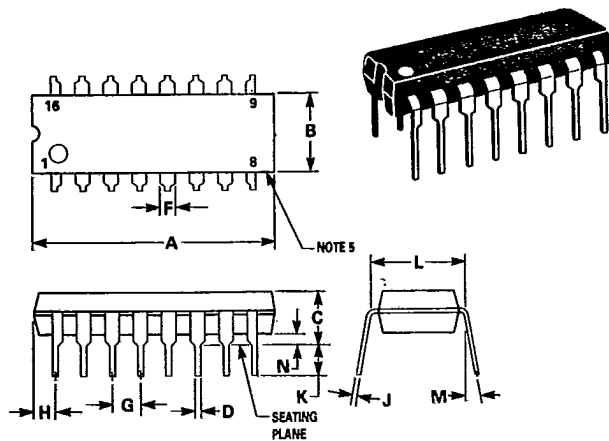


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC	—	0.050 BSC	—
F	1.40	1.77	0.055	0.070
G	2.54 BSC	—	0.100 BSC	—
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC	—	0.300 BSC	—
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

PLASTIC PACKAGE  
CASE 648-06



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC	—	0.100 BSC	—
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC	—	0.300 BSC	—
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

9

0565

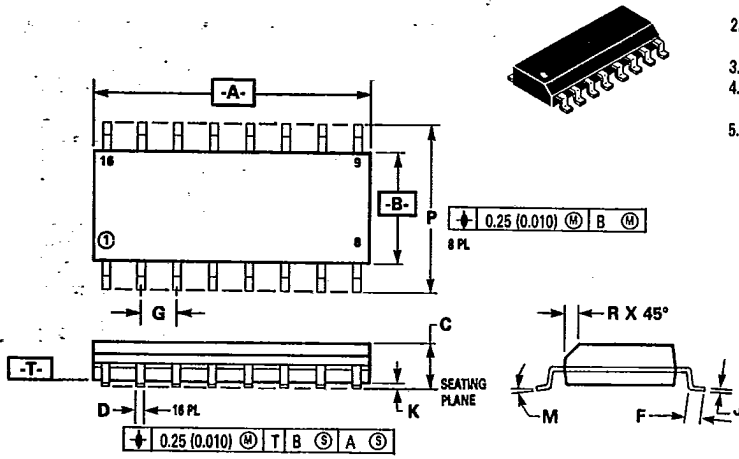
E-14

9-4

PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

SOIC PACKAGE  
CASE 751B-03  
D SUFFIX

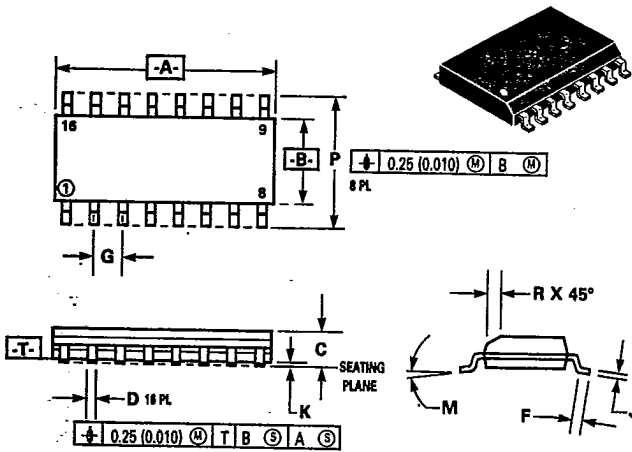


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOIC PACKAGE  
CASE 751G-01  
DW SUFFIX



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

0566 F-01

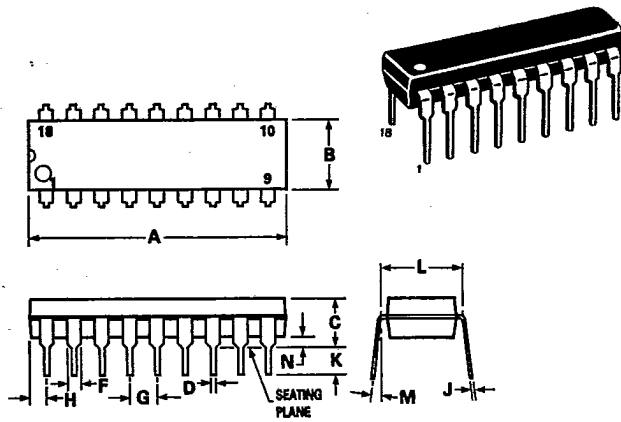
9-5

9

PACKAGE DIMENSIONS (Continued)

18-PIN PACKAGE

PLASTIC PACKAGE  
CASE 707-02

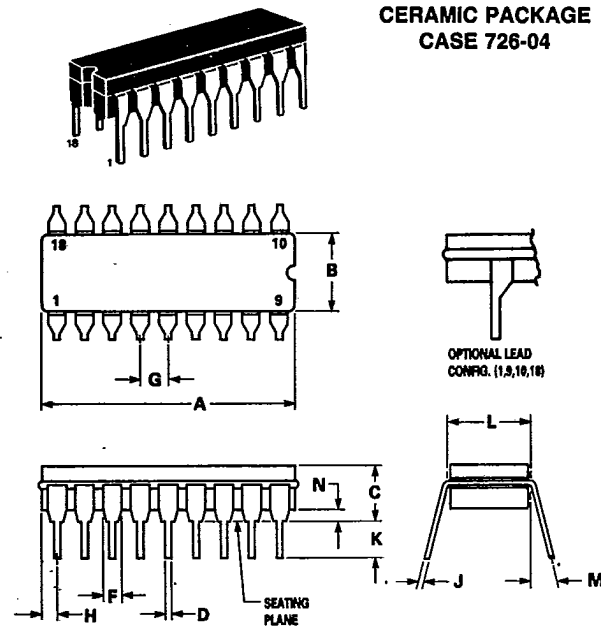


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CERAMIC PACKAGE  
CASE 726-04



NOTES:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.890	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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0567

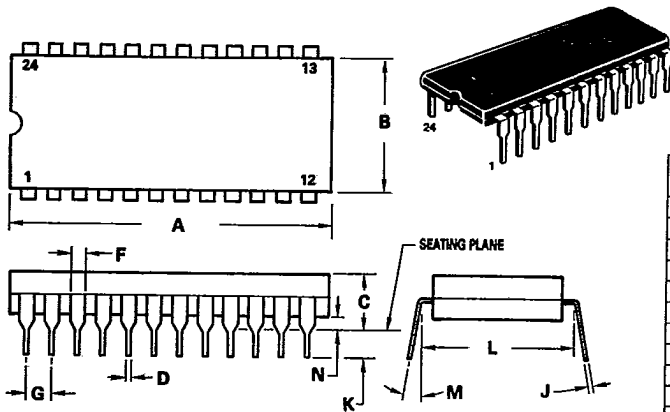
F-02

9-6

PACKAGE DIMENSIONS (Continued)

24-PIN PACKAGE

CERAMIC PACKAGE  
CASE 623-05

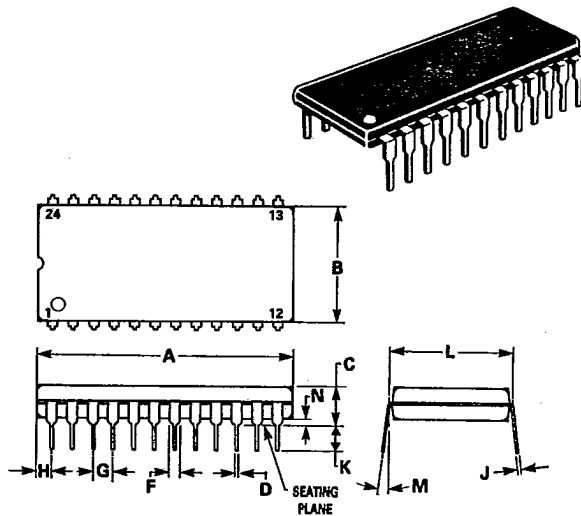


NOTES:

1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

PLASTIC PACKAGE  
CASE 709-02



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040