T-77-11

MOTOROLA

MC145026
MC145027
MC145028
MC145029

Advance Information

MC145026 ENCODER, MC145027/MC145028/MC145029 DECODERS

The MC145026 will encode nine bits of information and serially transmit this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0, 1, open) allowing 3^9 (19,683) different codes.

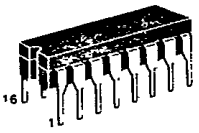
Three decoders are presently available; all use the same transmitter — the MC145026. The decoders receive the 9-bit word and interpret some of the bits as address codes and some as data. The MC145027 interprets the first five transmitted bits as address and the last four bits as data. The MC145029 interprets the first four transmitted bits as address and the last five bits as data. The MC145028 treats all nine bits as address. If no errors are received, the MC145027 outputs four data bits, and the MC145029 outputs five data bits, when the transmitter sends address codes that match that of the receiver. A valid transmission output will go high on the decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

- May be Addressed in either Binary or Trinary
- Trinary Addressing Maximizes Number of Codes
- Interfaces with RF, Ultrasonic, or Infrared Transmission Medias
- On-Chip R/C Oscillator; No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Standard B-Series Input and Output Characteristics
- 4.5 to 18 V Operation
- 2.9 V Low-Voltage Version Also Available by Special Order

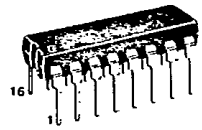
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

REMOTE CONTROL ENCODER/DECODER PAIRS



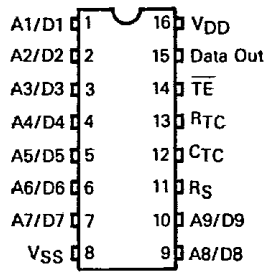
L SUFFIX
CERAMIC PACKAGE
CASE 620



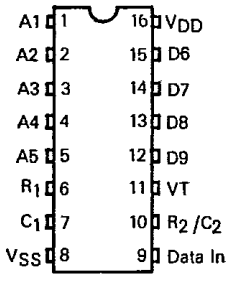
P SUFFIX
PLASTIC PACKAGE
CASE 648

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

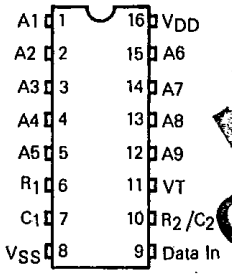
PIN ASSIGNMENTS



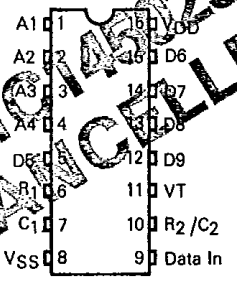
MC145026
Encoder



MC145027
Decoder



MC145028
Decoder



MC145029
Decoder

MC145029 CANCELLED

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.25	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 V)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current Source (V_{OH} = 2.5 V)	I_{OH}	5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mA
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current – $\overline{TE}$ (MC145026, Pullup Device)	I_{in}	5.0	–	–	3.0	4.0	9.0	–	–	µA
		10	–	–	16	20	32	–	–	
		15	–	–	35	45	70	–	–	
Input Current R_S (MC145026) Data In (MC145027, MC145028, MC145029)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Current A1/D1-A9/D9 (MC145026) A1-A5 (MC145027) A1-A9 (MC145028) A1-A4 (MC145029)	I_{in}	5.0	–	–	–	±55	±110	–	–	µA
		10	–	–	–	±300	±500	–	–	
		15	–	–	–	±650	±1000	–	–	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current – MC145026	I_{DD}	5.0	–	–	–	0.0050	0.10	–	–	µA
		10	–	–	–	0.0100	0.20	–	–	
		15	–	–	–	0.0150	0.30	–	–	
Quiescent Current – MC145027, MC145028, MC145029	I_{DD}	5.0	–	–	–	30	50	–	–	µA
		10	–	–	–	60	100	–	–	
		15	–	–	–	90	150	–	–	
Total Supply Current – MC145026 (f_c = 20 kHz)	I_T	5.0	–	–	–	100	200	–	–	µA
		10	–	–	–	200	400	–	–	
		15	–	–	–	300	600	–	–	
Total Supply Current – MC145027, MC145028, MC145029 (f_c = 20 kHz)	I_T	5.0	–	–	–	200	400	–	–	µA
		10	–	–	–	400	800	–	–	
		15	–	–	–	600	1200	–	–	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH} t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Data In Rise and Fall Time (MC145027, MC145028, MC145029)	t_{TLH} t_{THL}	5.0 10 15	– – –	– – –	15 15 15	μs
Encoder Clock Frequency	f_{cl}	5.0 10 15	0 0 0	– – –	2 5 10	MHz
Decoder Frequency (Referenced to Encoder Clock) (See Figure 10)	f_{cl}	5.0 10 15	1 1 1	– – –	240 410 450	kHz
$\overline{TE}$ Pulse Width	t_{WL}	5.0 10 15	65 30 20	– – –	– – –	ns
System Propagation Delay ($\overline{TE}$ to Valid Transmission)	–	–	–	182	–	Clock Cycles
Tolerance on Timing Components $(\Delta R_{TC} + \Delta C_{TC} + \Delta R_1 + \Delta C_1)$ $(\Delta R_2 + \Delta C_2)$	–	– –	– –	– –	±25 ±25	%

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins may be in either of three states (0, 1, open) allowing $3^9 = 19{,}683$ possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder outputs two identical data words. Between the two data words no signal is sent for three data bit times. If the $\overline{TE}$ input is kept low, the encoder continuously transmits the data word.

Each transmitted data bit is encoded into two data pulses (See Figure 7). A logic zero is encoded as two consecutive short pulses, a logic one as two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The $\overline{TE}$ input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the Data Out output pin.

Transmission must be initiated by using the $\overline{TE}$ pin rather than by holding $\overline{TE}$ low and applying power to the device because an internal reset occurs after the first transmit sequence.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical data words, is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address input at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches by VT and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid address has been received.

Although address information is normally encoded in trinary, the designer should be aware that, for the MC145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2 \times 3^8 = 13{,}122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However, if the encoder sends a trinary (or logic 1) and the decoder address is a logic 1 (or trinary) respectively, the valid transmission output length will be shortened to the $R1 \times C1$ time constant.

MC145029

This decoder operates like the MC145027, but it assumes the first four received bits to be address bits and the remaining five received bits to be data.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a vaild transmission output.

PIN DESCRIPTIONS

MC145026 ENCODER

A1/D1-A9/D9, ADDRESS/DATA INPUTS (PINS 1, 2, 3, 4, 5, 6, 7, 9, 10) — These inputs are encoded and the data is serially output from the encoder.

R_S, C_{TC}, R_{TC}, OSCILLATOR COMPONENTS (PINS 11, 12, 13) — These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$, TRANSMIT-ENABLE INPUT (PIN 14) This active low input initiates transmission when forced low. An internal pullup device keeps this input normally high.

Data Out, DATA OUTPUT (PIN 15) — This is the output of the encoder that serially presents the encoded word.

V_{DD}, POSITIVE SUPPLY (PIN 16) — The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) — The most negative supply (usually ground).

MC145027, MC145028, MC145029 DECODERS

A1-A5 (MC145027), A1-A9 (MC145028), A1-A4 (MC145029), ADDRESS INPUTS — These address inputs must match the corresponding encoder inputs in order for the decoder to output data.

D6-D9 (MC145027), D5-D9 (MC145029), DATA OUTPUTS — These outputs present the information that is on the corresponding encoder inputs. Note: only binary data will be acknowledged; a trinary open will be decoded as a logic one.

R_1, C_1, PULSE DISCRIMINATOR (PINS 6, 7) — These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant $R_1 \times C_1$ should be set to 1.72 encoder (transmitter) clock periods. $R_1C_1 = 3.95\ R_{TC}C_{TC}$.

R_2/C_2, DEAD TIME DISCRIMINATOR (PIN 10) — This pin accepts a resistor and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder (transmitter) clock periods (four data bit periods): $R_2C_2 = 77\ R_{TC}C_{TC}$. This time constant is used to determine that Data In has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage-equivalent two data bit times (0.4 R_2C_2) to detect the dead time between transmitted words.

VT, VALID TRANSMISSION (PIN 11) — This output goes high when the following conditions are satisfied:

1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (MC145027 and MC145029, only).

VT will remain high until a mismatch is received, or no input signal is received for four data bit times.

V_{DD}, POSITIVE SUPPLY (PIN 16) — The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) — The most negative supply (usually ground).

FIGURE 1— MC145026 ENCODER BLOCK DIAGRAM

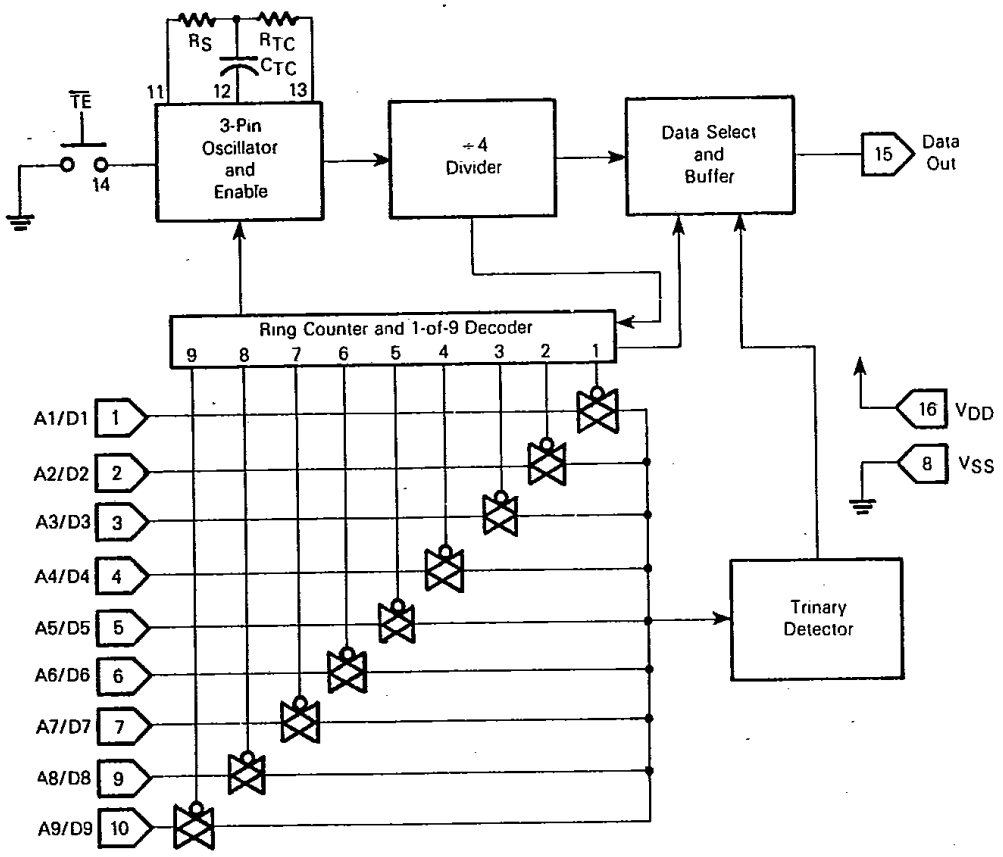


FIGURE 2 — MC145027 DECODER BLOCK DIAGRAM

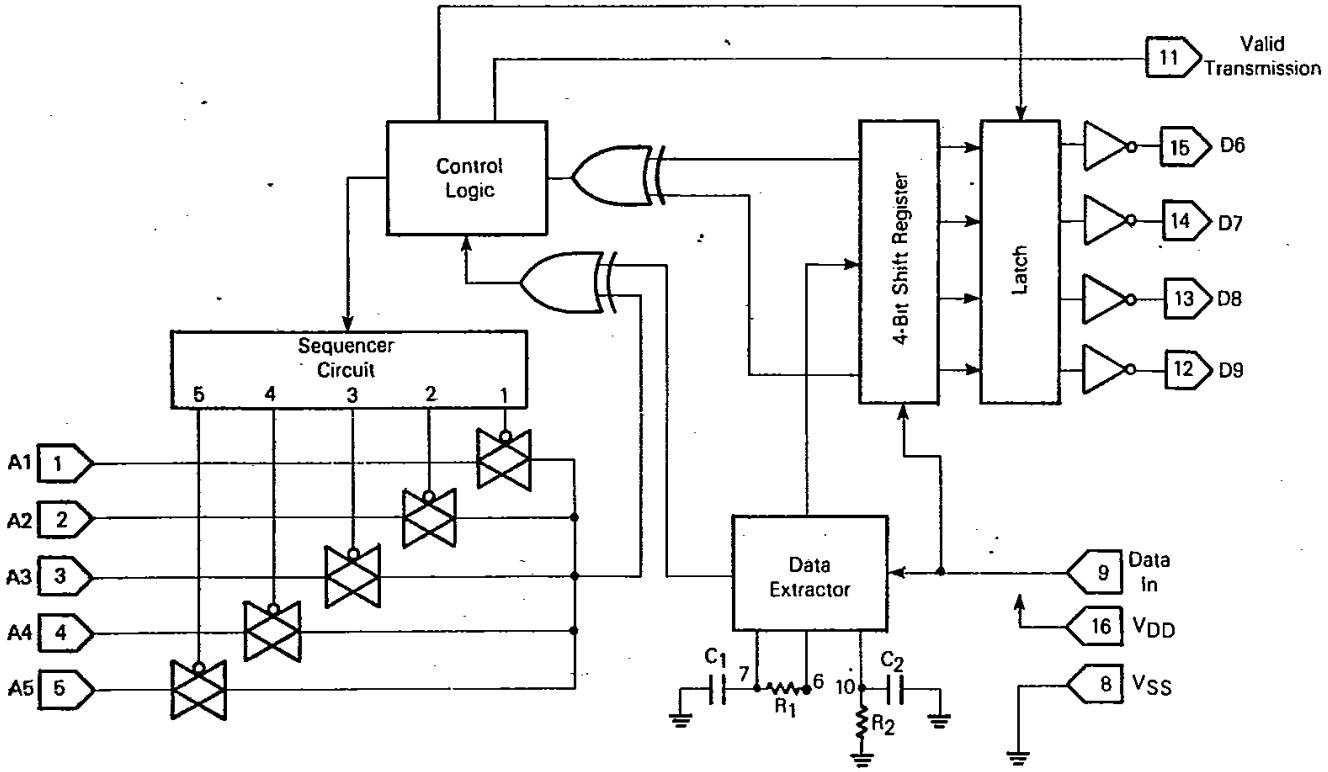


FIGURE 3 — MC145028 DECODER BLOCK DIAGRAM

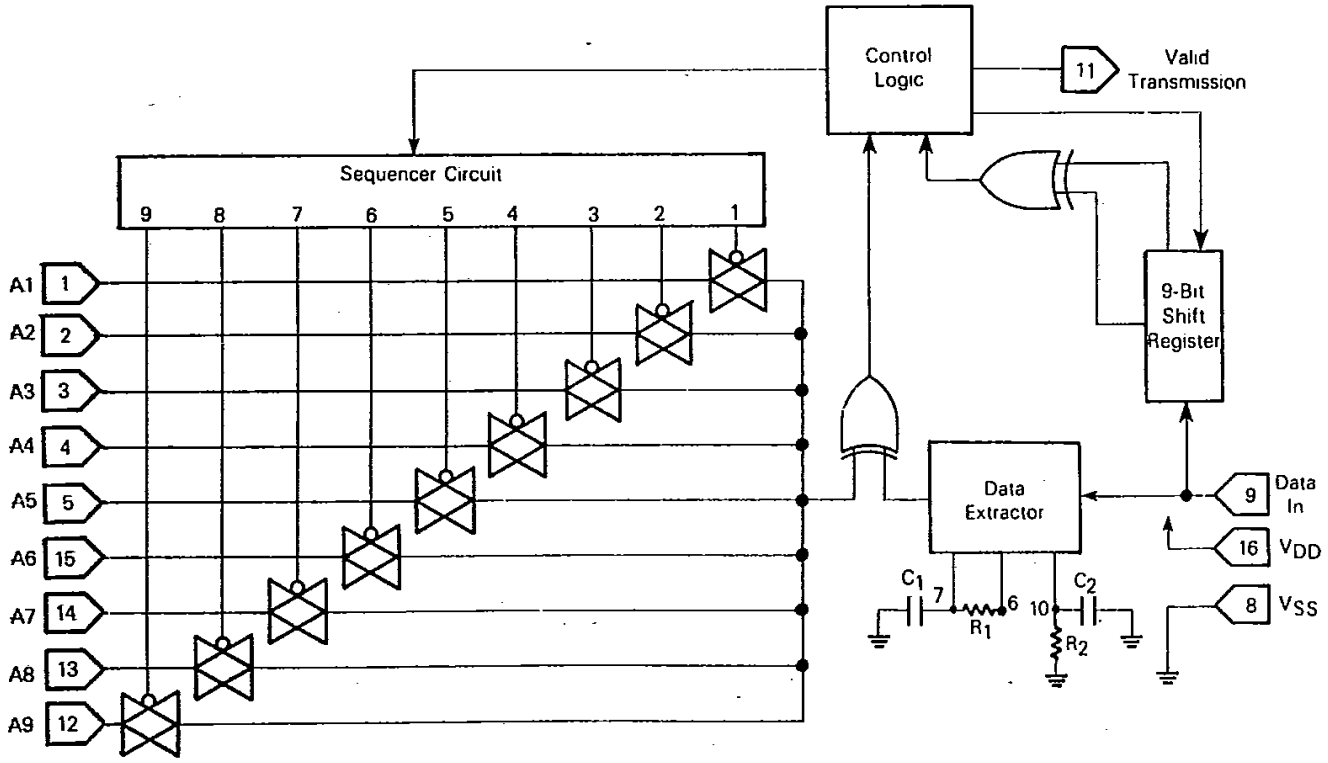


FIGURE 4 — MC145029 DECODER BLOCK DIAGRAM

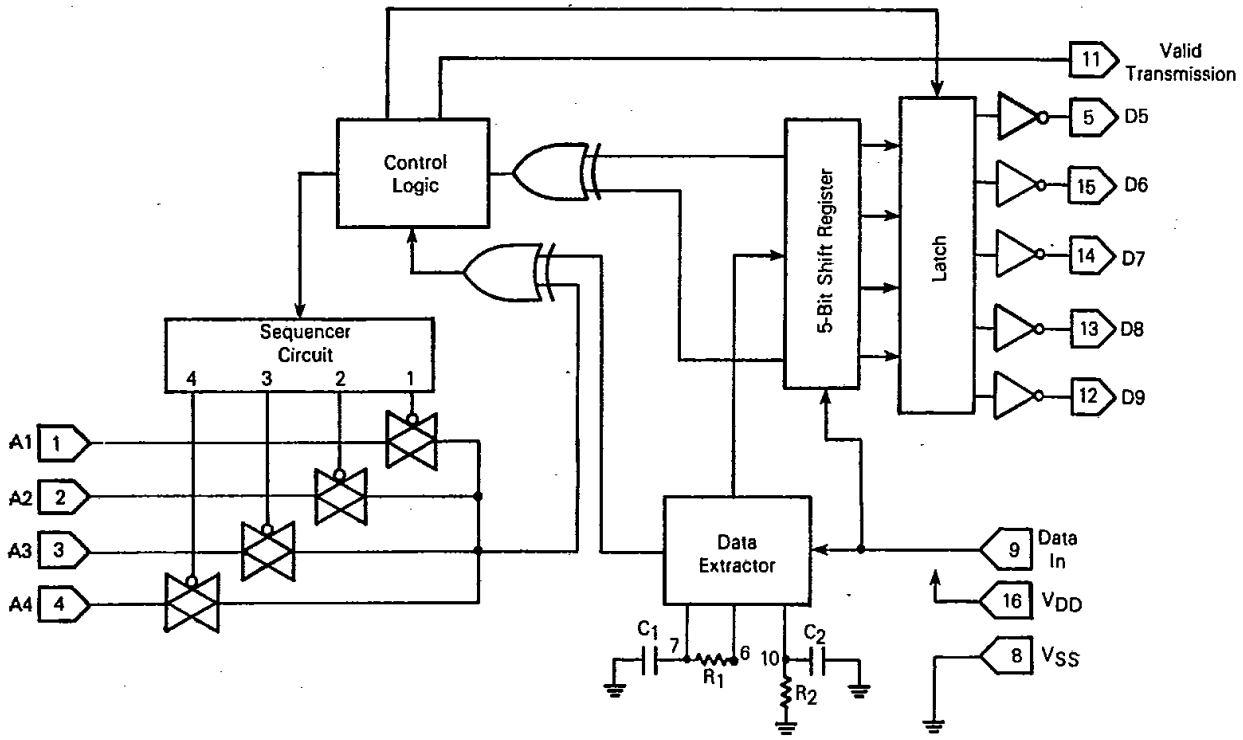
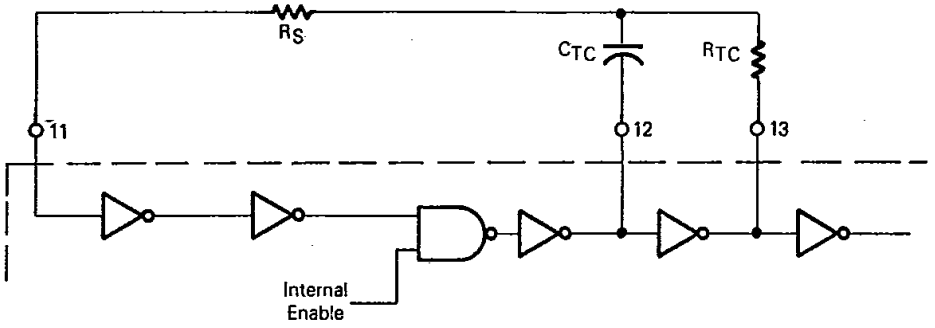


FIGURE 5 — ENCODER OSCILLATOR INFORMATION



This oscillator will operate at a frequency determined by the external RC network; i.e.,

$$f \cong \frac{1}{2.3\, R_{TC}\, C_{TC}'} \text{ (Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\, R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 μF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range will ensure that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that $R_S \times 5$ pF (input capacitance) is small compared to $R_{TC} \times C_{TC}$.

For frequencies outside the indicated range, the formula will be less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

FIGURE 6 — ENCODER/DECODER TIMING DIAGRAM

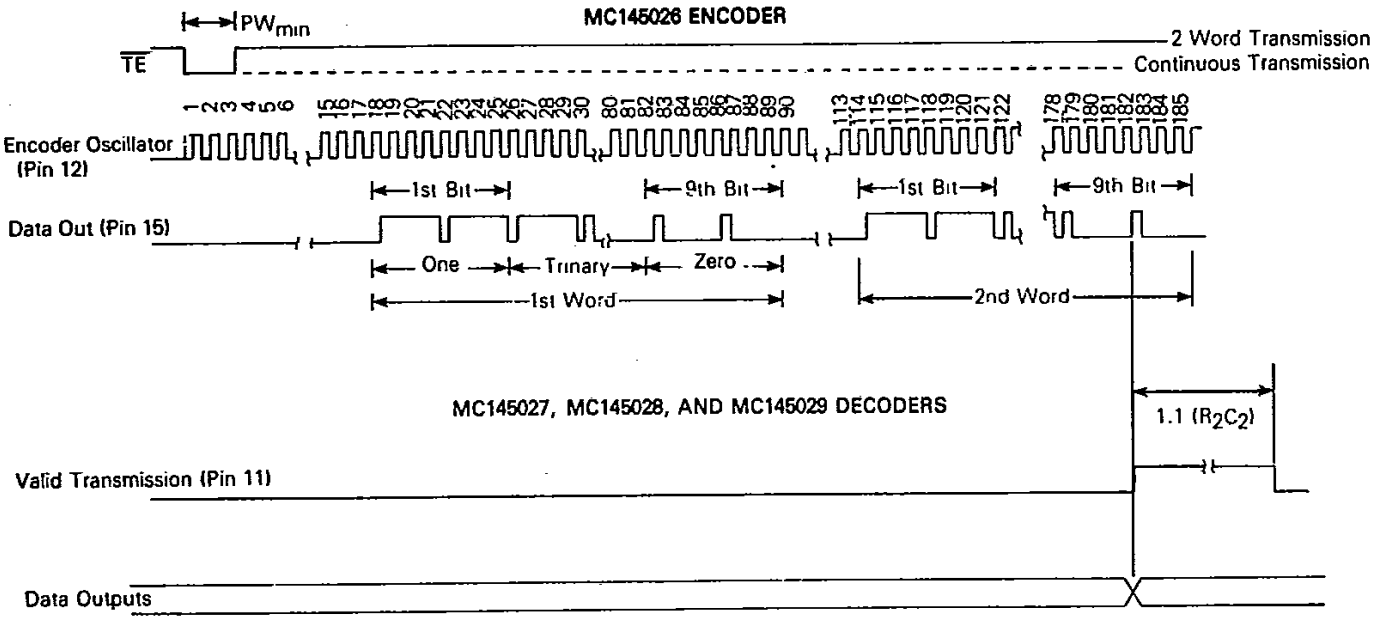


FIGURE 7 — MC145026 ENCODER DATA WAVEFORMS

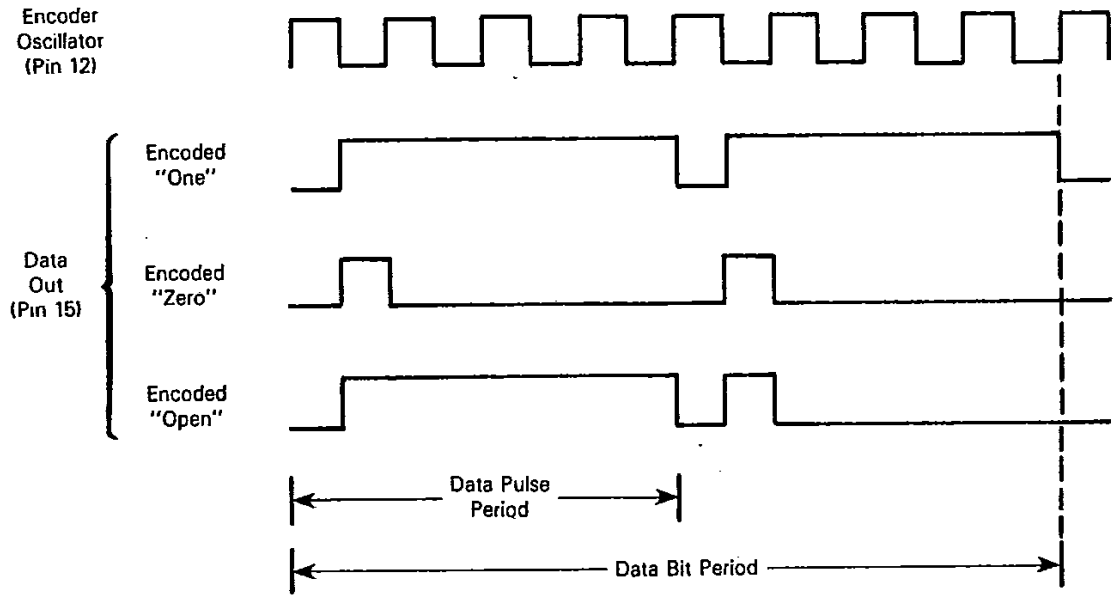


FIGURE 8 — MC145027/MC145029 FLOWCHART

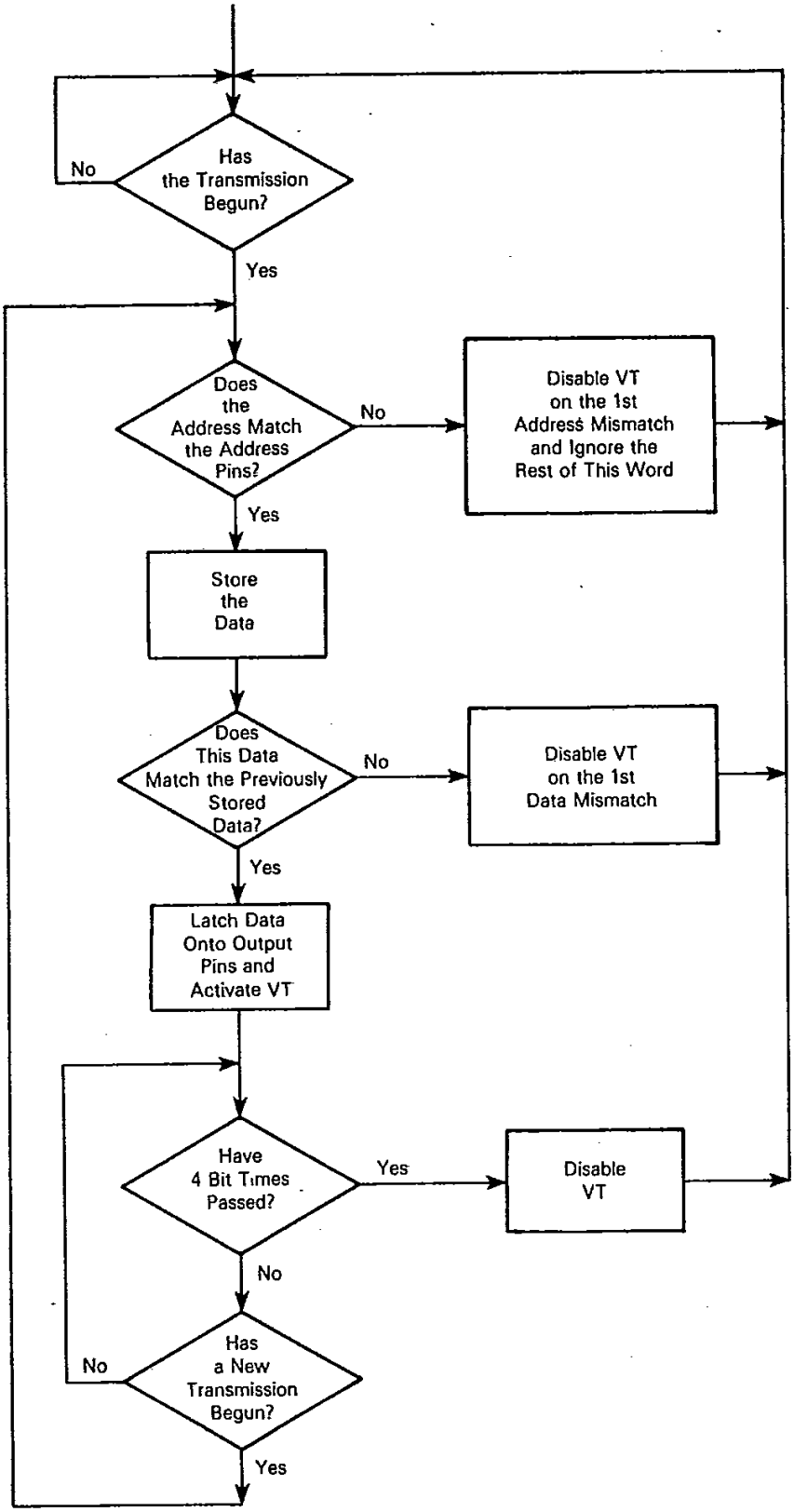
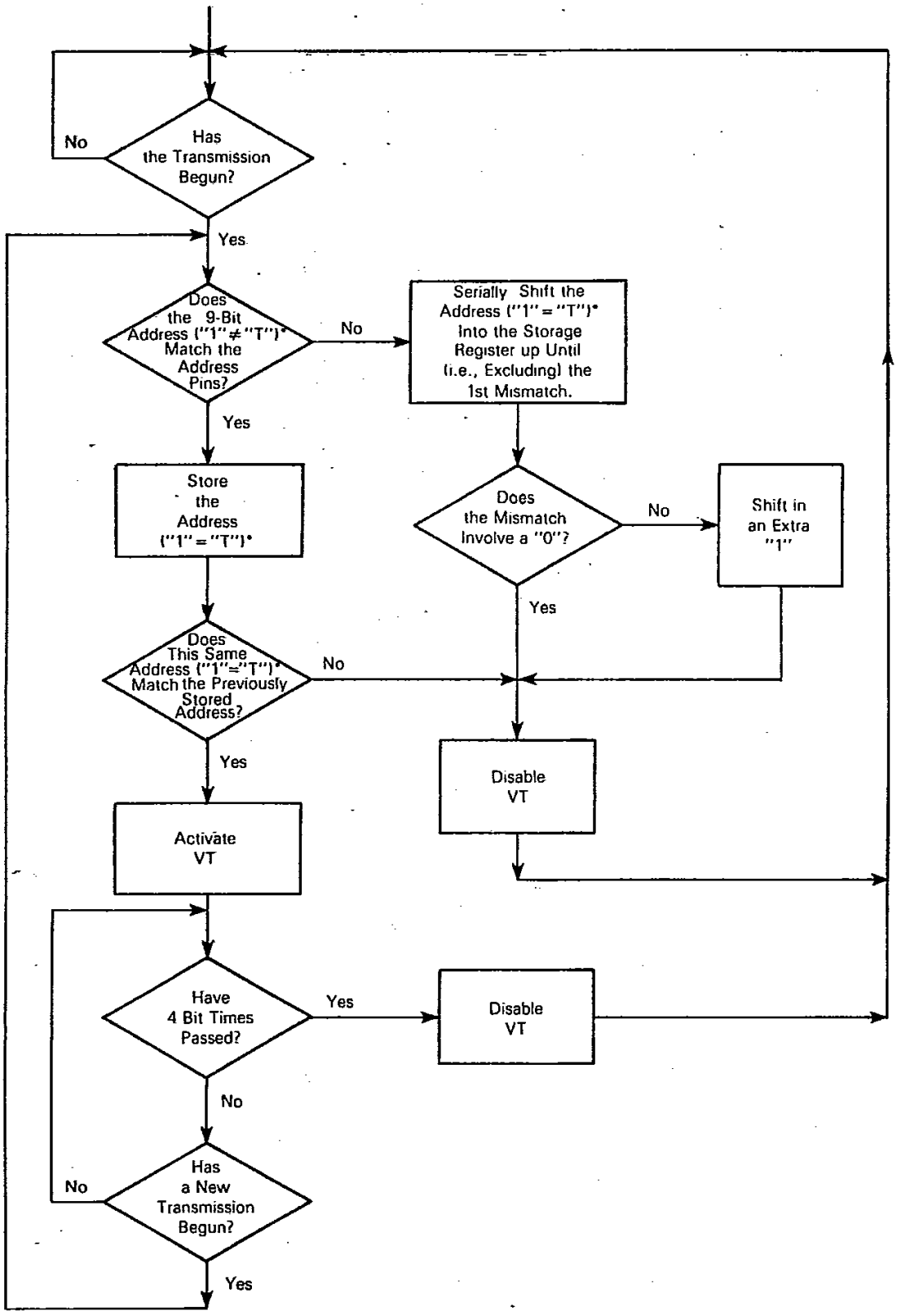
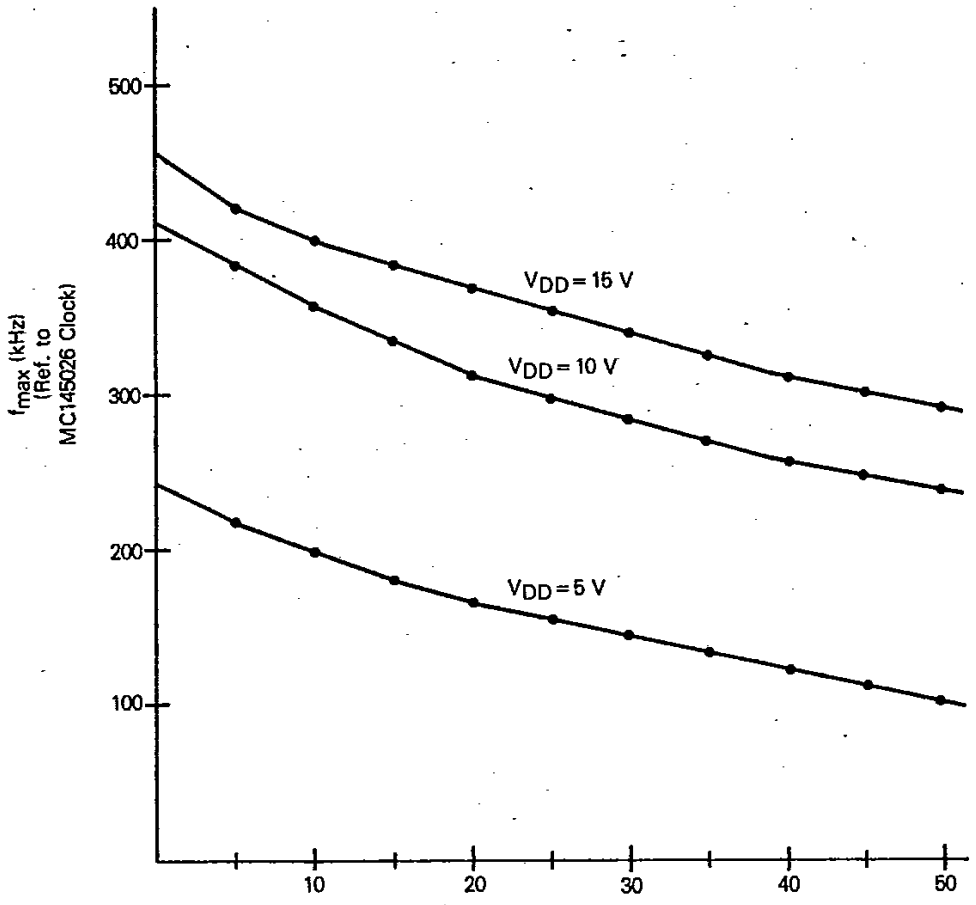


FIGURE 9 — MC145028 FLOWCHART



*For shift register comparisons, a "T" is stored as a "1".

FIGURE 10 — f_{max} vs C_{layout}
MC145027, MC145028, and MC145029



C_{layout} (pF) on Pins 1-5 (MC145027); Pins 1-5 and 12-15 (MC145028); Pins 1-4 (MC145029)

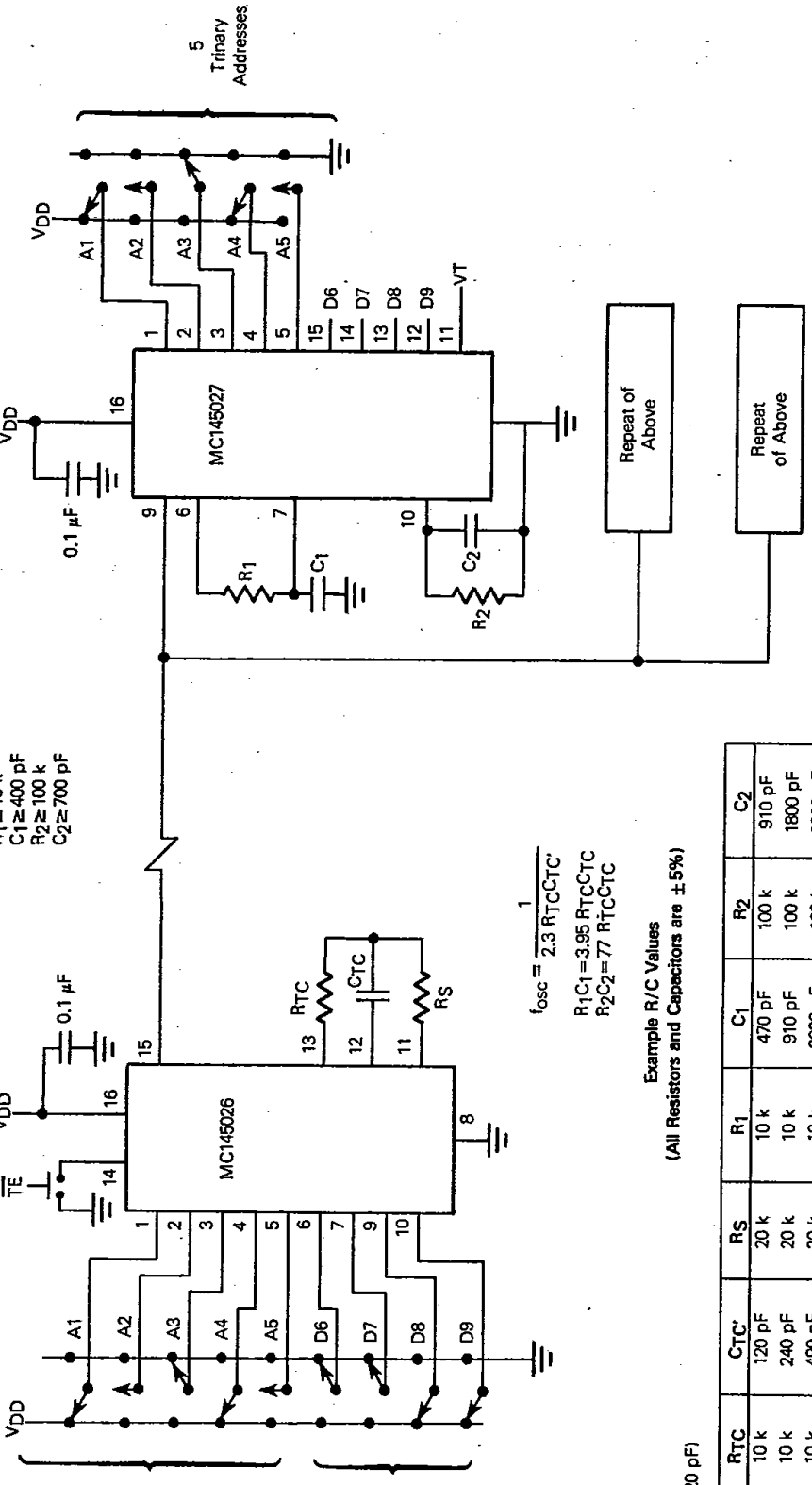


FIGURE 11 – TYPICAL APPLICATION

Example R/C Values
(All Resistors and Capacitors are ±5%)

($C_{TC'} = C_{TC} + 20$ pF)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF