# Programmable Timer Module (PTM)

The MC6840 is a programmable subsystem component of the M6800 Family designed to provide variable system time intervals.

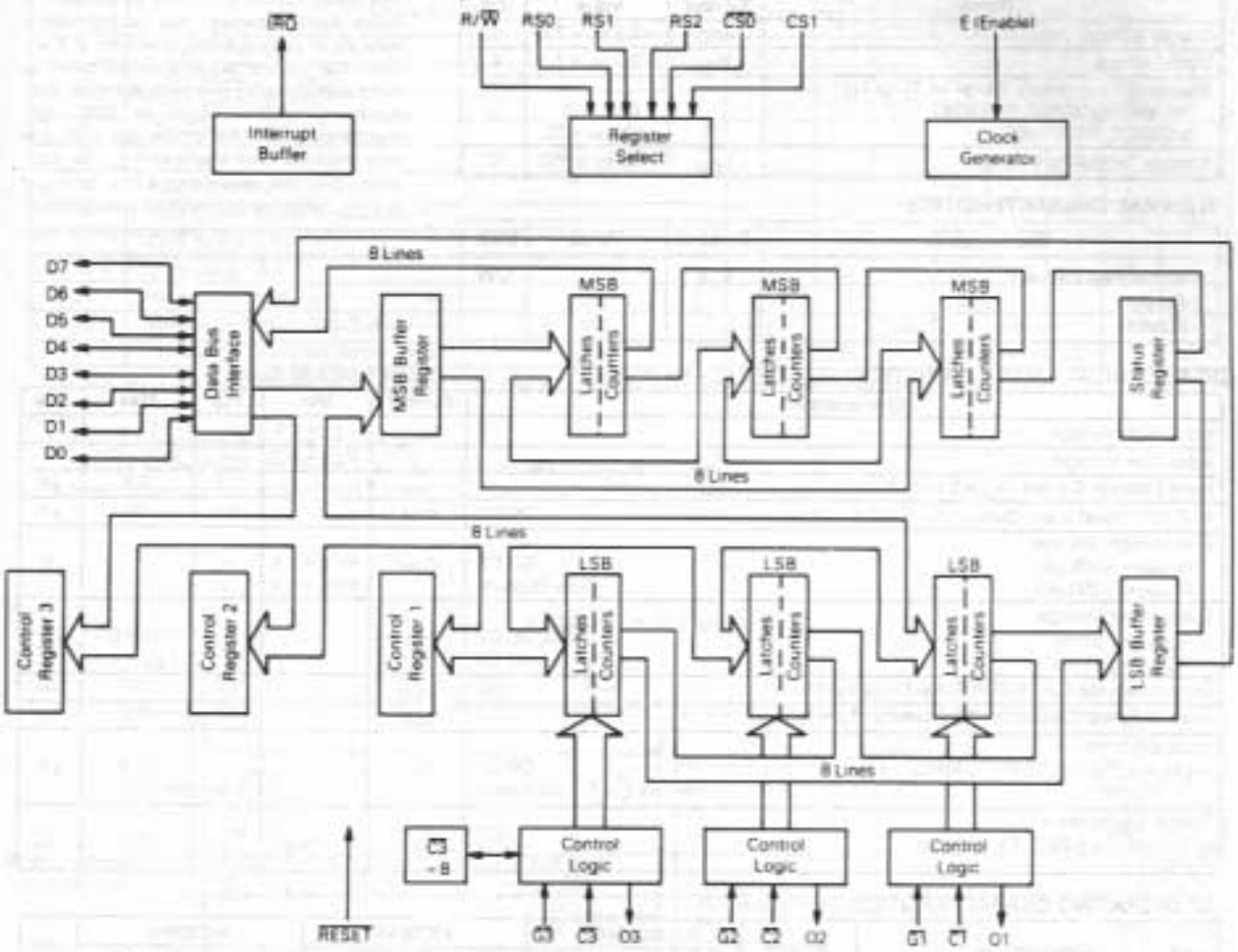
The MC6840 has three 16-bit binary counters, three corresponding control registers, and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The MC6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring, and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- Operates from a Single 5-Volt Power Supply
- Fully TTL Compatible
- Single System Clock Required (Enable)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the MC6840, 6 MHz for the MC68A40 and 8 MHz for the MC68B40
- Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go Until Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- $\overline{RESET}$ Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs



This document contains information on a new product. Specifications and information herein are subject to change without notice.

## BLOCK DIAGRAM




## POWER CONSIDERATIONS

The average chip-junction temperature, $T_J$, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

$T_A$ = Ambient Temperature, °C
$\theta_{JA}$ = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{PORT}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{PORT}$ = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} < P_{INT}$ and can be neglected. $P_{PORT}$ may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between $P_D$ and $T_J$ (if $P_{PORT}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | V |
| Operating Temperature Range — $T_L$ to $T_H$<br>MC6840, MC68A40, MC68B40<br>MC6840C, MC68A40C | $T_A$ | 0 to +70<br>−40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{CC}$).

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>Cerdip<br>Plastic | $\theta_{JA}$ | <br>65<br>100 | °C/W |

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 Vdc ±5%, $V_{SS}$ = 0, $T_A = T_L$ to $T_H$ unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input High Voltage | | $V_{IH}$ | $V_{SS}$ + 2.0 | – | $V_{CC}$ | V |
| Input Low Voltage | | $V_{IL}$ | $V_{SS}$ − 0.3 | – | $V_{SS}$ + 0.8 | V |
| Input Leakage Current ($V_{in}$ = 0 to 5.25 V) | | $I_{in}$ | – | 1.0 | 2.5 | μA |
| Hi-Z (Off State) Input Current ($V_{in}$ = 0.5 to 2.4 V) | D0-D7 | $I_{TSI}$ | – | 2.0 | 10 | μA |
| Output High Voltage<br>($I_{Load}$ = −205 μA)<br>($I_{Load}$ = −200 μA) | D0-D7<br>Other Outputs | $V_{OH}$ | $V_{SS}$ + 2.4<br>$V_{SS}$ + 2.4 | –<br>– | –<br>– | V |
| Output Low Voltage<br>($I_{Load}$ = 1.6 mA)<br>($I_{Load}$ = 3.2 mA) | $\overline{IRQ}$, D0-D7<br>O1-O3 | $V_{OL}$ | –<br>– | –<br>– | $V_{SS}$ + 0.4<br>$V_{SS}$ + 0.4 | V |
| Output Leakage Current (Off State) ($V_{OH}$ = 2.4 V) | $\overline{IRQ}$ | $I_{LOH}$ | – | 1.0 | 10 | μA |
| Internal Power Dissipation (Measured at $T_A = T_L$) | | $P_{INT}$ | – | 470 | 700 | mW |
| Input Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | D0-D7<br>All Others | $C_{in}$ | –<br>– | –<br>– | 12.5<br>7.5 | pF |
| Output Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | $\overline{IRQ}$<br>O1, O2, O3 | $C_{out}$ | –<br>– | –<br>– | 5.0<br>10 | pF |

## AC OPERATING CHARACTERISTICS (See Figures 2-7)

| Characteristic | Symbol | MC6840 | | MC68A40 | | MC68B40 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Input Rise and Fall Times<br>(Figures 4 and 5) $\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | $t_r$, $t_f$ | – | 1.0* | – | 0.666* | – | 0.500* | μs |
| Input Pulse Width Low (Figure 2)<br>(Asynchronous Input)<br>$\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | $PW_L$ | $t_{cycE} + t_{su} + t_{hd}$ | – | $t_{cycE} + t_{su} + t_{hd}$ | – | $t_{cycE} + t_{su} + t_{hd}$ | – | ns |
| Input Pulse Width High (Figure 3)<br>(Asynchronous Input) $\overline{C}$, $\overline{G}$ | $PW_H$ | $t_{cycE} + t_{su} + t_{hd}$ | – | $t_{cycE} + t_{su} + t_{hd}$ | – | $t_{cycE} + t_{su} + t_{hd}$ | – | ns |
| Input Setup Time (Figure 4)<br>(Synchronous Input)<br>$\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | $t_{su}$ | 200 | – | 120 | – | 75 | – | ns |
| Input Hold Time (Figure 4)<br>(Synchronous Input)<br>$\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | $t_{hd}$ | 50 | – | 50 | – | 50 | – | ns |
| Input Synchronization Time (Figure 7)<br>$\overline{C3}$ (÷8 Prescaler Mode Only) | $t_{sync}$ | 250 | – | 200 | – | 175 | – | ns |
| Input Pulse Width<br>$\overline{C3}$ (÷8 Prescaler Mode Only) | $PW_L$, $PW_H$ | 120 | – | 80 | – | 60 | – | ns |
| Output Delay, O1-O3 (Figure 5)<br>($V_{OH}$ = 2.4 V, Load B) TTL<br>($V_{OH}$ = 2.4 V, Load D) MOS<br>($V_{OH}$ = 0.7 $V_{DD}$, Load D) CMOS | $t_{co}$<br>$t_{om}$<br>$t_{cmos}$ | –<br>–<br>– | 700<br>450<br>2.0 | –<br>–<br>– | 460<br>450<br>1.35 | –<br>–<br>– | 340<br>340<br>1.0 | ns<br>ns<br>μs |
| Interrupt Release Time (Figure 6) | $t_{IR}$ | – | 1.2 | – | 0.9 | – | 0.7 | μs |

*$t_r$ and $t_f \le t_{cycE}$

**BUS TIMING CHARACTERISTICS** (See Notes 1, 2, and 3)

| Ident. Number | Characteristic | Symbol | MC6840 | | MC68A40 | | MC68B40 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | Cycle Time | $t_{cyc}$ | 1.0 | 10 | 0.67 | 10 | 0.5 | 10 | μs |
| 2 | Pulse Width, E Low | $PW_{EL}$ | 430 | 9500 | 280 | 9500 | 210 | 9500 | ns |
| 3 | Pulse Width, E High | $PW_{EH}$ | 450 | 9500 | 280 | 9500 | 220 | 9500 | ns |
| 4 | Clock Rise and Fall Time | $t_r$, $t_f$ | – | 25 | – | 25 | – | 20 | ns |
| 9 | Address Hold Time | $t_{AH}$ | 10 | – | 10 | – | 10 | – | ns |
| 13 | Address Setup Time Before E | $t_{AS}$ | 80 | – | 60 | – | 40 | – | ns |
| 14 | Chip Select Setup Time Before E | $t_{CS}$ | 80 | – | 60 | – | 40 | – | ns |
| 15 | Chip Select Hold Time | $t_{CH}$ | 10 | – | 10 | – | 10 | – | ns |
| 18 | Read Data Hold Time | $t_{DHR}$ | 20 | 50* | 20 | 50* | 20 | 50* | ns |
| 21 | Write Data Hold Time | $t_{DHW}$ | 10 | – | 10 | – | 10 | – | ns |
| 30 | Peripheral Output Data Delay Time | $t_{DDR}$ | – | 290 | – | 180 | – | 150 | ns |
| 31 | Peripheral Input Data Setup Time | $t_{DSW}$ | 165 | – | 80 | – | 60 | – | ns |

*The data bus output buffers are no longer sourcing or sinking current by $t_{DHR}$ max (High Impedance).

NOTES:
1. Not all signals are applicable to every part.
2. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 1 — BUS TIMING

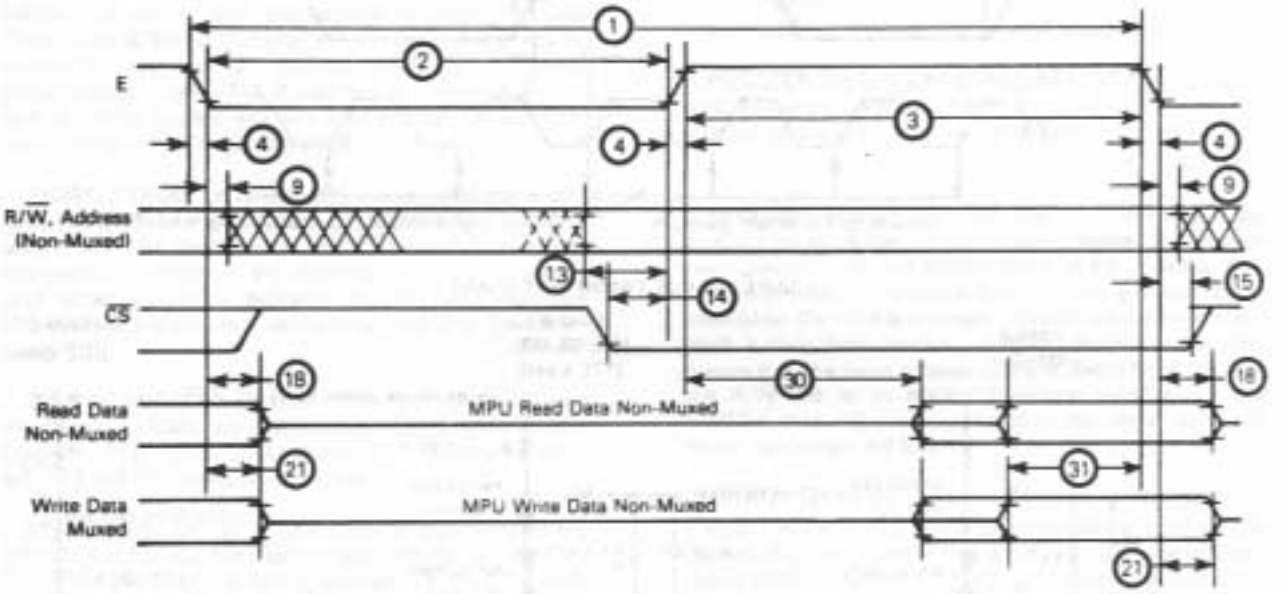



FIGURE 2 — INPUT PULSE WIDTH LOW

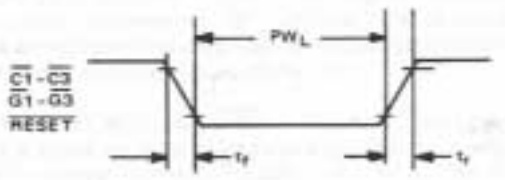



FIGURE 3 — INPUT PULSE WIDTH HIGH