

MM74C240 • MM74C244

Inverting • Non-Inverting Octal Buffer and Line Driver with 3-STATE Outputs

General Description

The MM74C240 and MM74C244 octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with 3-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

Features

- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- 3-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

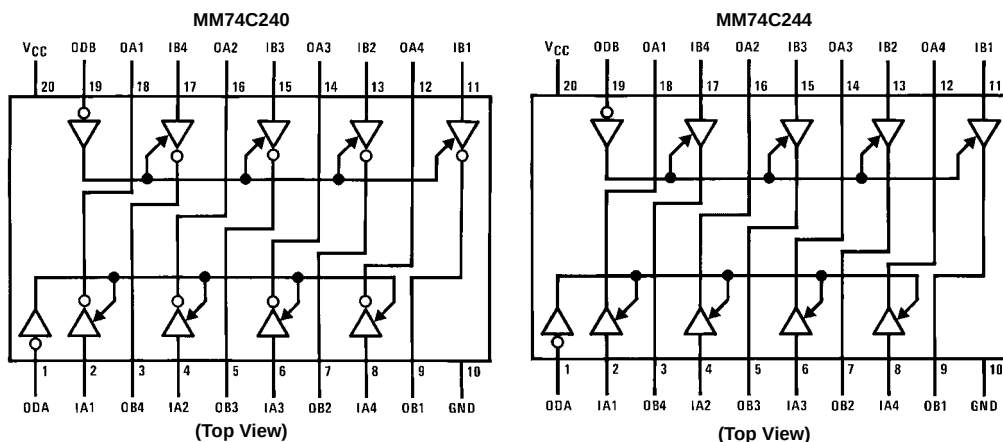
Ordering Code:

Order Number	Package Number	Package Description
MM74C240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
MM74C240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
MM74C244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

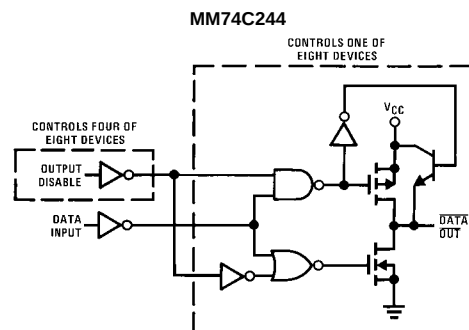
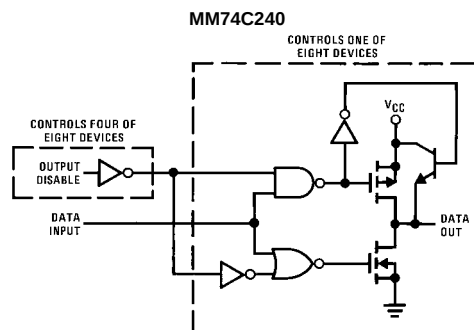
Connection Diagrams

Pin Assignments for DIP and SOIC



MM74C240 • MM74C244 Inverting • Non-Inverting Octal Buffer and Line Driver with 3-STATE Outputs

Logic Diagrams



Truth Tables

MM74C240

ODA	IA	OA
1	X	Z
1	X	Z
0	0	1
0	1	0

ODB	IB	OB
1	X	Z
1	X	Z
0	0	1
0	1	0

MM74C244

ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

1 = HIGH
 0 = LOW
 X = Don't Care
 Z = 3-STATE

Absolute Maximum Ratings (Note 1)		Absolute Maximum V_{CC}	18V
Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$	Lead Temperature (Soldering, 10 seconds)	260°C
Operating Temperature Range	$-40^{\circ}C$ to $+85^{\circ}C$		
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$		
Power Dissipation			
Dual-In-Line	700 mW		
Small Outline	500 mW		
Operating V_{CC} Range	3V to 15V		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted

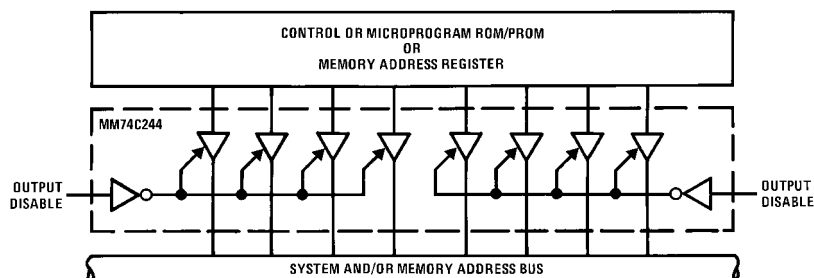
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$			0.5 1.0	V
I_{OZ}	3-STATE Output Current	$V_{CC} = 10V, OD = V_{IH}$			± 10	μA
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -450 \mu A$ $V_{CC} = 4.75V, I_O = -2.2 mA$	$V_{CC} - 0.4$ 2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 2.2 mA$			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$ $V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$	-14 -36	-30 -70		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$ $V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$	12 48	20 70		mA

AC Electrical Characteristics (Note 2) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

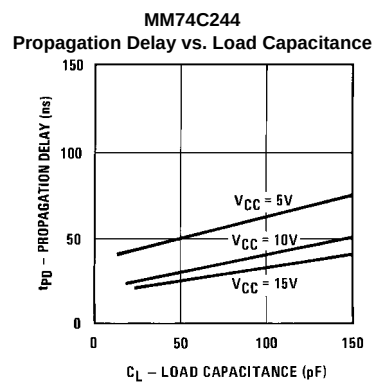
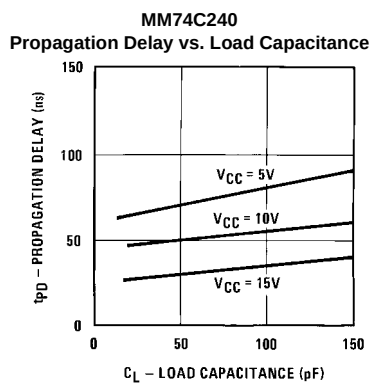
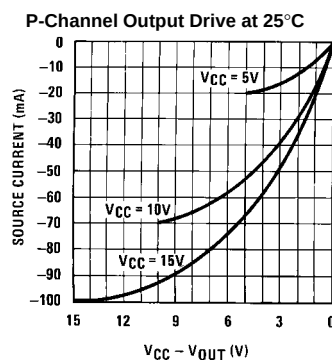
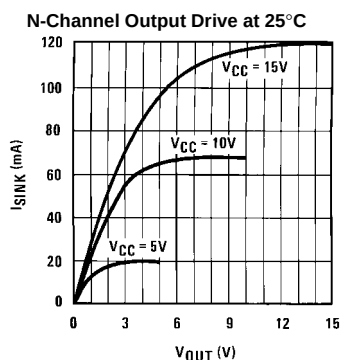
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PD(1)}$, $t_{PD(0)}$	Propagation Delay (Data In to Out) MM74C240	$V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$		60	90	ns
		$V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$		40	70	ns
		$V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$		80	110	ns
		$V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$		60	90	ns
	MM74C244	$V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$		45	70	ns
		$V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$		25	50	ns
		$V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$		60	90	ns
		$V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$		40	70	ns
t_{1H} , t_{0H}	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1\text{k}$, $C_L = 50\text{ pF}$				
		$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		45 35	80 60	ns ns
t_{H1} , t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1\text{k}$, $C_L = 50\text{ pF}$				
		$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		50 30	90 60	ns ns
$t_{T(HL)}$, $t_{T(LH)}$	Transition Time	$V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$		45	80	ns
		$V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$		30	60	ns
		$V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$		75	140	ns
		$V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled per Buffer) MM74C240 MM74C244	(Note 3)				
				100 100		pF pF
	(Output Disabled per Buffer) MM74C240 MM74C244			10 0		pF pF
C_{IN}	Input Capacitance (Note 4) (Any Input)	$V_{IN} = 0\text{V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$		10		pF
C_O	Output Capacitance (Note 4) (Output Disabled)	$V_{IN} = 0\text{V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$		10		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.**Note 3:** C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note, AN-90.**Note 4:** Capacitance is guaranteed by periodic testing.

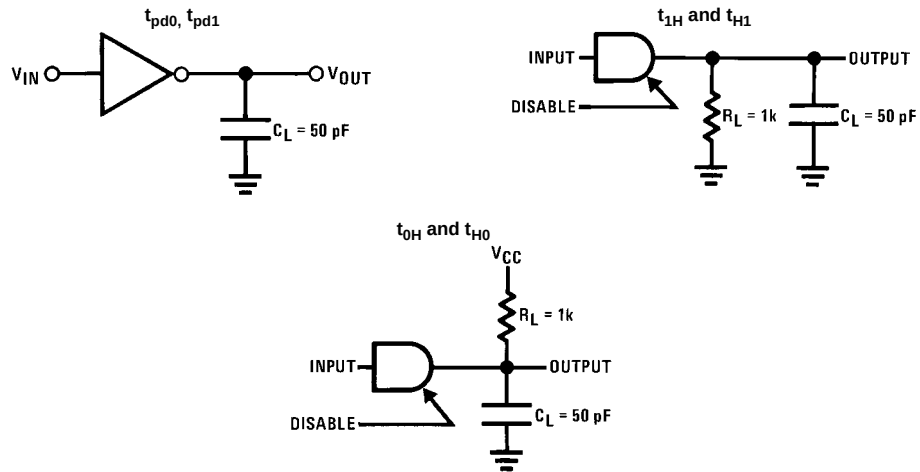
Typical Application



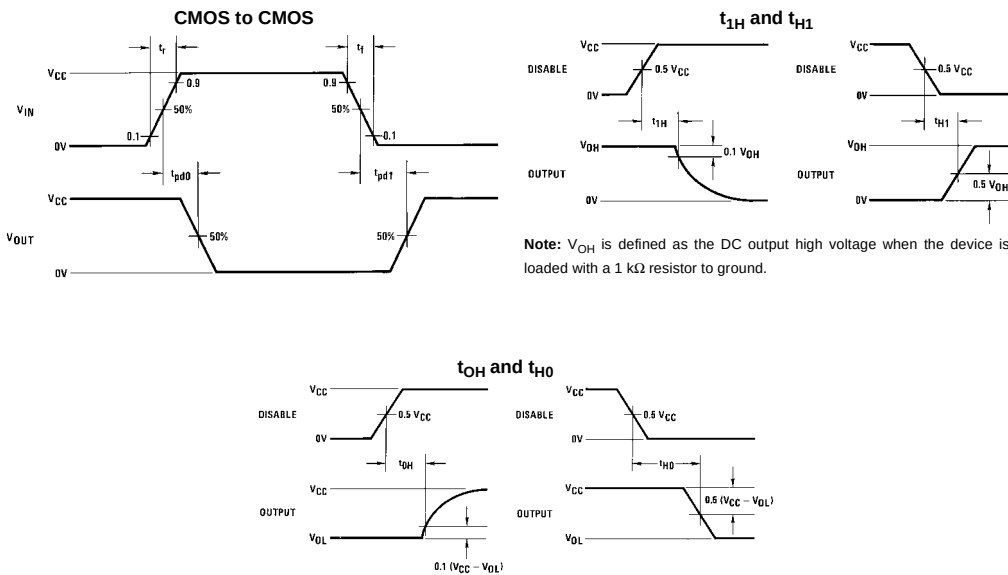
Typical Performance Characteristics



AC Test Circuits and Switching Time Waveforms



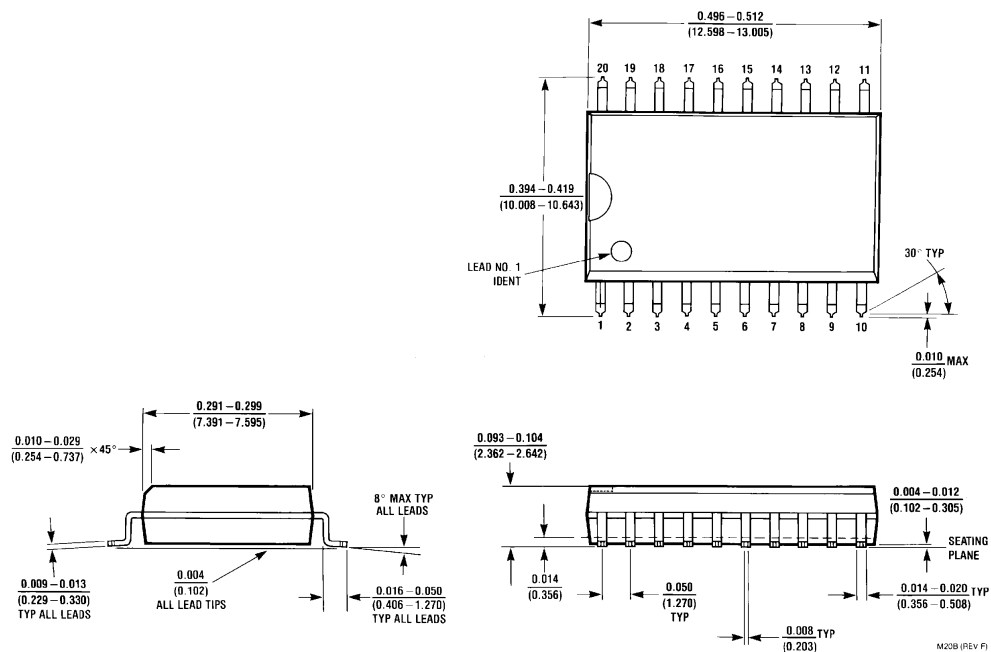
Note: Delays measured with input t_r , $t_f \leq 20 \text{ ns}$.



Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a $1 \text{ k}\Omega$ resistor to ground.

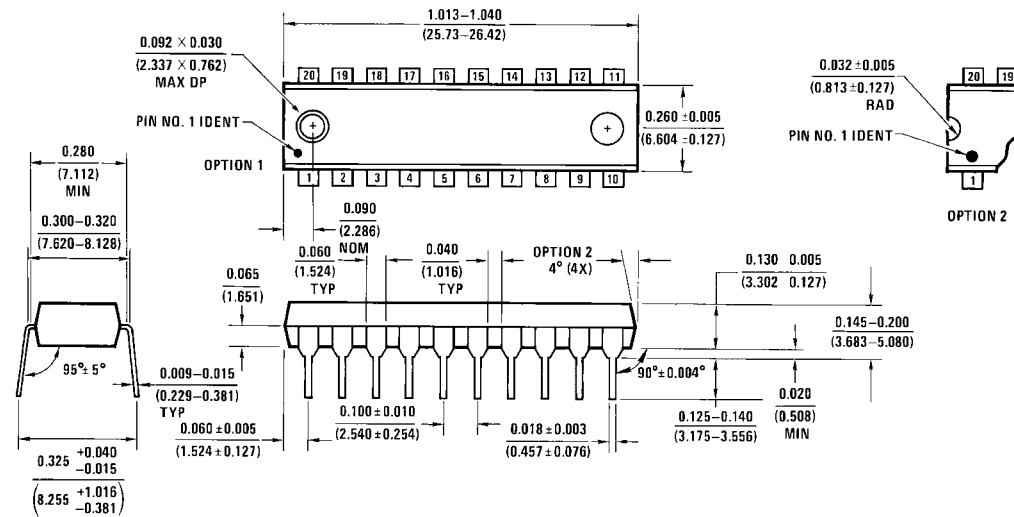
Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a $1 \text{ k}\Omega$ resistor to V_{CC} .

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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