

## MM74HC175 Quad D-Type Flip-Flop With Clear

### General Description

The MM74HC175 high speed D-type flip-flop with complementary outputs utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the D inputs of the MM74HC175 is transferred to the Q and  $\bar{Q}$  outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip-flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four  $\bar{Q}$  outputs to a logical "1."

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

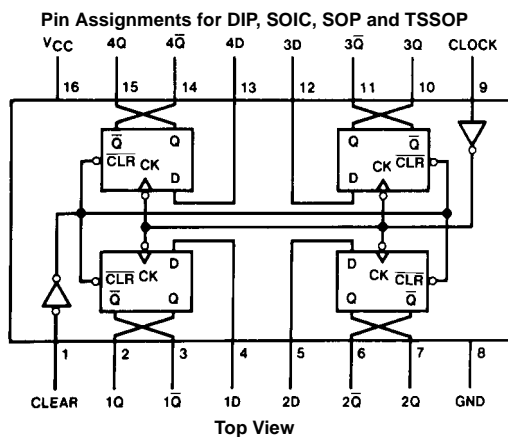
- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum
- Low quiescent supply current: 80  $\mu$ A maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC175M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC175N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



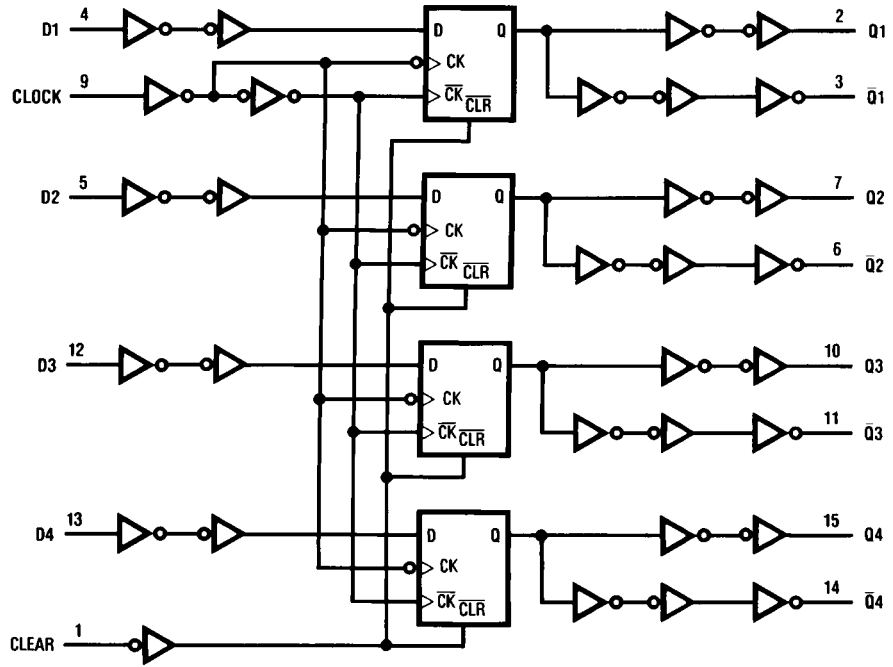
### Truth Table

(Each Flip-Flop)

Clear	Inputs			Outputs	
	Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	L	X	$Q_0$	$\bar{Q}_0$	

H = HIGH Level (steady state)  
L = LOW Level (steady state)  
X = Irrelevant  
↑ = Transition from LOW-to-HIGH level  
 $Q_0$  = The level of Q before the indicated steady-state input conditions were established

### Logic Diagram



Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions			
(Note 2)			<b>Min</b>	<b>Max</b>	<b>Units</b>
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V	Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$	DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$	Operating Temperature Range ( $T_A$ )	-40	+85	°C
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA	Input Rise or Fall Times ( $t_r, t_f$ )			
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA	$V_{CC} = 2.0V$		1000	ns
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA	$V_{CC} = 4.5V$		500	ns
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	$V_{CC} = 6.0V$		400	ns
Power Dissipation ( $P_D$ )		<b>Note 1:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.			
(Note 3)	600 mW	<b>Note 2:</b> Unless otherwise specified all voltages are referenced to ground.			
S.O. Package only	500 mW	<b>Note 3:</b> Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.			
Lead Temperature ( $T_L$ )					
(Soldering 10 seconds)	260°C				

### DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			$T_A = -40 \text{ to } 85^\circ C$			Units
				Typ			Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V		
			4.5V		3.15	3.15	3.15	V		
			6.0V		4.2	4.2	4.2	V		
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V		
			4.5V		1.35	1.35	1.35	V		
			6.0V		1.8	1.8	1.8	V		
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V		
			4.5V	4.5	4.4	4.4	4.4	V		
			6.0V	6.0	5.9	5.9	5.9	V		
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2	V		
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V		
			4.5V	0	0.1	0.1	0.1	V		
			6.0V	0	0.1	0.1	0.1	V		
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4	V		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC} \text{ or } GND$	6.0V		±0.1	±1.0	±1.0	μA		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC} \text{ or } GND$ $I_{OUT} = 0 \mu A$	6.0V		8	80	160	μA		

**Note 4:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		60	35	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$		15	25	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Reset to Q or $\bar{Q}$		13	21	ns
$t_{REC}$	Minimum Removal Time, Clear to Clock			20	ns
$t_S$	Minimum Setup Time, Data to Clock			20	ns
$t_H$	Minimum Hold Time, Data from Clock			0	ns
$t_W$	Minimum Pulse Width, Clock or Clear		10	16	ns

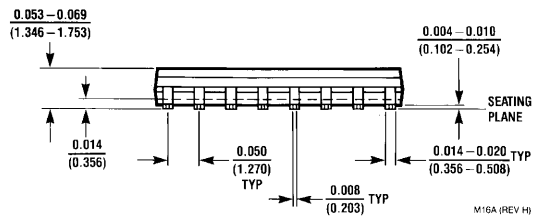
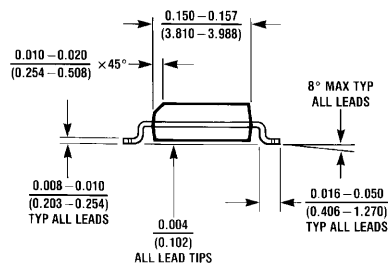
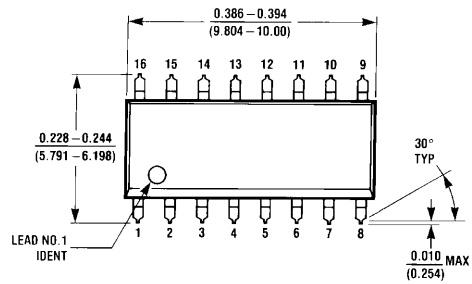
## AC Electrical Characteristics

$V_{CC} = 2.0V$  to  $6.0V$ ,  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  (unless otherwise specified)

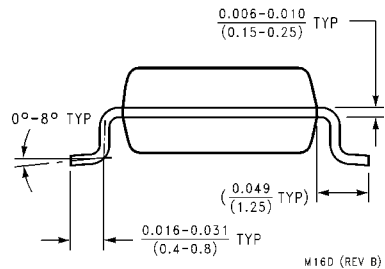
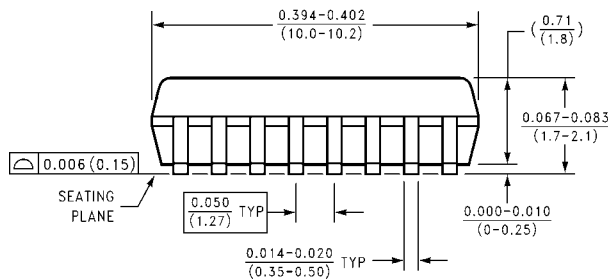
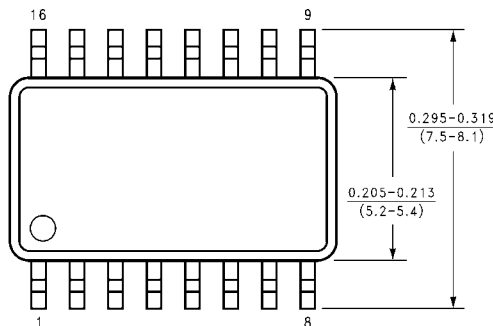
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency		2.0V	12	6	5	4	MHz
			4.5V	60	30	24	20	MHz
			6.0V	70	35	28	24	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$		2.0V	80	150	190	225	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Reset to Q or $\bar{Q}$		2.0V	64	125	158	186	ns
			4.5V	14	25	32	37	ns
			6.0V	12	21	27	32	ns
$t_{REM}$	Minimum Removal Time Clear to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
$t_S$	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
$t_H$	Minimum Hold Time Data from Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
$t_W$	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per package)		150				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

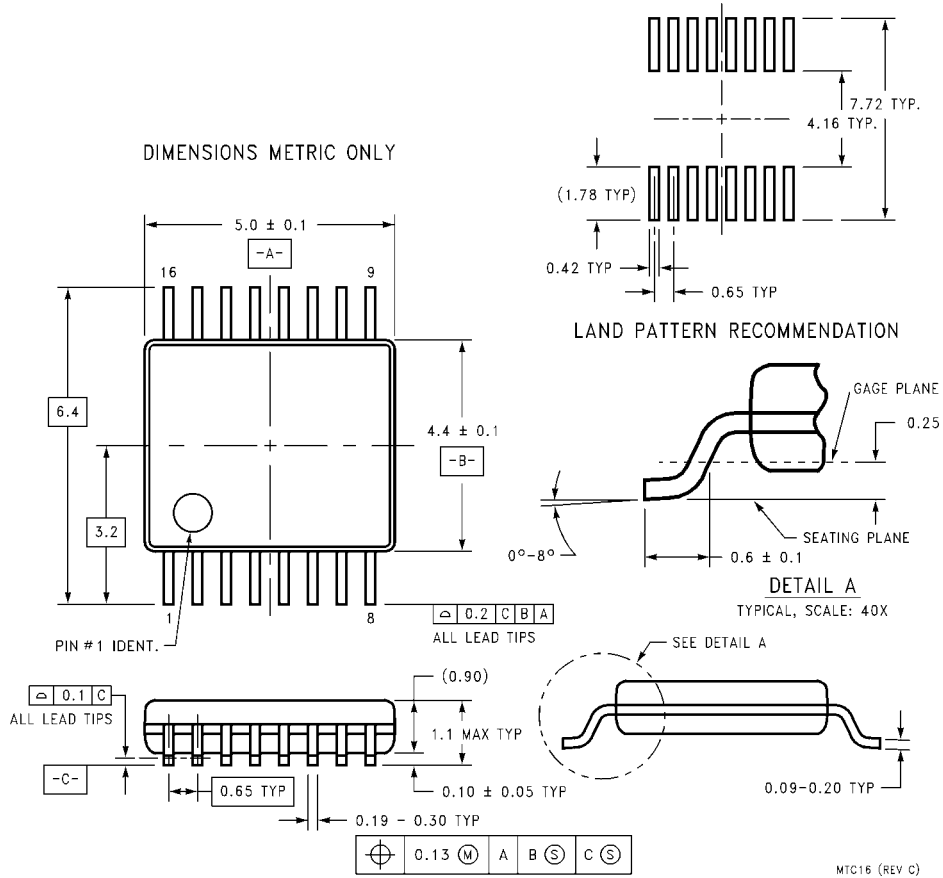


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



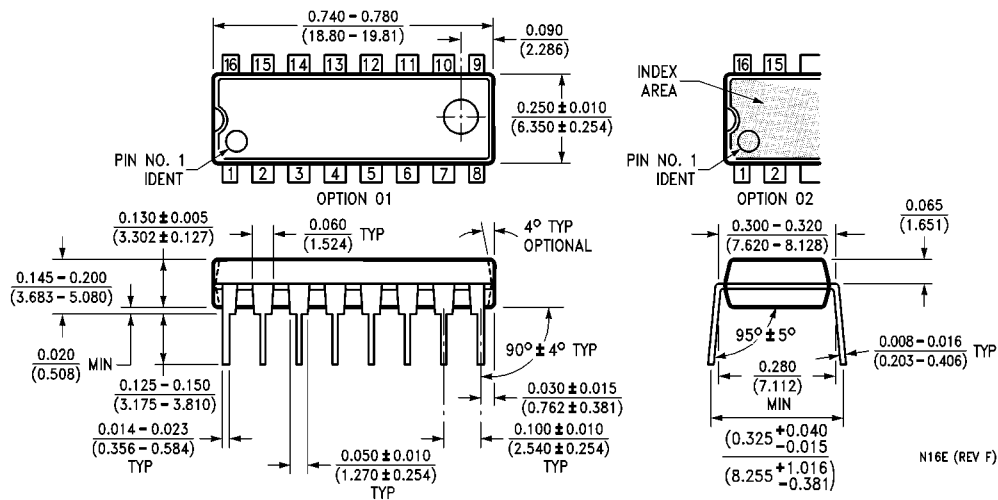
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

MM74HC175 Quad D-Type Flip-Flop With Clear

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