

MM74HC597 8-Bit Shift Registers with Input Latches

General Description

This high speed register utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM74HC597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. the shift register also has direct load (from storage) and clear inputs.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

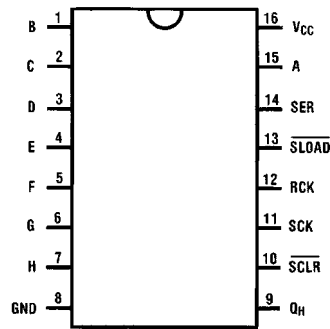
- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load and clear
- Guaranteed shift frequency: DC to 30 MHz
- Low quiescent current: 80 μ A maximum

Ordering Code:

Order Number	Package Number	Package Description
MM74HC597M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
MM74HC597N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

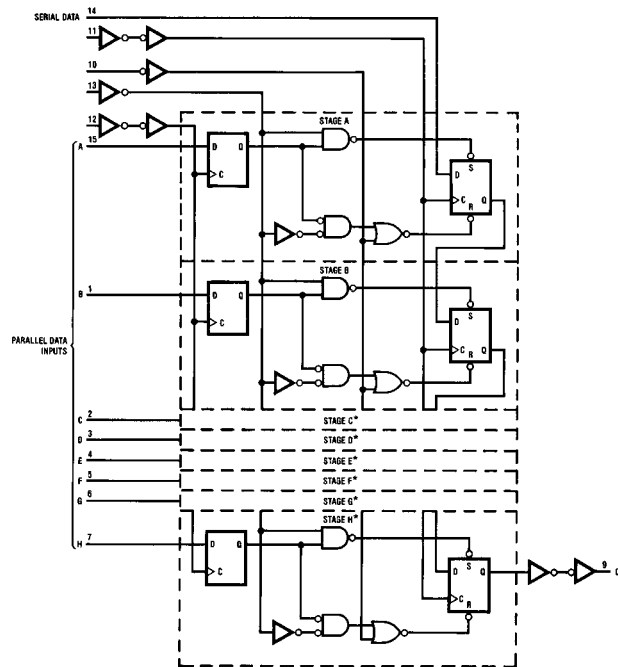


Top View

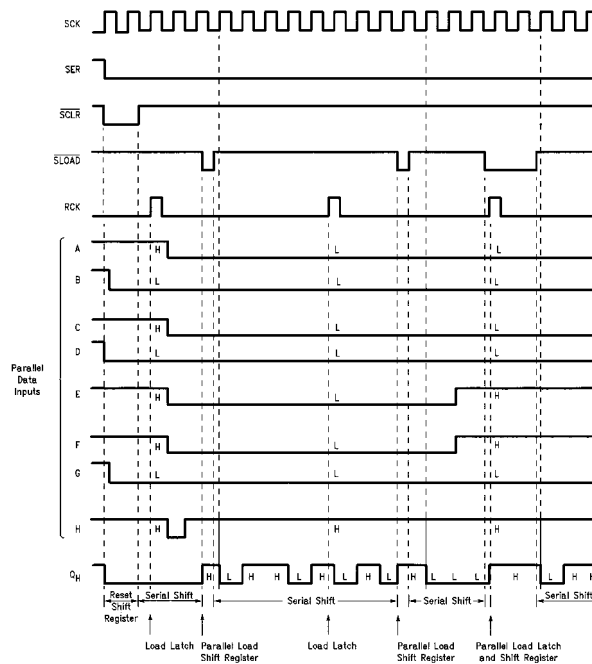
Truth Table

RCK	SCK	SLOAD	SCLR	Function
\uparrow	X	X	X	Data Loaded to input latches
\uparrow	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	\uparrow	H	H	Shift register clocked $Q_n = Q_{n-1}$, $Q_0 = SER$

Functional Block Diagram (Positive Logic)



Timing Diagram



Absolute Maximum Ratings ^(Note 1)				Recommended Operating Conditions				
(Note 2)								
Supply Voltage (V_{CC})		-0.5 to +7.0V		Supply Voltage (V_{CC})	Min	Max	Units	
DC Input Voltage (V_{IN})		-1.5 to $V_{CC}+1.5V$		DC Input or Output Voltage	2	6	V	
DC Output Voltage (V_{OUT})		-0.5 to $V_{CC}+0.5V$		(V_{IN}, V_{OUT})	0	V_{CC}	V	
Clamp Diode Current (I_{IK}, I_{OK})		± 20 mA		Operating Temperature Range (T_A)	-40	+85	$^{\circ}C$	
DC Output Current, per pin (I_{OUT})		± 25 mA		Input Rise or Fall Times				
DC V_{CC} or GND Current, per pin (I_{CC})		± 70 mA		(t_r, t_f) $V_{CC} = 2.0V$		1000	ns	
Storage Temperature Range (T_{STG})		-65 $^{\circ}C$ to +150 $^{\circ}C$		$V_{CC} = 4.5V$		500	ns	
Power Dissipation (P_D)				$V_{CC} = 6.0V$		400	ns	
(Note 3)		600 mW						
S.O. Package only		500 mW						
Lead Temperature (T_L)								
(Soldering 10 seconds)		260 $^{\circ}C$						
<p>Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.</p> <p>Note 2: Unless otherwise specified all voltages are referenced to ground.</p> <p>Note 3: Power Dissipation temperature derating — plastic "N" package: - 12 mW/$^{\circ}C$ from 65$^{\circ}C$ to 85$^{\circ}C$.</p>								
DC Electrical Characteristics (Note 4)								
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^{\circ}C$			Units	
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6.0V		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage (Note 5)		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6.0V		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.2	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA
<p>Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.</p> <p>Note 5: V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY89.</p>								

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL} t_{PLH}	Maximum Propagation Delay from SCK to Q_H		20	30	ns
t_{PHL} t_{PLH}	Maximum Propagation Delay from SLOAD to Q_H		20	30	ns
t_{PHL} t_{PLH}	Maximum propagation Delay from RCK to Q_H	$\overline{SLOAD} = \text{logic "0"}$	25	45	ns
t_{PHL}	Maximum Propagation Delay from SCLR to Q_H		20	30	ns
t_{REM}	Minimum Removal Time, SCLR to SCK		10	20	ns
t_S	Minimum Setup Time from RCK to SCK		30	40	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		-2	0	ns
t_W	Minimum Pulse Width SCK, RCK, SCLR SLOAD		10	16	ns

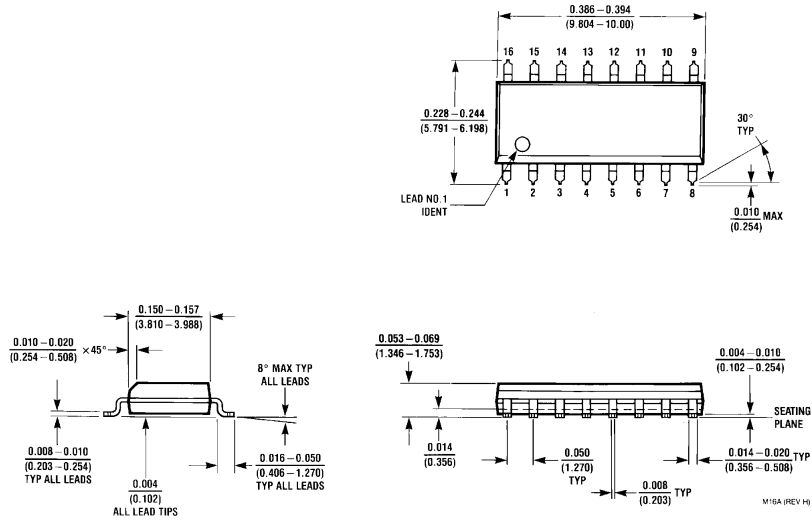
AC Electrical Characteristics $V_{CC} = 2.0\text{--}6.0V, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	Units
				Typ	Guaranteed Limits				
f_{MAX}	Maximum Operating Frequency		2.0V	10	6.0	4.8	4.0	MHz	
			4.5V	45	30	24	20		
			6.0V	50	35	28	24		
t_{PHL} t_{PLH}	Maximum Propagation Delay from SCK to Q_H		2.0V	62	175	220	263	ns	
			4.5V	20	35	44	53		
			6.0V	18	30	38	45		
t_{PHL} t_{PLH}	Maximum Propagation Delay from SLOAD to Q_H		2.0V	65	175	220	263	ns	
			4.5V	20	35	44	53		
			6.0V	18	30	38	45		
t_{PHL} t_{PLH}	Maximum Propagation Delay from RCK to Q_H	SLOAD = Logic "0"	2.0V	120	205	255	310	ns	
			4.5V	30	41	51	62		
			6.0V	28	35	43	53		
t_{PHL}	Maximum Propagation Delay from SCLR to Q_H		2.0V	66	175	220	263	ns	
			4.5V	20	35	44	53		
			6.0V	18	30	38	45		
t_{REM}	Minimum Removal Time SCLR to SCK		2.0V		100	125	150	ns	
			4.5V		20	25	30		
			6.0V		17	21	25		
t_S	Minimum Setup Time from RCK to SCK		2.0V		200	250	300	ns	
			4.5V		40	50	60		
			6.0V		34	42	50		
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns	
			4.5V		20	25	30		
			6.0V		17	21	25		

AC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t _S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	
			6.0V		17	21	25	
t _H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	
			6.0V		0	0	0	
t _W	Minimum Pulse Width SCK, RCK, SCLR, SLOAD		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	
			6.0V	8	14	18	20	
t _r , t _f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	
			6.0V		400	400	400	
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	
			6.0V	8	13	16	19	
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time		2.0V		75	95	110	ns
			4.5V		15	19	22	ns
			6.0V		13	16	19	ns
C _{PD}	Power Dissipation Capacitance, Outputs (Note 6)			87				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance			15	20	20	20	pF

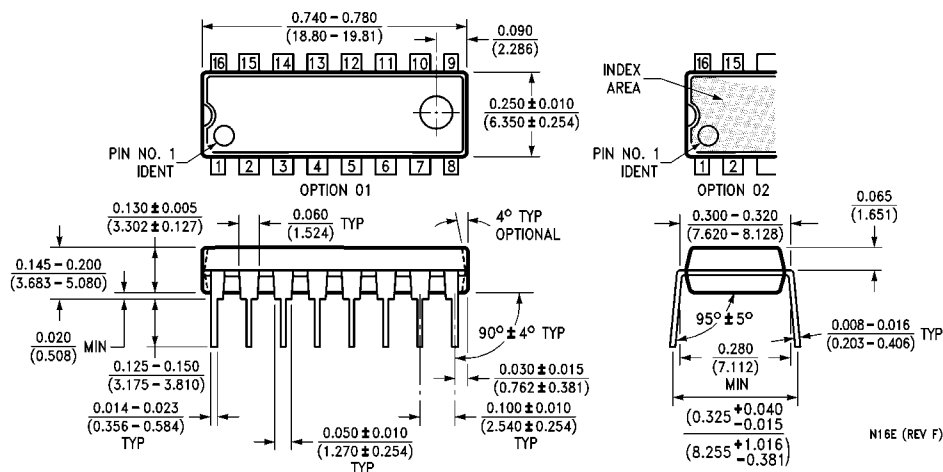
Note 6: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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