

T-39-11

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM12N05
MTP12N05
MTP12N06

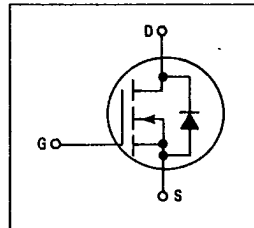
TMOS POWER FETs
12 AMPERES
 $r_{DS(on)} = 0.2 \text{ OHM}$
50 and 60 VOLTS

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS



These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

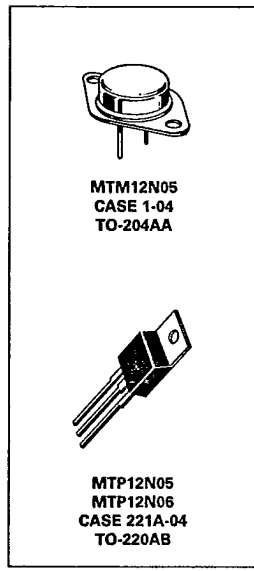


MAXIMUM RATINGS

Rating	Symbol	MTM12N05	MTP12N05 MTP12N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS} V_{GSM}	± 20 ± 40		Vdc Vpk
Drain Current Continuous Pulsed	I_D I_{DM}	12 30		A dc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient	$R_{\theta JA}$	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MOTOROLA TMOS POWER MOSFET DATA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	MTM/MTP12N05 MTP12N06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)		I_{DSS}	—	10 100	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)		I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 6 \text{ Adc}$)		$r_{DS(on)}$	—	0.2	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 12 \text{ Adc}$) ($I_D = 6 \text{ Adc}, T_J = 100^\circ\text{C}$)		$V_{DS(on)}$	—	3 2.8	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 6 \text{ A}$)		g_{FS}	4	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$) See Figure 11	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	100	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms}$) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	160	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	110	
Total Gate Charge	($V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V}$) See Figure 12	Q_g	13 (Typ)	26	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	($I_S = \text{Rated } I_D$ $V_{GS} = 0$)	V_{SD}	1.8 (Typ)	3.2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

MOTOROLA TMOS POWER MOSFET DATA

3-484

TYPICAL ELECTRICAL CHARACTERISTICS

T-39-11

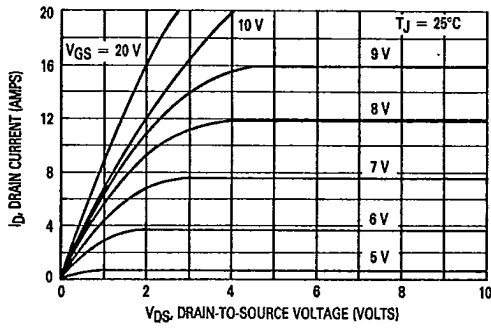


Figure 1. On-Region Characteristics

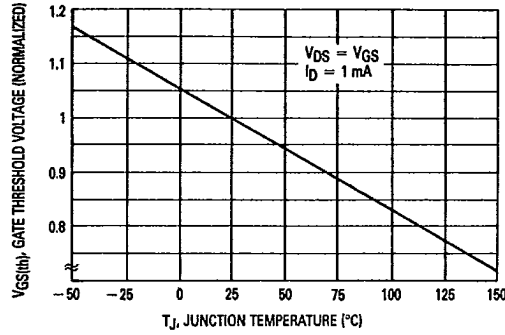


Figure 2. Gate-Threshold Voltage Variation With Temperature

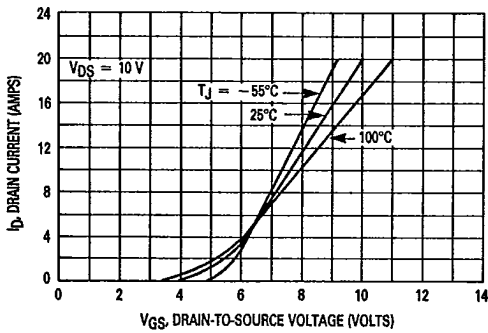


Figure 3. Transfer Characteristics

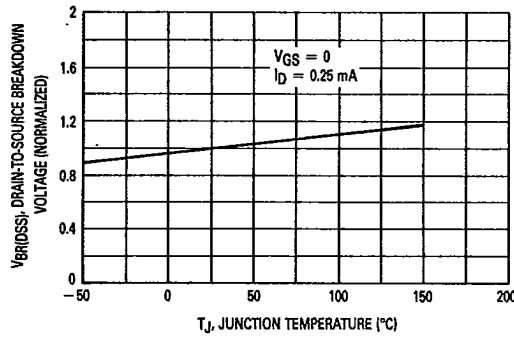


Figure 4. Breakdown Voltage Variation With Temperature

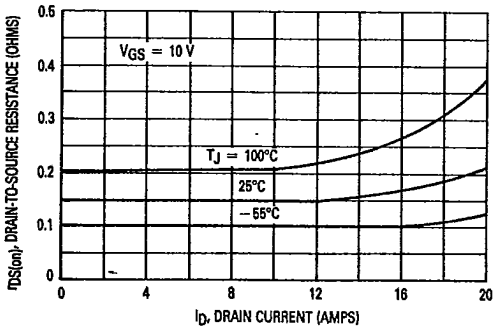


Figure 5. On-Resistance versus Drain Current

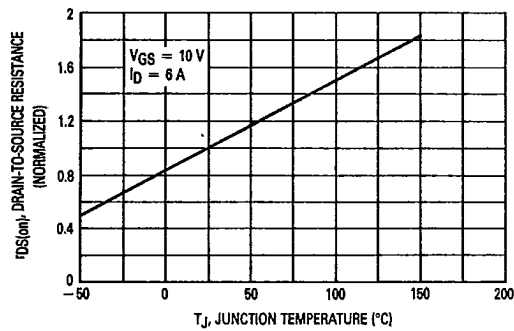


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

T-39-11

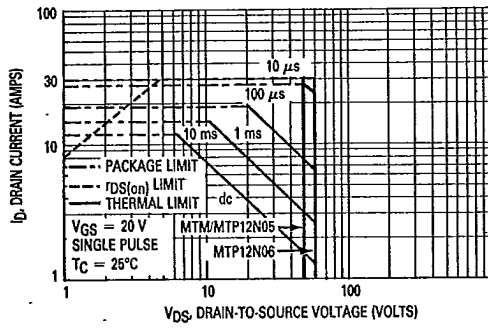


Figure 7. Maximum Rated Forward Biased Safe Operating Area

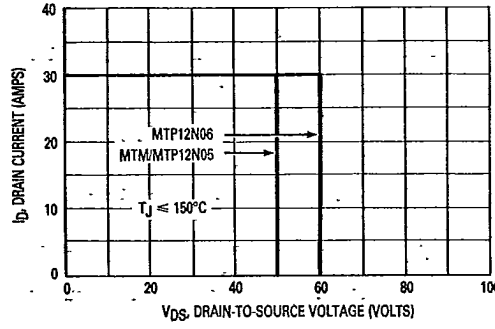


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

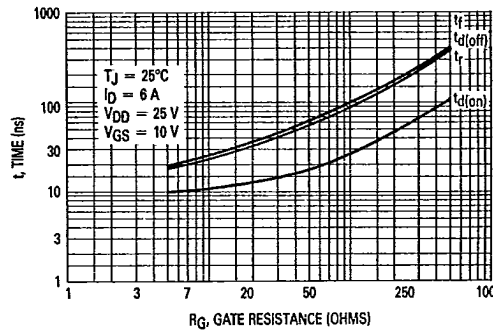


Figure 9. Resistive Switching Time Variation versus Gate Resistance

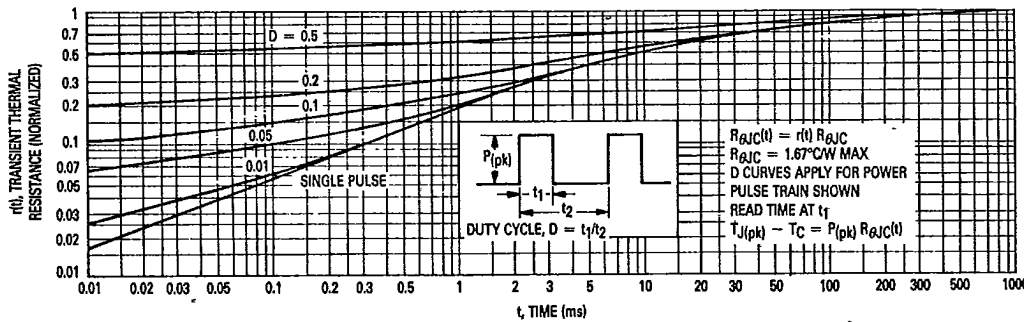


Figure 10. Thermal Response

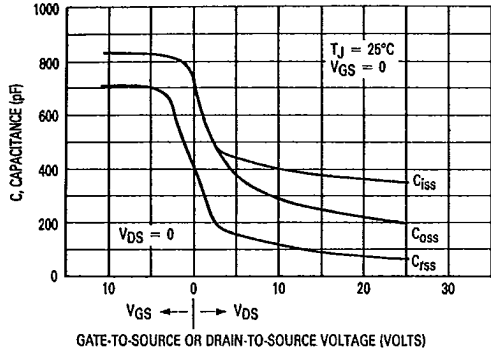


Figure 11. Capacitance Variation

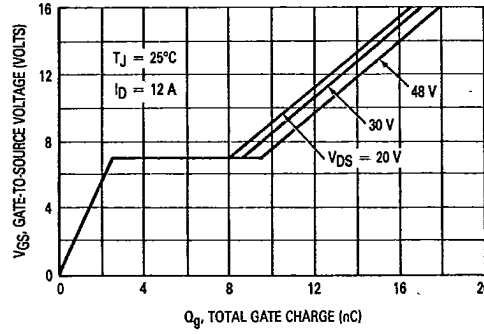


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

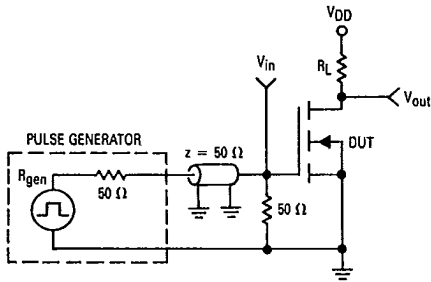


Figure 13. Switching Test Circuit

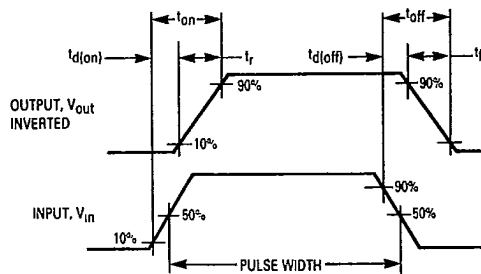


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-04 TO-204AA

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	29.27	—	1.150
B	—	21.06	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30 15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.83 BSC		0.665 BSC	
K	11.18	12.13	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
 1. DIAMETER V AND SURFACE WARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 + $\phi 0.25 (0.010)$ (M) (W) (V) (Q)
 3. POSITIONAL TOLERANCE FOR LEADS:
 + $\phi 0.30 (0.012)$ (M) (W) (V) (Q) (Q)

STYLE 3:
 PIN 1, GATE
 2, SOURCE
 CASE DRAIN

CASE 221A-04 TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.08	12.78	0.358	0.503
C	4.07	4.82	0.160	0.190
D	0.54	0.86	0.021	0.034
F	3.81	3.73	0.150	0.147
G	2.44	2.68	0.096	0.106
H	7.80	3.83	0.311	0.151
J	0.38	0.59	0.014	0.023
K	12.75	14.17	0.500	0.557
L	1.15	1.36	0.045	0.054
N	4.83	5.33	0.190	0.211
Q	2.54	3.04	0.100	0.120
R	2.04	1.78	0.080	0.070
S	1.15	1.30	0.045	0.051
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	7.34	—	0.289

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z REFERS TO ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 8:
 PIN 1, GATE
 2, DRAIN
 3, SOURCE
 4, DRAIN