MOTOROLA

MTM10N25
MTP10N25

Designer's Data Sheet

10 AMPERE

N-CHANNEL TMOS POWER FET

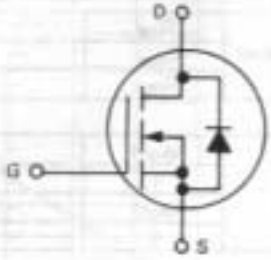
$r_{DS(on)}$ = 0.45 OHM
250 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

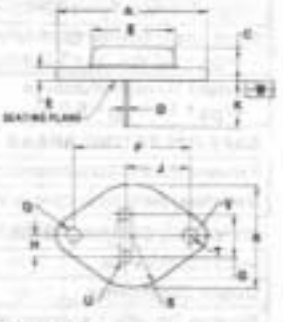
These TMOS Power FETs are designed for 120 V line operated high speed power switching applications such as motor controls, switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

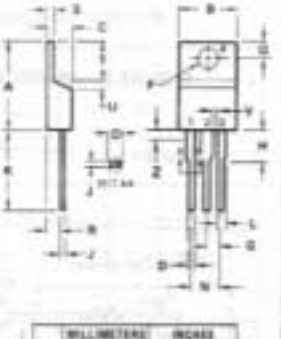


MTM10N25



CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP10N25



CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM10N25 MTP10N25	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate - Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 30	Adc
Gate Current — Pulsed	I_{GM}	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM10N25/MTP10N25	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
T_J = 100°C			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5.0 Adc)		$V_{DS(on)}$	—	2.25	Vdc
(I_D = 10 Adc)			—	5.60	
(I_D = 5.0 Adc, T_J = 100°C)			—	4.50	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$r_{DS(on)}$	—	0.45	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)		g_{fs}	3.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 5.0 A, R_{gen} = 50 ohms) See Figures 1 and 2.	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = 10 A, V_{GS} = 0)	V_{SD}	1.5	Vdc
Forward Turn-On Time		t_{on}	50	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

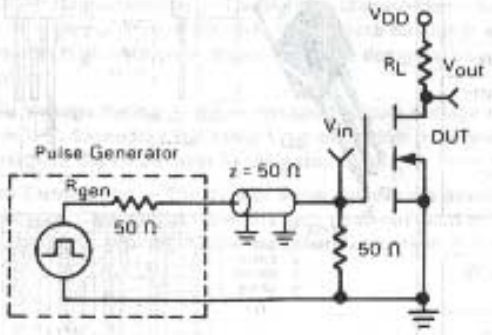
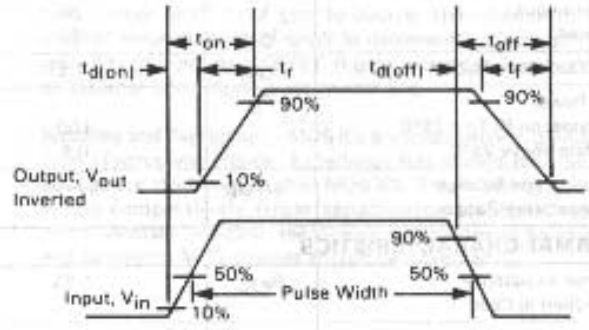


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

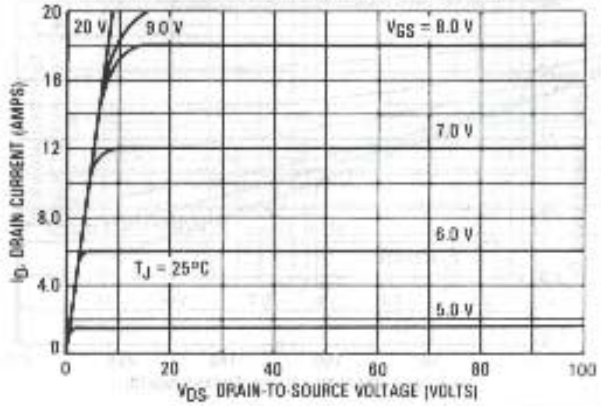


FIGURE 4 — ON-REGION CHARACTERISTICS

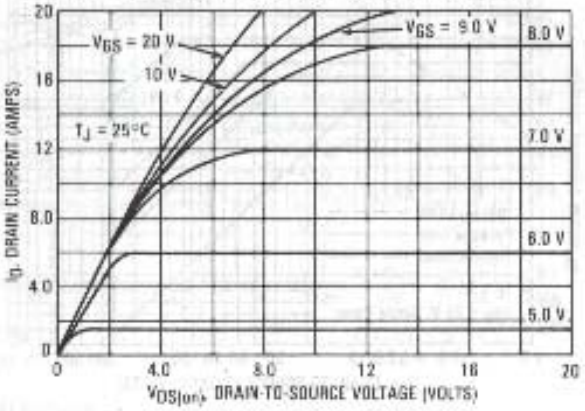


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

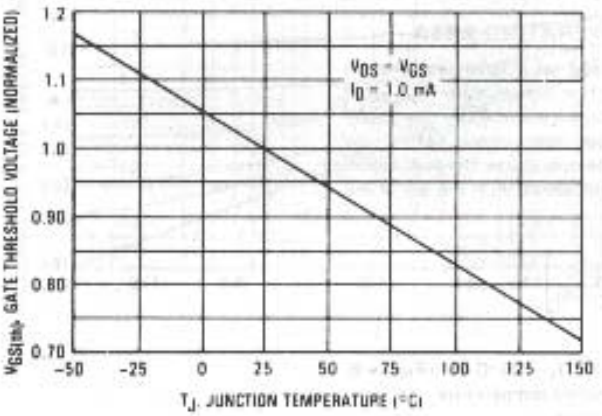


FIGURE 6 — TRANSFER CHARACTERISTICS

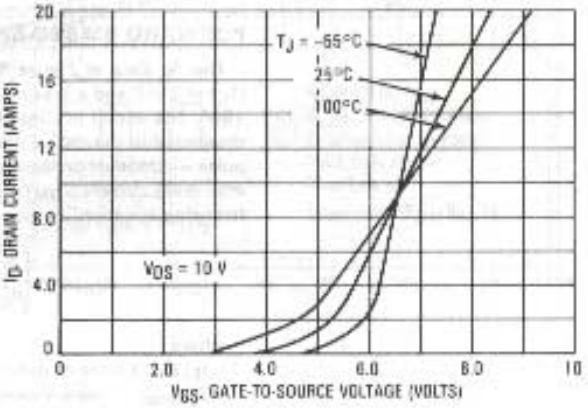


FIGURE 7 — ON RESISTANCE versus DRAIN CURRENT

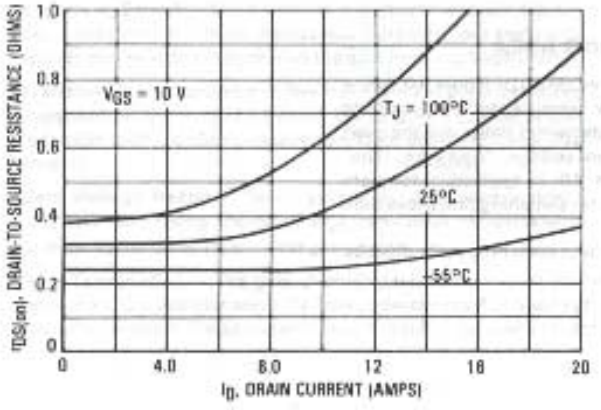
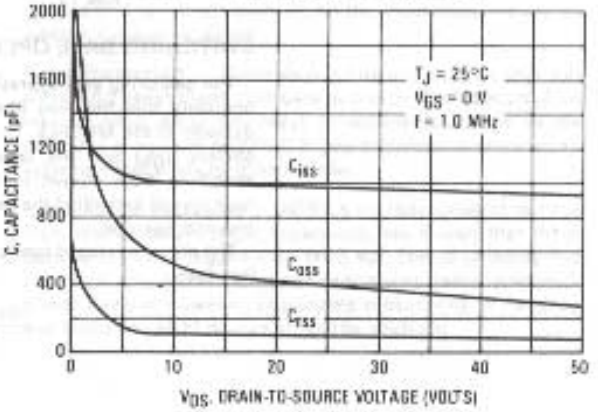


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

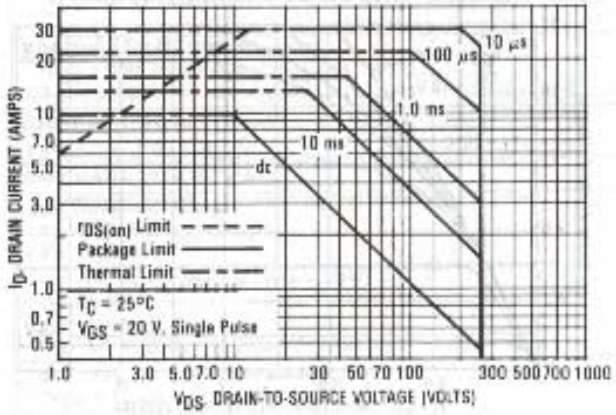
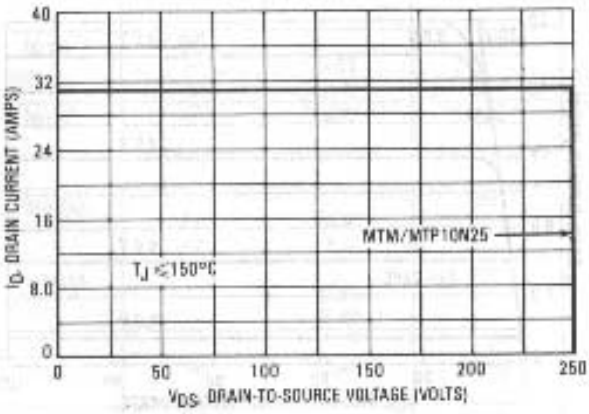


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figures 11 and 12

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL RESPONSE

FIGURE 11 — MTM10N25

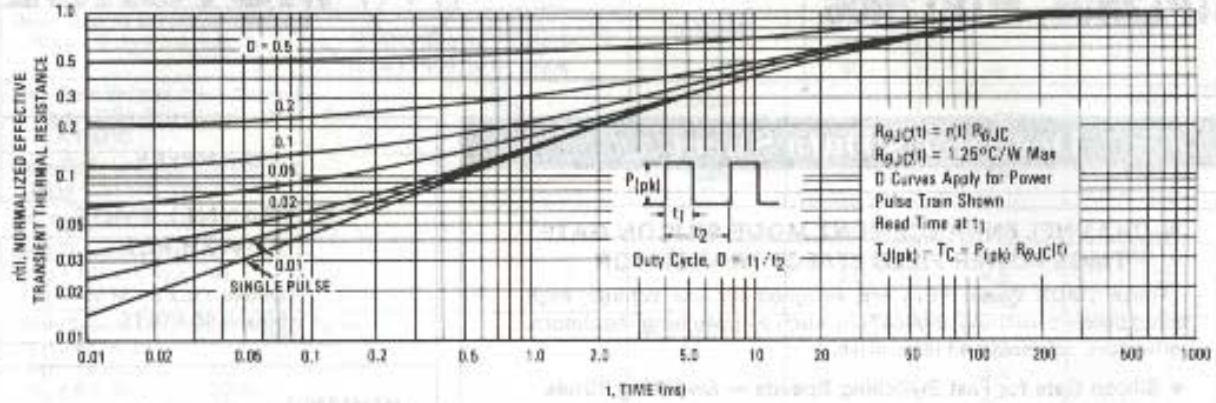
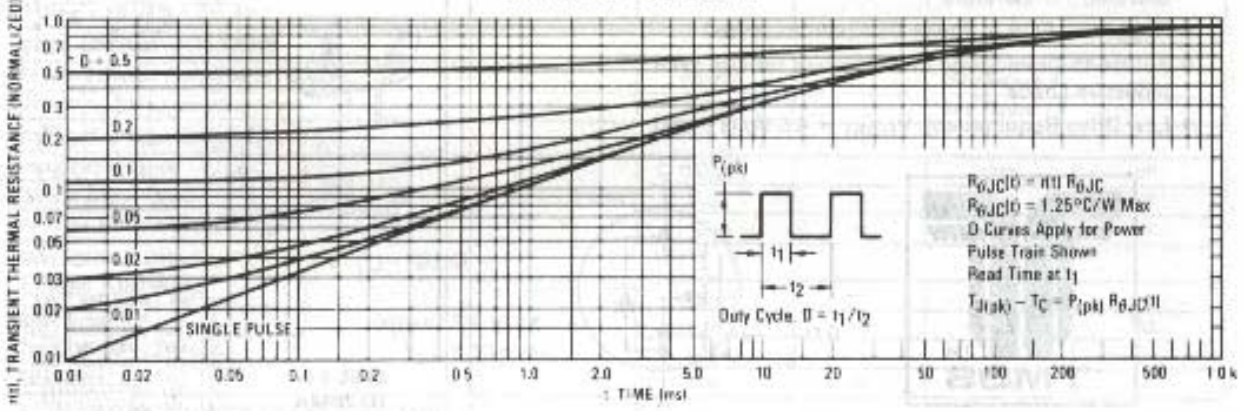


FIGURE 12 — MTP10N25



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 Amps (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.