

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

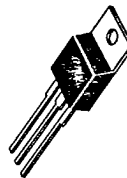
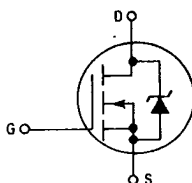
Designer's Data Sheet
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

MTP20N10E

TMOS POWER FET
20 AMPERES
r_{DS(on)} = 0.15 OHM
100 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	100	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	100	Vdc
Gate-Source Voltage — Continuous	V _{GSM}	±20	Vdc
— Non-repetitive (t _p < 50 μs)	V _{GSM}	±40	Vpk
Drain Current — Continuous	I _D	20	Adc
— Pulsed	I _{DM}	60	
Total Power Dissipation (at T _C = 25°C)	PD	100	Watts
Derate above 25°C		0.67	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J ≤ 175°C)

Single Pulse Drain-to-Source Avalanche Energy	W _{DSS} (1)	400	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	W _{DSS} (2)	100	
	W _{DSR} (3)	10	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _{θJC}	1.5	°C/W
— Junction to Ambient	R _{θJA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

(1) V_{DD} = 25 V, I_D = 20 A, L = 1.5 mH, Initial T_C = 25°C
 (2) V_{DD} = 25 V, I_D = 20 A, L = 380 μH, Initial T_C = 100°C
 (3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design. TMOS and Designer's are trademarks of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V(BR)DSS	100	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)	I _{DSS}	—	10 80	μA
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	I _{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 10 Adc)	r _{DS(on)}	—	0.15	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 20 Adc) (I _D = 10 Adc, T _J = 100°C)	V _{DS(on)}	—	3.6 3	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 10 A)	g _{FS}	6	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 16	C _{iss}	—	1600	pF
Output Capacitance		C _{oss}	—	600	
Reverse Transfer Capacitance		C _{rss}	—	200	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figure 9	t _{d(on)}	—	50	ns
Rise Time		t _r	—	450	
Turn-Off Delay Time		t _{d(off)}	—	100	
Fall Time		t _f	—	200	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figures 17 and 18	Q _g	28 (Typ)	50	nC
Gate-Source Charge		Q _{gs}	15 (Typ)	—	
Gate-Drain Charge		Q _{gd}	13 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I _S = Rated I _D V _{GS} = 0)	V _{SD}	1.4 (Typ)	1.9	Vdc
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	300 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

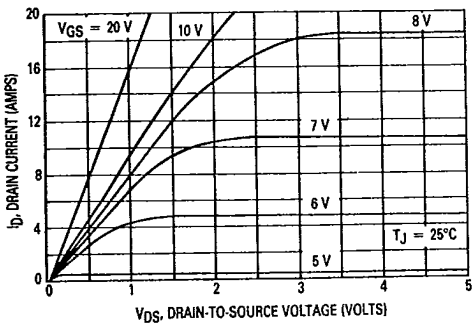


Figure 2. Gate-Threshold Voltage Variation With Temperature

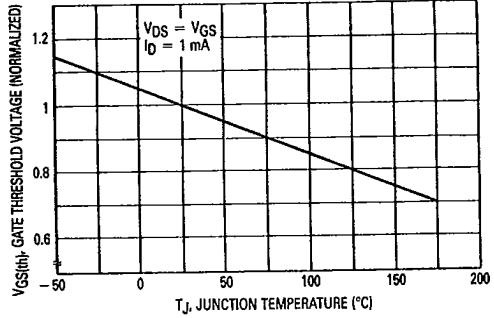


Figure 3. Transfer Characteristics

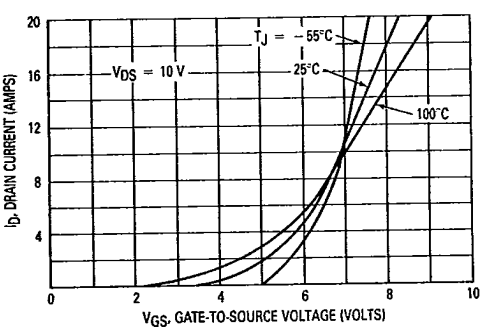


Figure 4. Breakdown Voltage Variation With Temperature

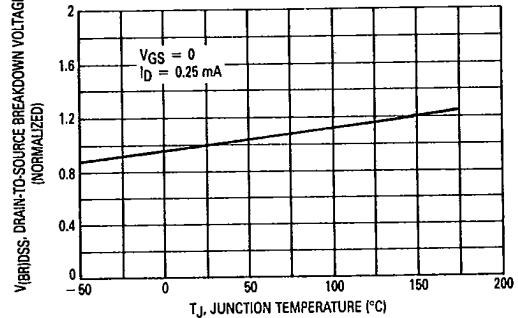


Figure 5. On-Resistance versus Drain Current

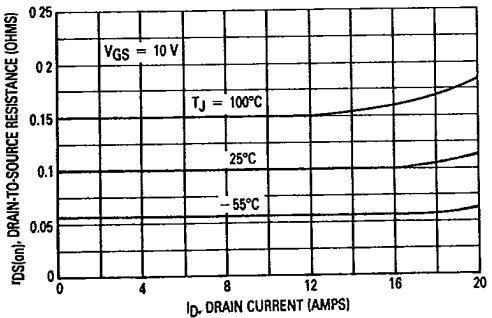
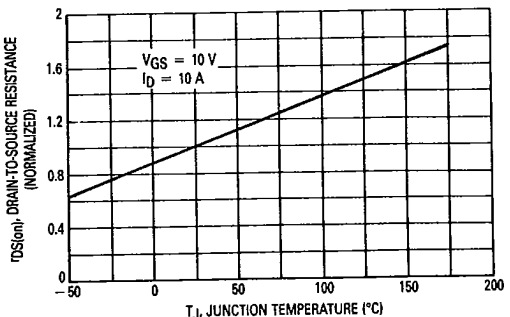
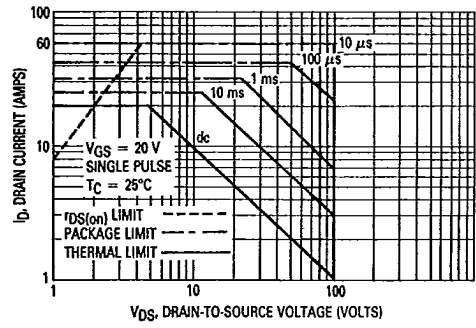


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area



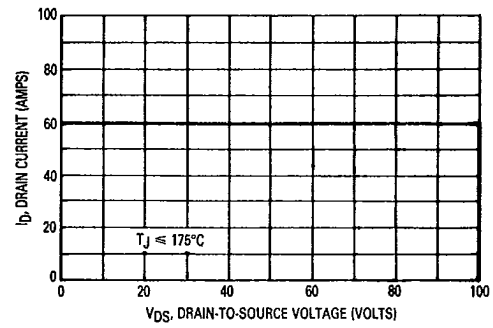
FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

Figure 8. Maximum Rated Switching Safe Operating Area



The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(\max) - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

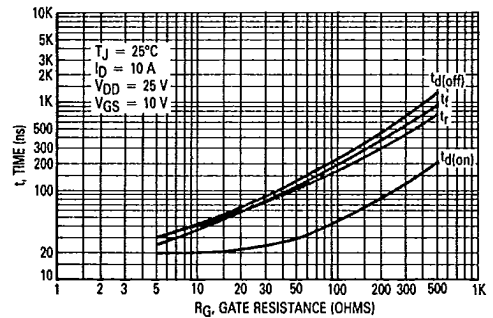
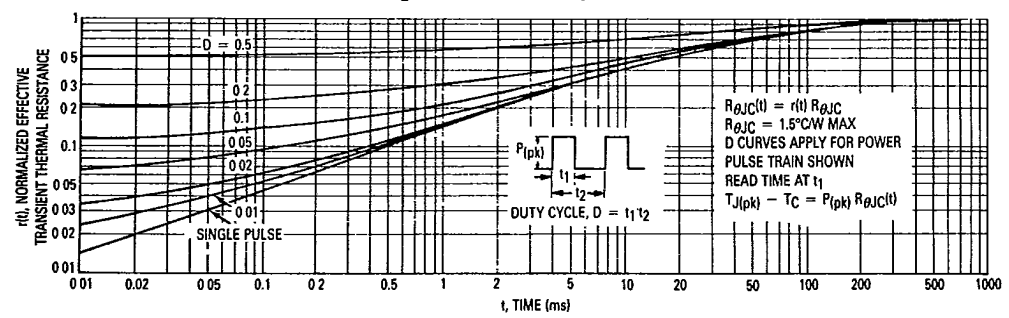


Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM} , peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{frr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

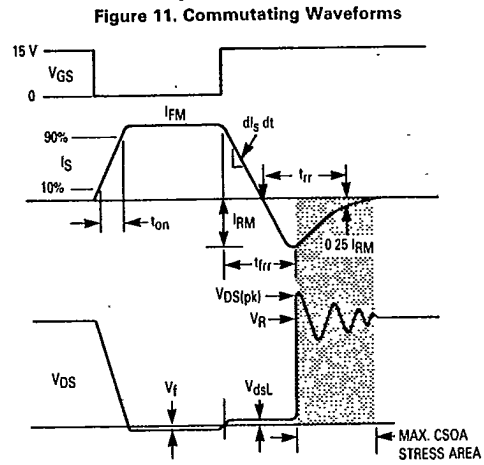


Figure 11. Commutating Waveforms

Figure 12. Commutating Safe Operating Area (CSOA)

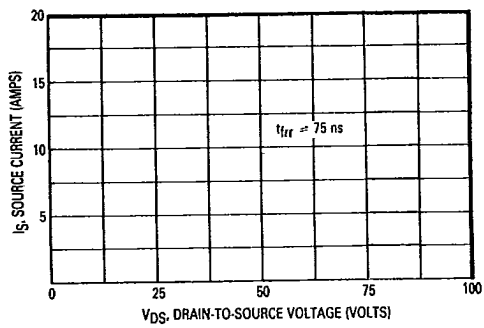


Figure 14. Unclamped Inductive Switching Test Circuit

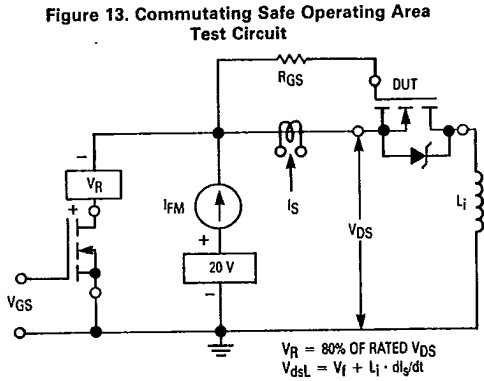
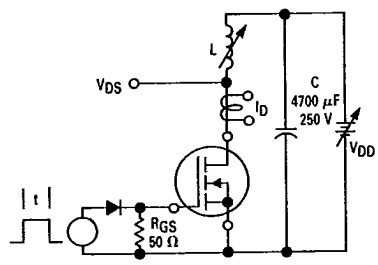


Figure 13. Commutating Safe Operating Area Test Circuit

Figure 15. Unclamped Inductive Switching Waveforms

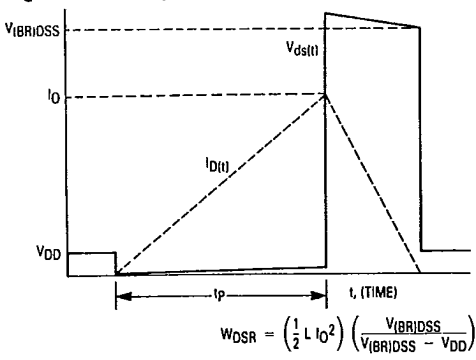


Figure 16. Capacitance Variation

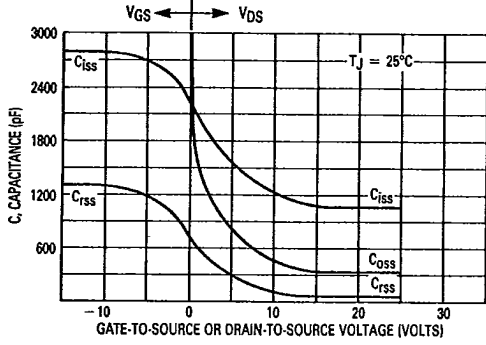


Figure 17. Gate Charge versus Gate-to-Source Voltage

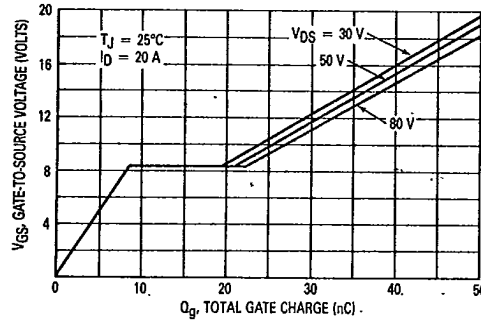
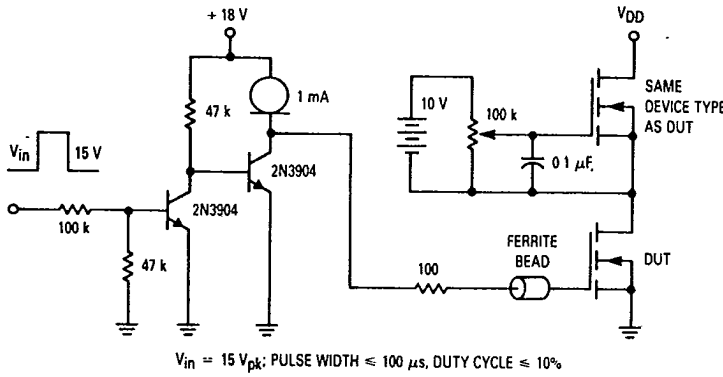


Figure 18. Gate Charge Test Circuit



OUTLINE DIMENSIONS

STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.43	15.75	0.570	0.620
B	9.58	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.38	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.80	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB