MOTOROLA

MTP4N08, MTP5N05
MTP4N10, MTP5N06

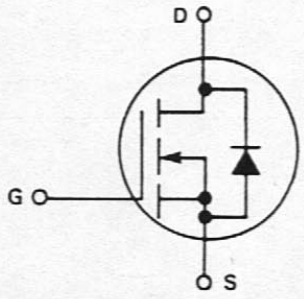
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

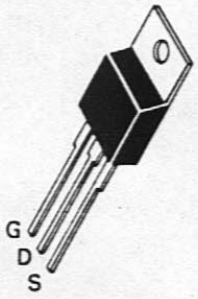


4.0 and 5.0 AMPERE

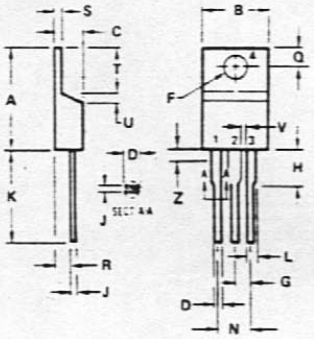
N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.8 OHM
80 and 100 VOLTS

$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS



MTP4N08
MTP4N10
MTP5N05
MTP5N06



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 5N05	MTP 5N06	MTP 4N08	MTP 4N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 5.0 10		 4.0 9.0		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTP5N05	$V_{(BR)DSS}$	50	—	Vdc
	MTP5N06		60	—	
	MTP4N08		80	—	
	MTP4N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTP5N05, MTP5N06	$r_{DS(on)}$	—	0.6	Ohms
(V_{GS} = 10 Vdc, I_D = 2.0 Adc)	MTP4N08/MTP4N10		—	0.8	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 5.0 Adc)	MTP5N05/MTP5N06		—	3.75	
(I_D = 2.5 Adc, T_J = 100°C)			—	3.0	
(I_D = 4.0 Adc)	MTP4N08, MTP4N10		—	4.8	
(I_D = 2.0 Adc, T_J = 100°C)			—	3.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	MTP5N05/MTP5N06	g_{fs}	0.75	—	mhos
(V_{DS} = 15 V, I_D = 2.0 A)	MTP4N08/MTP4N10		0.75	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	300	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	250	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	60	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	30	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0,	V_{SD}	2.5	Vdc
Forward Turn-On Time		t_{on}	150	ns
Reverse Recovery Time		t_{rr}	250	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

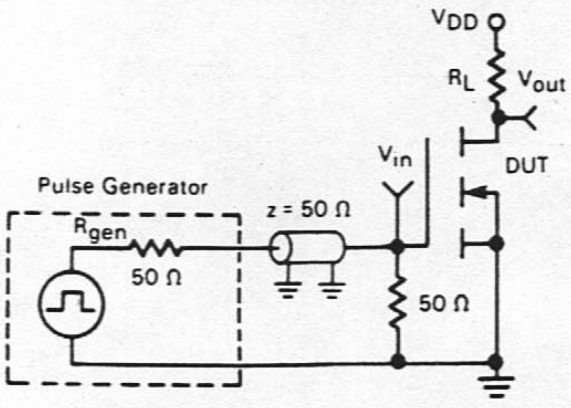


FIGURE 2 — SWITCHING WAVEFORMS