

# NC7SZ374

## TinyLogic™ UHS D-Type Flip-Flop with 3-STATE Output

### General Description

The NC7SZ374 is a single positive edge-triggered D-type CMOS Flip-Flop with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic™ in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad  $V_{CC}$  operating range. The device is specified to operate over the 1.8V–5.5V  $V_{CC}$  range. The inputs and output are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 7V independent of  $V_{CC}$  operating voltage. This single flip-flop will store the state of the D input that meets the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition.

The output tolerates voltages above  $V_{CC}$  in the 3-STATE condition.

### Features

- Space saving SC70 6-lead package
- Ultra High Speed;  $t_{PD}$  2.6 ns Typ into 50 pF at 5V  $V_{CC}$
- High Output Drive;  $\pm 24$  mA at 3V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V  $V_{CC}$
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V – 3V translation

### Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7SZ374P6	MAA06A	Z74	6-Lead SC70, EIAJ SC88, 1.25mm Wide	250 Units on Tape and Reel
NC7SZ374P6X	MAA06A	Z74	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

### Pin Descriptions

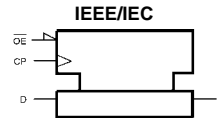
Pin Names	Description
D	Data Input
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
Q	Flip-Flop Output

### Function Table

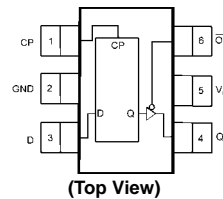
Inputs			Output
CP	D	$\overline{OE}$	Q
⎓	L	L	L
⎓	H	L	H
⎓	X	L	$Q_n$
X	X	H	Z

H = HIGH Logic Level      Z = High Impedance      X = Immaterial  
L = LOW Logic Level       $Q_n$  = No change in data

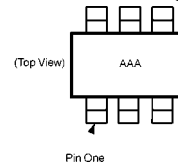
### Logic Symbol



### Connection Diagrams



### Pin One Orientation Diagram



AAA represents Package Top Mark - see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top package mark left to right, Pin One is the lower left pin (see diagram).

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**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_{IN} < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_{OUT} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Source/Sink Current	$\pm 50$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}/I_{GND}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature under Bias ( $T_J$ )	150°C
Junction Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C
Power Dissipation ( $P_D$ ) @ +85°C	180 mW

**Recommended Operating Conditions**

Power Supply	
Operating ( $V_{CC}$ )	1.8V to 5.5V
Data Retention	1.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	
Active State	0V to $V_{CC}$
3-STATE	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 to 10 ns/V
$V_{CC} = 5.5V \pm 0.5V$	0 to 5 ns/V
Operating Temperature ( $T_A$ )	-40°C to +85°C
Thermal Resistance ( $\theta_{JA}$ )	350° C/W

**Note 1:** Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Control Input Voltage	1.8	0.75 $V_{CC}$		0.75 $V_{CC}$		V		
		2.3 to 5.5	0.75 $V_{CC}$		0.7 $V_{CC}$				
$V_{IL}$	LOW Level Control Input Voltage	1.8	0.25 $V_{CC}$		0.25 $V_{CC}$		V		
		2.3 to 5.5	0.3 $V_{CC}$		0.3 $V_{CC}$				
$V_{OH}$	HIGH Level Control Output Voltage	1.8	1.7	1.8	1.7		V	$V_{IN} = V_{IH}$	$I_{OH} = -100 \mu A$
		2.3	2.2	2.3	2.2				
		3.0	2.9	3.0	2.9				
		4.5	4.4	4.5	4.4				
		2.3	1.9	2.15	1.9				$I_{OH} = -8 \text{ mA}$ $I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$
		3.0	2.4	2.8	2.4				
		3.0	2.3	2.68	2.3				
		4.5	3.8	4.2	3.8				
$V_{OL}$	LOW Level Control Output Voltage	1.8	0.0		0.1		V	$V_{IN} = V_{IH}$	$I_{OL} = 100 \mu A$
		2.3	0.0		0.1				
		3.0	0.0		0.1				
		4.5	0.0		0.1				
		2.3	0.10		0.3				$I_{OL} = 8 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$
		3.0	0.15		0.4				
		3.0	0.22		0.55				
		4.5	0.22		0.55				
$I_{IN}$	Input Leakage Current	0 to 5.5			$\pm 0.1$		$\mu A$	$0 \leq V_{IN} \leq 5.5V$	
$I_{OZ}$	3-STATE Output Leakage	1.8 to 5.5			$\pm 0.5$		$\mu A$	$V_{IN} = V_{IL}$ or $V_{IH}$ $0 \leq V_{OUT} \leq 5.5V$	
$I_{OFF}$	Power Off Leakage Current	0.0			1.0		$\mu A$	$V_{IN}$ or $V_{OUT} = 5.5V$	
$I_{CC}$	Quiescent Supply Current	1.8 to 5.5			1.0		$\mu A$	$V_{IN} = 5.5V, GND$	

AC Electrical Characteristics										
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
f <sub>MAX</sub>	Maximum Clock Frequency	1.8				100		MHz	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω, S <sub>1</sub> = Open	Figure 1
		2.5 ± 0.2				125				Figure 3
		3.3 ± 0.3				150				
		5.0 ± 0.5				175				
t <sub>PLH</sub>	Propagation Delay CP to Q	1.8	2.5	6.5	10.0	2.5	11.0	ns	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	Figure 1
		2.5 ± 0.2	2.0	3.8	6.5	2.0	7.0			Figure 3
t <sub>PHL</sub>	CP to Q	3.3 ± 0.3	1.5	2.8	4.5	1.4	5.0	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	Figure 1
		5.0 ± 0.5	1.0	2.2	3.5	1.0	3.8			Figure 3
		3.3 ± 0.3	2.0	3.4	5.5	1.6	6.2			
		5.0 ± 0.5	1.5	2.6	4.0	1.4	4.7			
t <sub>PZL</sub>	Output Enable Time	1.8	2.0	6.0	9.0	2.0	9.5	ns	C <sub>L</sub> = 50 pF, V <sub>I</sub> = 2x V <sub>CC</sub> R <sub>U</sub> , R <sub>D</sub> = 500 Ω S <sub>1</sub> = GND for t <sub>PZH</sub> S <sub>1</sub> = V <sub>I</sub> for t <sub>PZL</sub>	Figure 1
		2.5 ± 0.2	2.0	3.7	6.0	1.8	6.6			Figure 4
		3.3 ± 0.3	1.5	2.8	5.0	1.4	5.3			
		5.0 ± 0.5	1.0	2.2	3.7	1.0	3.9			
t <sub>PLZ</sub>	Output Disable Time	1.8	2.0	5.1	8.0	2.0	8.5	ns	C <sub>L</sub> = 50 pF, V <sub>I</sub> = 2x V <sub>CC</sub> R <sub>U</sub> , R <sub>D</sub> = 500 Ω S <sub>1</sub> = GND for t <sub>PHZ</sub> S <sub>1</sub> = V <sub>I</sub> for t <sub>PLZ</sub>	Figure 1
		2.5 ± 0.2	2.0	3.5	6.0	1.8	6.3			Figure 4
		3.3 ± 0.3	1.5	2.8	4.5	1.4	4.7			
		5.0 ± 0.5	1.0	2.3	3.7	1.0	3.9			
t <sub>S</sub>	Setup Time, CP to D	2.5 ± 0.2				2.5		ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	Figure 1
		3.3 ± 0.3				2.0				Figure 5
		5.0 ± 0.5				1.5				
t <sub>H</sub>	Hold Time, CP to D	2.5 ± 0.2				1.5		ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	Figure 1
		3.3 ± 0.3				1.5				Figure 5
		5.0 ± 0.5				1.5				
t <sub>W</sub>	Pulse Width, CP	2.5 ± 0.2				3.0		ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	Figure 1
		3.3 ± 0.3				2.8				Figure 5
		5.0 ± 0.5				2.5				

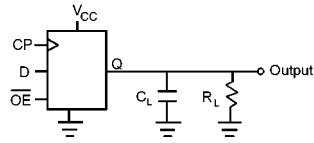
  

Capacitance (Note 2)					
Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Input Capacitance	3		pF	V <sub>CC</sub> = Open, V <sub>IN</sub> 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	4		pF	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance (Note 3)	10		pF	V <sub>CC</sub> = 3.3V
		12		pF	V <sub>CC</sub> = 5.0V

**Note 2:** T<sub>A</sub> = +25°C, f = 1MHz.

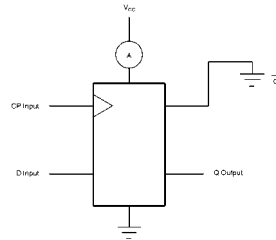
**Note 3:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:  
I<sub>CCD</sub> = (C<sub>PD</sub>) (V<sub>CC</sub>) (f<sub>IN</sub>) + (I<sub>CC</sub>static).

## AC Loading and Waveforms



$C_L$  includes load and stray capacitance  
 Input PRR = 1.0 MHz;  $t_w = 500$  ns

FIGURE 1. AC Test Circuit



CP Input = AC Waveform;  $t_r = t_f = 1.8$  ns;  
 CP Input PRR = 10 MHz; Duty Cycle = 50%  
 D Input PRR = 5MHz; Duty Cycle = 50%

FIGURE 2.  $I_{CCD}$  Test Circuit

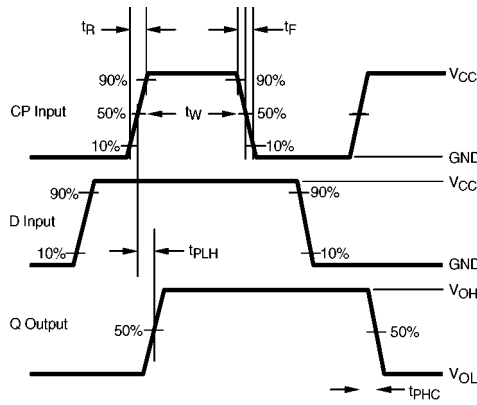


FIGURE 3. AC Waveforms

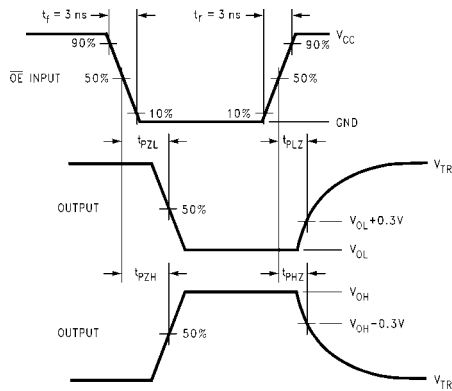


FIGURE 4. AC Waveforms

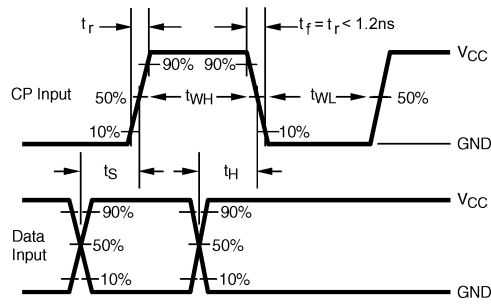


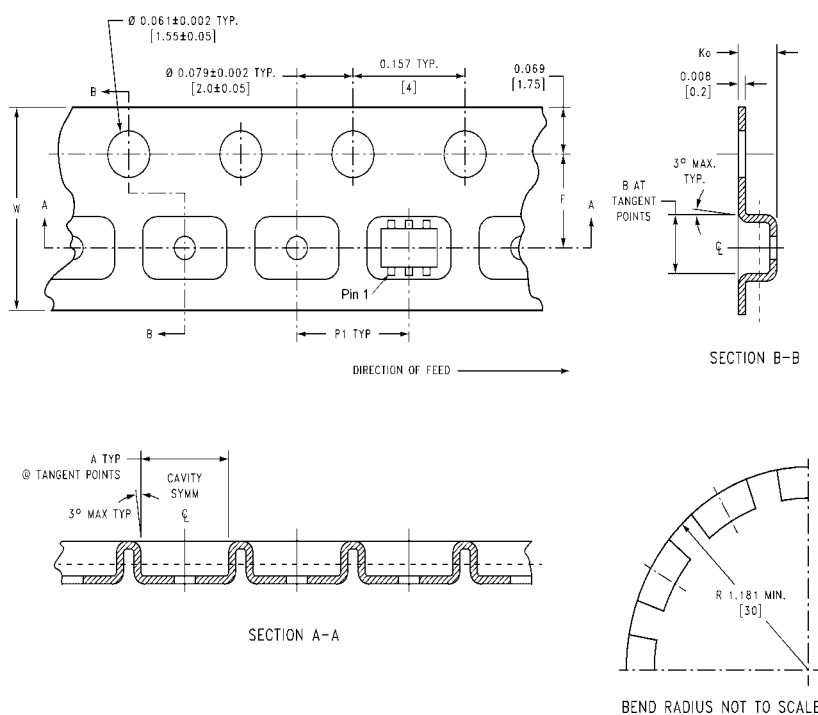
FIGURE 5. AC Waveforms

## Tape and Reel Specification

### TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

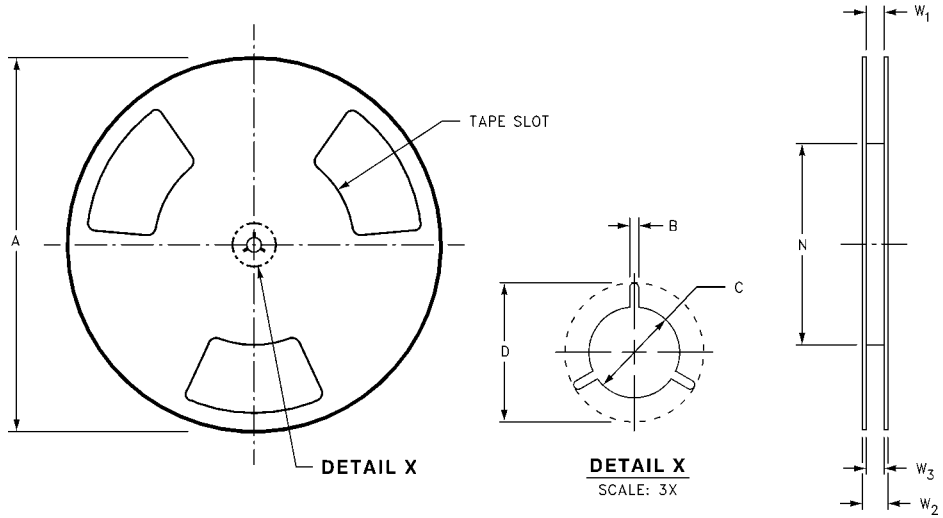
### TAPE DIMENSIONS inches (millimeters)



Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>0</sub>	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

NC7SZ374

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	$0.331 + 0.059/-0.000$ ( $8.40 + 1.50/-0.00$ )	0.567 (14.40)	$W1 + 0.078/-0.039$ ( $W1 + 2.00/-1.00$ )

