



September 1999
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NC7WZ38

TinyLogic™ UHS Dual 2-Input NAND Gate (Open Drain Output) (Preliminary)

General Description

The NC7WZ38 is a dual 2-Input NAND Gate with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. The open drain output stage will tolerate voltages up to 7V independent of V_{CC} when in the high impedance state.

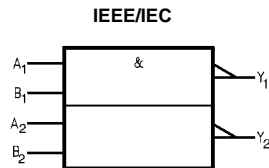
Features

- Space saving US8 8-lead package
- Open Drain output stage for OR tied applications
- Ultra High Speed; t_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High Output Sink Drive; 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

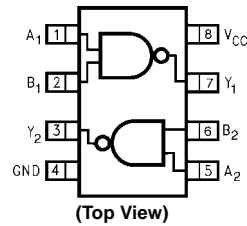
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7WZ38K8X	MAB08A	WZ38	8-Lead US8, 0.7mm x 3.1mm x 2.0 mm	3k Units on Tape and Reel

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
Y_n	Output

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	*H
L	H	*H
H	L	*H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level
*H = HIGH Impedance output state (Open Drain)

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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7V
DC Input Voltage (V_{IN})	-0.5V to +7V
DC Output Voltage (V_{OUT})	-0.5V to +7V
DC Input Diode Current (I_{IK}) @ $V_{IN} < -0.5V$	-50 mA
DC Output Diode Current (I_{OK}) @ $V_{OUT} < -0.5V$	-50 mA
DC Output Current (I_{OUT})	+50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_1); (Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	TBD

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.8V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f) $V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	TBD

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

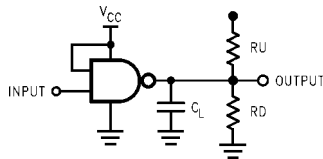
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level	1.8	0.75 V_{CC}		0.75 V_{CC}		V		
	Input Voltage	2.3 to 5.5	0.7 V_{CC}		0.7 V_{CC}				
V_{IL}	LOW Level	1.8	0.25 V_{CC}		0.25 V_{CC}		V		
	Input Voltage	2.3 to 5.5	0.3 V_{CC}		0.3 V_{CC}				
I_{LKG}	HIGH Level	5.5			± 5		μA	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND	
	Output Leakage				± 10				
V_{OL}	LOW Level	1.8	0.0		0.1		V	$V_{IN} = V_{IH}$ $I_{OL} = 100 \mu A$	
		2.3	0.0		0.1				
		3.0	0.0		0.1				
		4.5	0.0		0.1				
	Output Voltage	2.3	0.10		0.3		V	$I_{OL} = 8 mA$ $I_{OL} = 16 mA$ $I_{OL} = 24 mA$ $I_{OL} = 32 mA$	
		3.0	0.15		0.4				
		3.0	0.22		0.55				
		4.5	0.22		0.55				
I_{IN}	Input Leakage Current	5.5	± 0.1		± 1		μA	$V_{IN} = 5.5V, GND$	
I_{OFF}	Power Off Leakage Current	0.0	1		10		μA	V_{IN} or $V_{OUT} = 5.5V$	
I_{CC}	Quiescent Supply Current	5.5	1		10		μA	$V_{IN} = 5.5V, GND$	

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t _{PZL}	Propagation Delay	1.8	1.5		10.5	1.5	11.0	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 × V _{CC}	Figure 1, Figure 3
		2.5 ± 0.2	0.8		7.0	0.8	7.5			
		3.3 ± 0.3	0.8		5.0	0.8	5.2			
		5.0 ± 0.5	0.5		4.3	0.5	4.5			
t _{PLZ}	Propagation Delay	1.8	1.5		10.5	1.5	11.0	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 × V _{CC}	Figure 1, Figure 3
		2.5 ± 0.2	0.8		7.0	0.8	7.5			
		3.3 ± 0.3	0.8		5.0	0.8	5.2			
		5.0 ± 0.5	0.5		4.3	0.5	4.5			
C _{IN}	Input Capacitance	0	TBD					pF		
C _{OUT}	Output Capacitance	0	TBD					pF		
C _{PD}	Power Dissipation	3.3	TBD					pF	(Note 3)	Figure 2
	Capacitance	5.0	TBD							

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC \text{ static}})$

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit

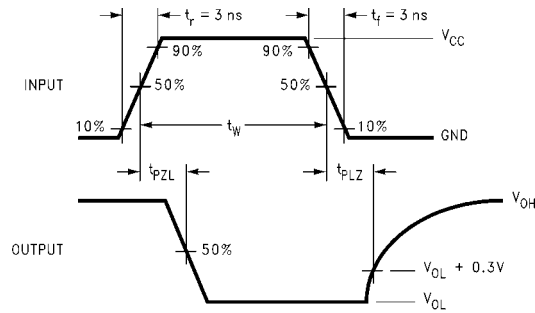
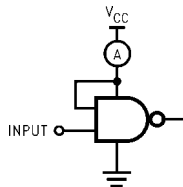


FIGURE 3. AC Waveforms



Input = AC Waveform; t_r = t_f = 1.8 ns
 PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

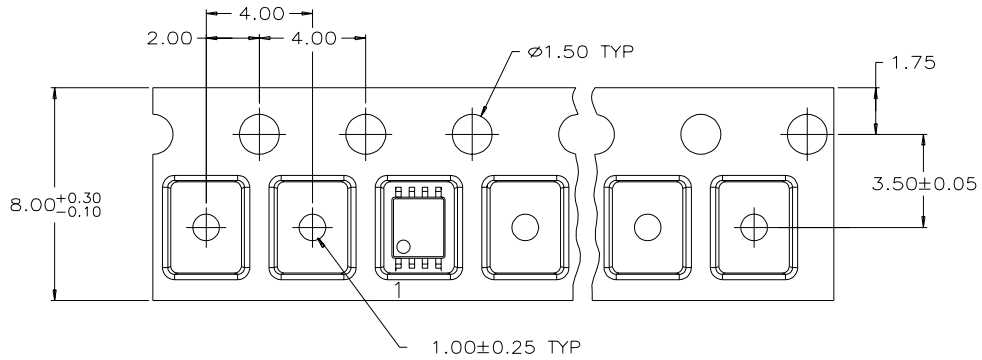
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Tape and Reel Specification

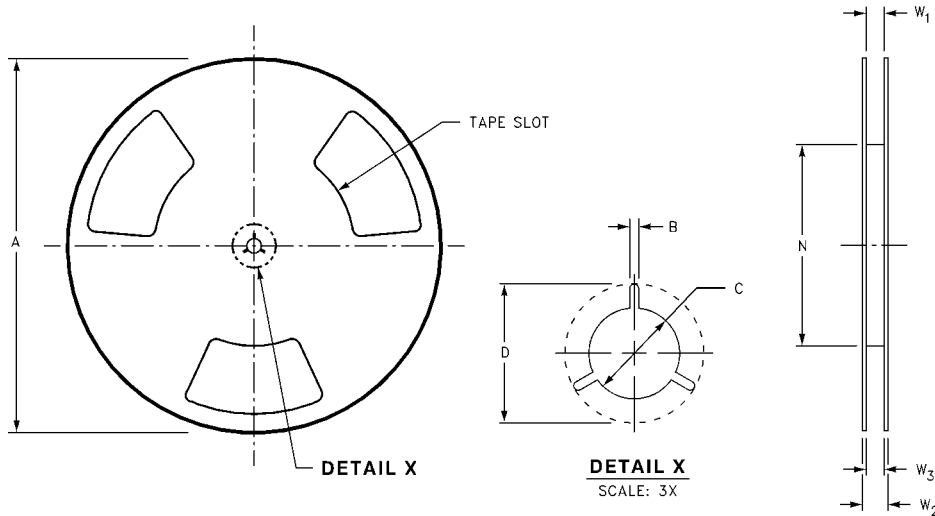
TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

