

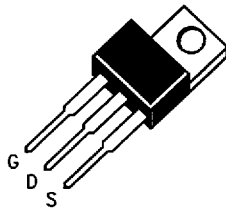
NDP605A/NDP605B, NDP606A/NDP606B N-Channel Enhancement Mode Power Field Effect Transistor

General Description

These n-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

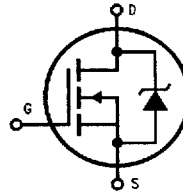
Features

- 48 and 42 Amp, 50V and 60V, $R_{DS(on)} = 0.025\Omega$ and 0.028Ω
- Critical DC electrical parameters specified at elevated temperature
- Rugged internal source-drain diode eliminates the need for external Zener Diode Transient Suppressor
- 175°C maximum junction temperature rating
- Easily paralleled for higher current applications
- High density cell design (3 million/in²) for extremely low $R_{DS(on)}$
- Lower $R_{DS(on)}$ temperature coefficient



TO-220AB

TL/G/11112-1



TL/G/11112-2

Absolute Maximum Ratings

Symbol	Parameter	NDP606A	NDP605A	NDP606B	NDP605B	Units
V_{DSS}	Drain-Source Voltage	60	50	60	50	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} = 1\text{ M}\Omega$)	60	50	60	50	V
V_{GSS}	Gate-Source Voltage—Continuous —Non Repetitive ($t_p < 50\ \mu\text{s}$)	± 20 ± 40				V
I_D	Drain Current—Continuous —Pulsed	48 144		42 126		A
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	100 0.67				W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175				$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, $1/8"$ from Case for 5 sec.	275				$^\circ\text{C}$

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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted									
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units		
OFF CHARACTERISTICS									
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	NDP605A NDP605B	50			V		
			NDP606A NDP606B	60			V		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = \text{Rated Voltage}, V_{GS} = 0V, T_J = 25^\circ\text{C}$	All			250	μA		
			All			1.0	mA		
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20V$	All			100	nA		
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20V$	All			-100	nA		
ON CHARACTERISTICS									
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	All	$T_J = 25^\circ\text{C}$	2.0	4.0	V		
				$T_J = 125^\circ\text{C}$	1.4	3.6	V		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$T_J = 25^\circ\text{C}$ $V_{GS} = 10V$	NDP605A NDP606A	$I_D = 24A$		0.020	0.025	Ω	
				$I_D = 21A$			0.028	Ω	
			NDP605A NDP606A	$T_J = 125^\circ\text{C}$ $V_{GS} = 10V$	$I_D = 24A$		0.030	0.038	Ω
				$I_D = 21A$			0.048	Ω	
g_{FS}	Forward Transconductance	$V_{GS} = 10V, I_D = 0.5 \text{ Rated } I_D$	All	10	18		mhos		
DYNAMIC CHARACTERISTICS									
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$	All		1375	1800	pF		
C_{rss}	Reverse Transfer Capacitance		All		300	400	pF		
C_{oss}	Output Capacitance		All		620	800	pF		
SWITCHING CHARACTERISTICS									
$t_{D(on)}$	Turn-On Delay Time	$V_{DD} = 25V, I_D = 0.5 \text{ Rated } I_D,$ $R_{GEN} = 7.5\Omega$ $V_{GS} = 10V$	All		16	30	ns		
t_r	Rise Time		All		80	120	ns		
$t_{D(off)}$	Turn-Off Delay Time		All		30	60	ns		
t_f	Fall Time		All		55	100	ns		
Q_g	Total Gate Charge		$V_{DS} = 0.8 \text{ Rated } V_{DSS},$	All		60		nC	
Q_{gs}	Gate-Source Charge	$I_D = \text{Rated } I_D,$	All		6		nC		
Q_{gd}	Gate-Drain Charge	$V_{GS} = 10V$	All		32		nC		

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted (Continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
SOURCE-DRAIN DIODE CHARACTERISTICS							
I_S	Maximum Continuous Source Current		NDP605A NDP606A			48	A
			NDP605B NDP606B			42	A
I_{SM}	Maximum Pulsed Source Current		NDP605A NDP606A			144	A
			NDP605B NDP606B			126	A
V_{SD}	Diode Forward Voltage	$I_S = 0.5 \text{ Rated } I_S$ $V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	All		1.3	V
			$T_J = 125^\circ\text{C}$	All		1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_S = 0.5 \text{ Rated } I_S$ $di_S/dt = 100 \text{ A}/\mu\text{s}$	All		85		ns
I_{rr}	Reverse Recovery Current		All		4.8		A
THERMAL CHARACTERISTICS							
$R_{\theta JC}$	Thermal Resistance, Junction to Case					1.50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient					62.5	$^\circ\text{C}/\text{W}$

Typical Electrical Characteristics

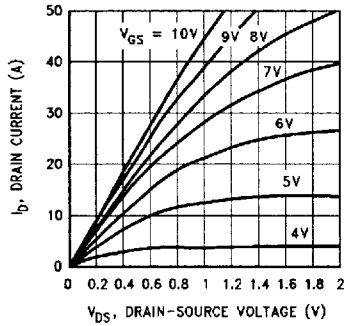


FIGURE 1. On-Region Characteristics

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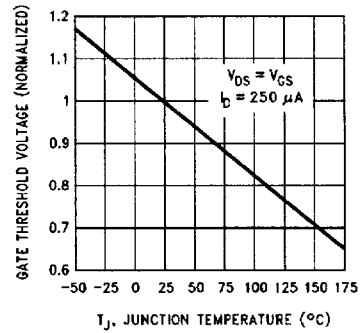


FIGURE 2. Gate Threshold Variation with Temperature

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Typical Electrical Characteristics (Continued)

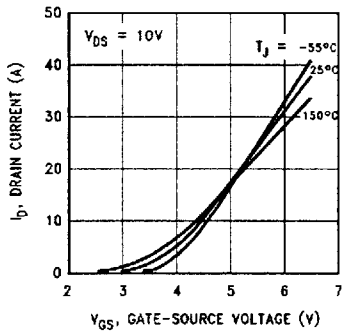


FIGURE 3. Transfer Characteristics

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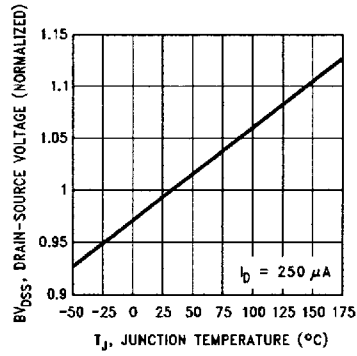


FIGURE 4. Breakdown Voltage Variation with Temperature

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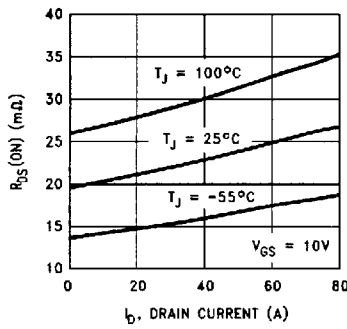


FIGURE 5. On-Resistance versus Drain Current

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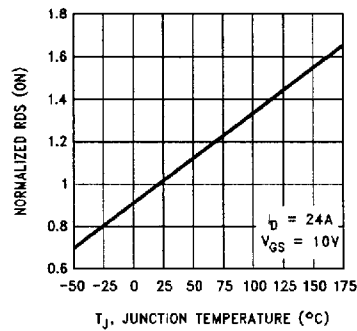


FIGURE 6. On-Resistance Variation with Temperature

TL/G/11112-8

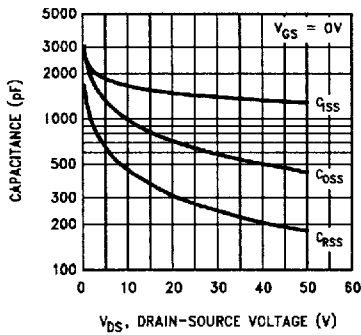


FIGURE 7. Capacitance versus Drain-Source Voltage

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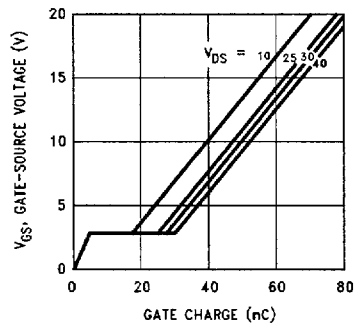


FIGURE 8. Gate Charge versus Gate-Source Voltage

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Typical Electrical Characteristics (Continued)

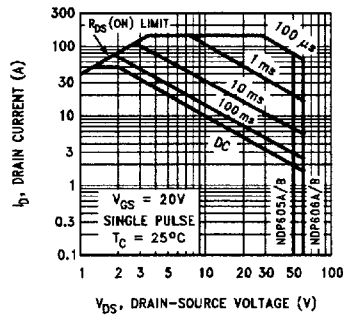


FIGURE 9. Maximum Rated Forward Biased Safe Operating Area

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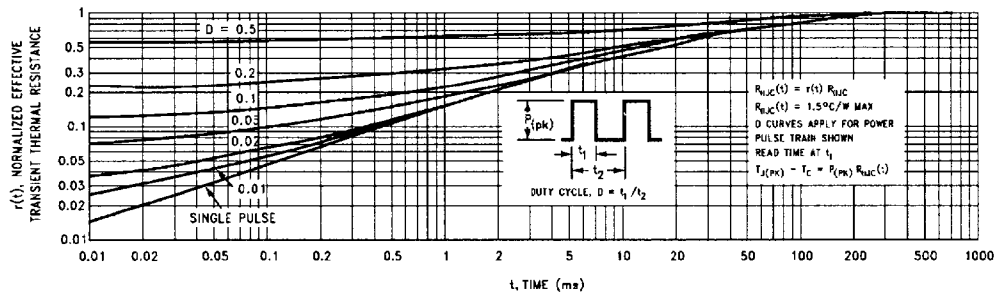


FIGURE 10. Thermal Response

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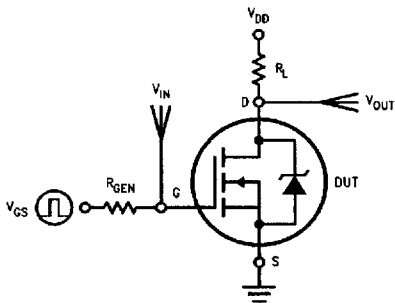


FIGURE 11. Switching Test Circuit

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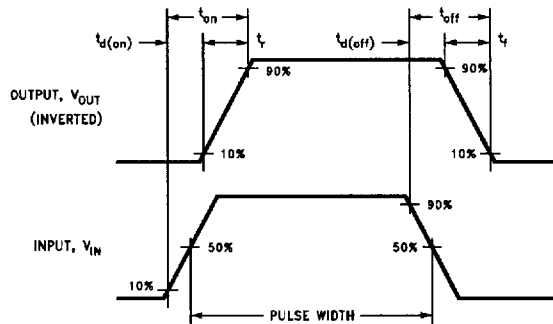
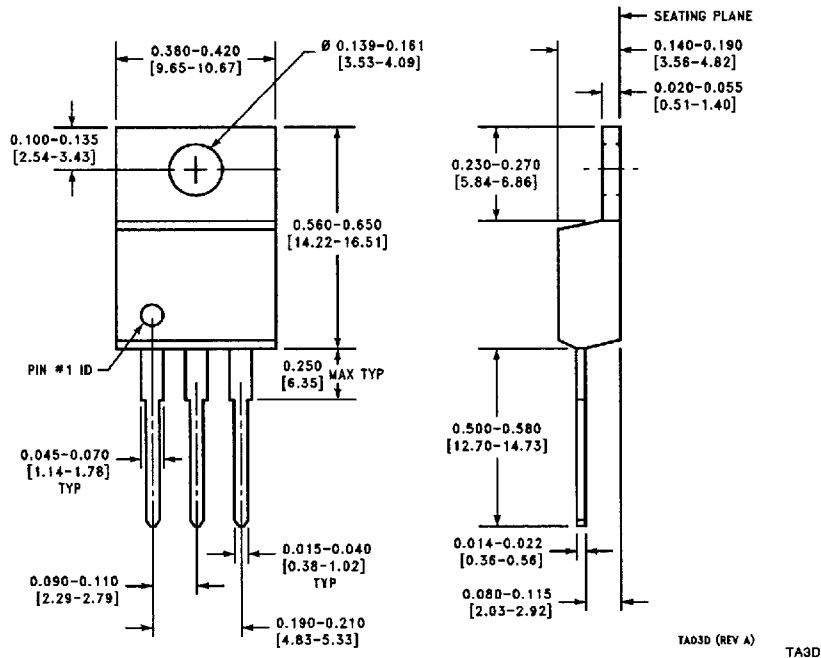


FIGURE 12. Switching Waveforms

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NDP605A/NDP605B, NDP606A/NDP606B
N-Channel Enhancement Mode Power Field Effect Transistor

Package Information



Pin	TO-220
1	Gate
2	Drain
3	Source

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