HITACHI

PM50100K

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

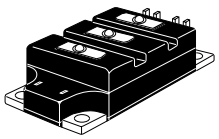
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

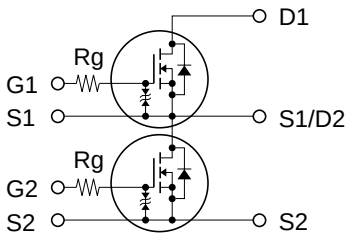
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	100	A
Drain peak current	$I_{D(peak)}$	240	A
Body-drain diode reverse drain current	I_{DR}	100	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	240	A
Channel dissipation	Pch*1	400	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

Electrical Characteristics (Ta = 25°C) (Per FET chip)

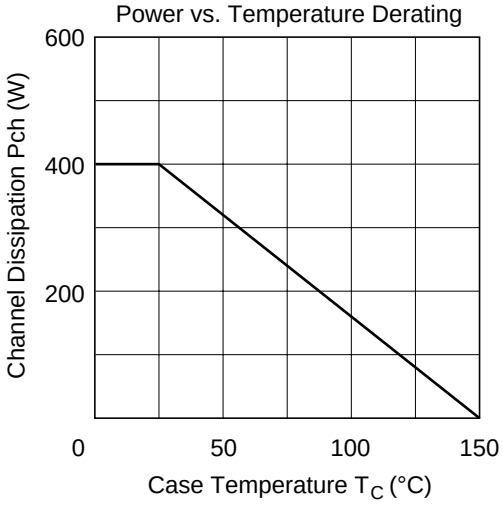
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	1	mA	V_{DS} = 400 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	4.0	5.0	V	I_D = 50 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.08	0.10	Ω	I_D = 50 A, V_{GS} = 10 V*1
Forward transfer admittance	$\|y_{fs}\|$	—	55	—	S	I_D = 50 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	14600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	3500	—		
Reverse transfer capacitance	Crss	—	650	—		
Turn-on delay time	$t_{d(on)}$	—	200	—	ns	I_D = 50 A, V_{GS} = 10 V Rg = 50 Ω R_L = 0.6 Ω
Rise time	t_r	—	690	—		
Turn-off delay time	$t_{d(off)}$	—	760	—		
Fall time	t_f	—	260	—		
Body-drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 100 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 100 A, V_{GS} = 0 V di/dt = 100 A/µs

Note: 1. Pulse Test

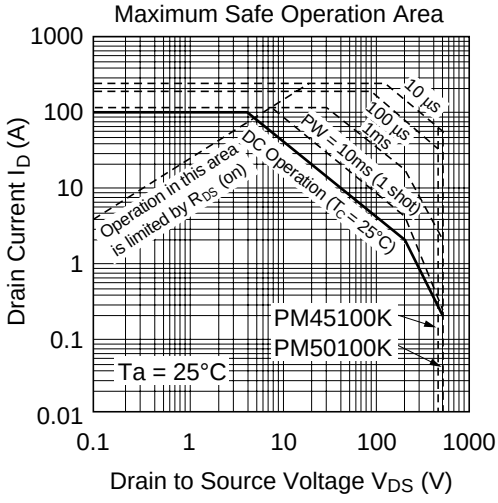
Mechanical characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	380	g

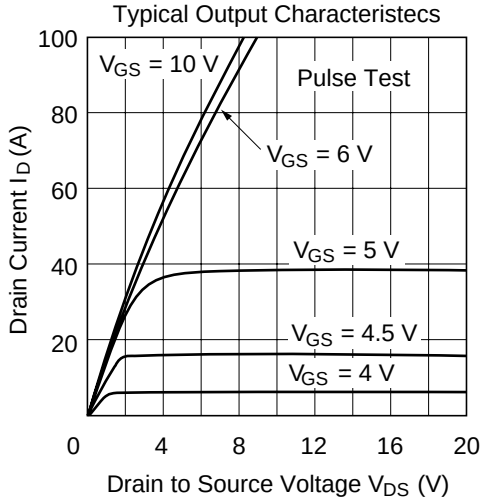
Power vs. Temperature Derating



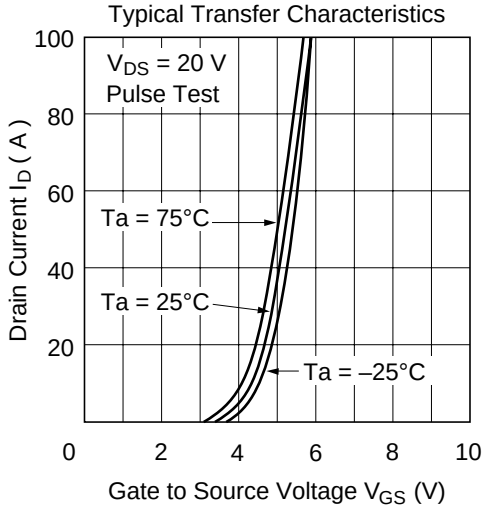
Maximum Safe Operation Area

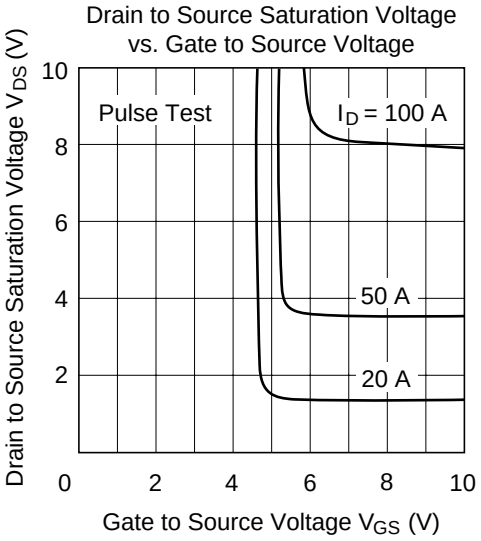


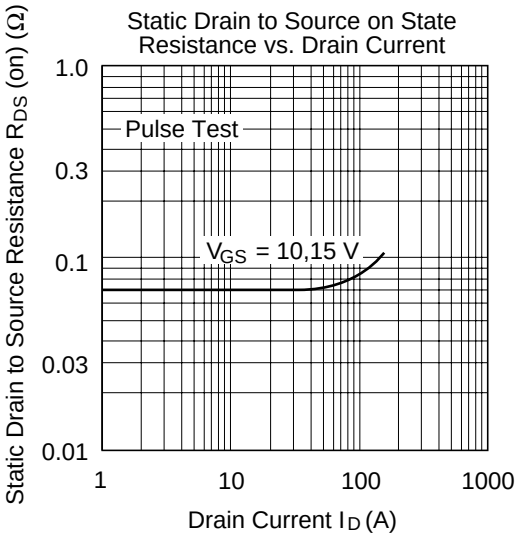
Typical Output Characteristecs

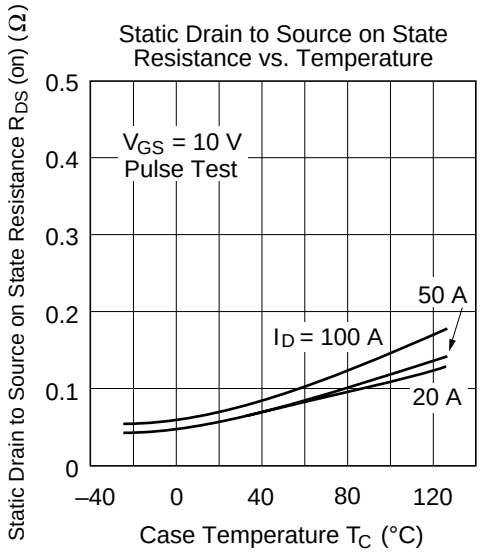


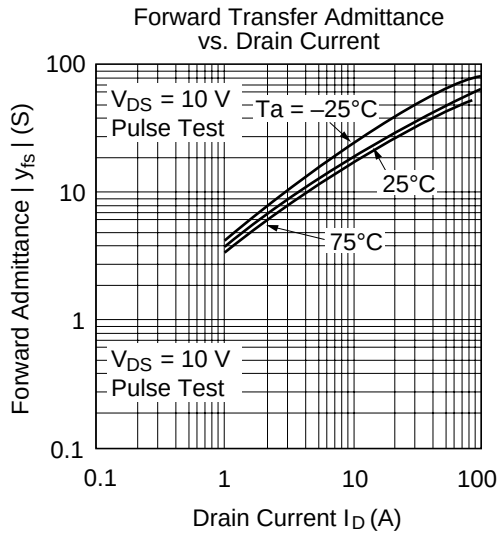
Typical Transfer Characteristics



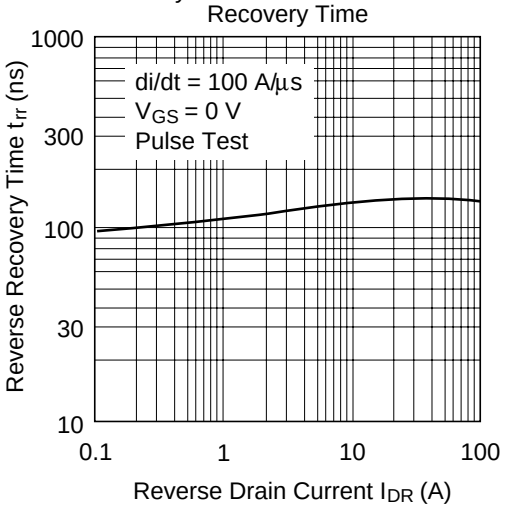

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
I_D = 100 A
50 A
20 A
10
8
6
4
2
0
2
4
6
8
10


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source Resistance R_{DS} (on) (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10,15 V
1.0
0.3
0.1
0.03
0.01
1
10
100
1000

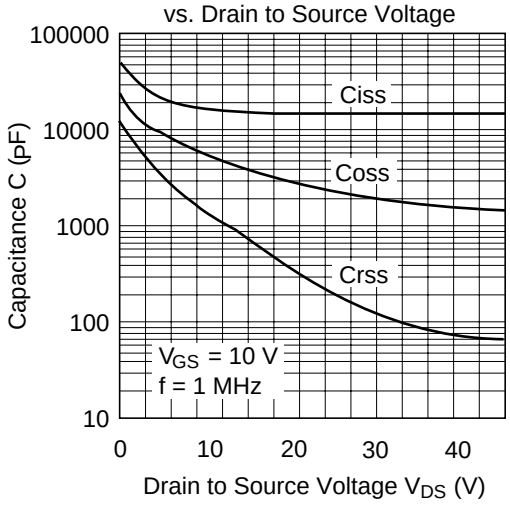

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance R_{DS} (on) (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
50 A
I_D = 100 A
20 A
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120


Forward Transfer Admittance
vs. Drain Current
Forward Admittance | y_{fs} | (S)
Drain Current I_D (A)
V_{DS} = 10 V
Pulse Test
Ta = –25°C
25°C
75°C
V_{DS} = 10 V
Pulse Test
100
10
1
0.1
0.1
1
10
100

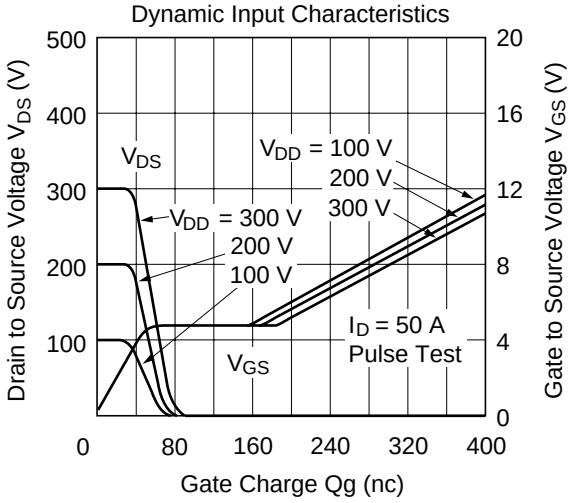
Body to Drain Diode Reverse Recovery Time



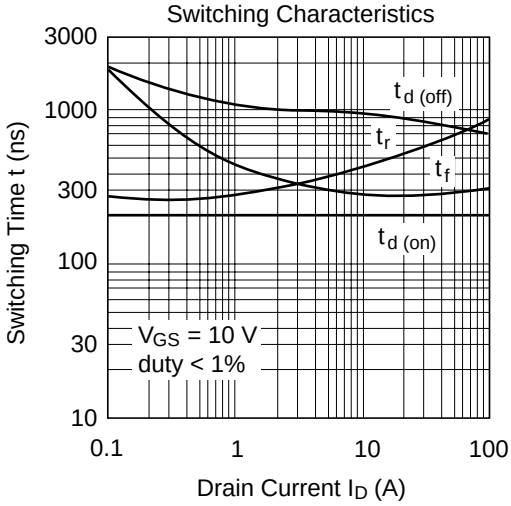
Typical Capacitance vs. Drain to Source Voltage

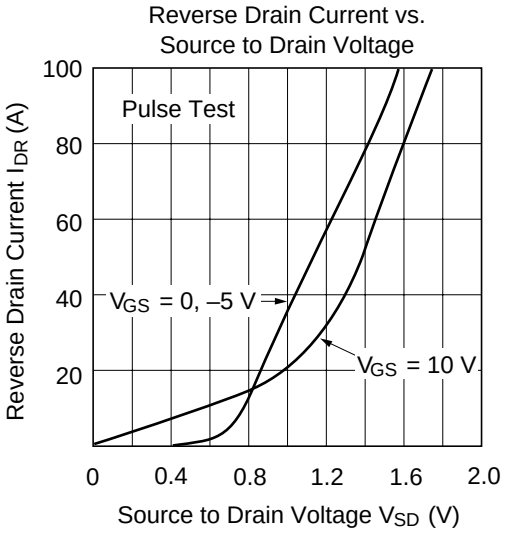


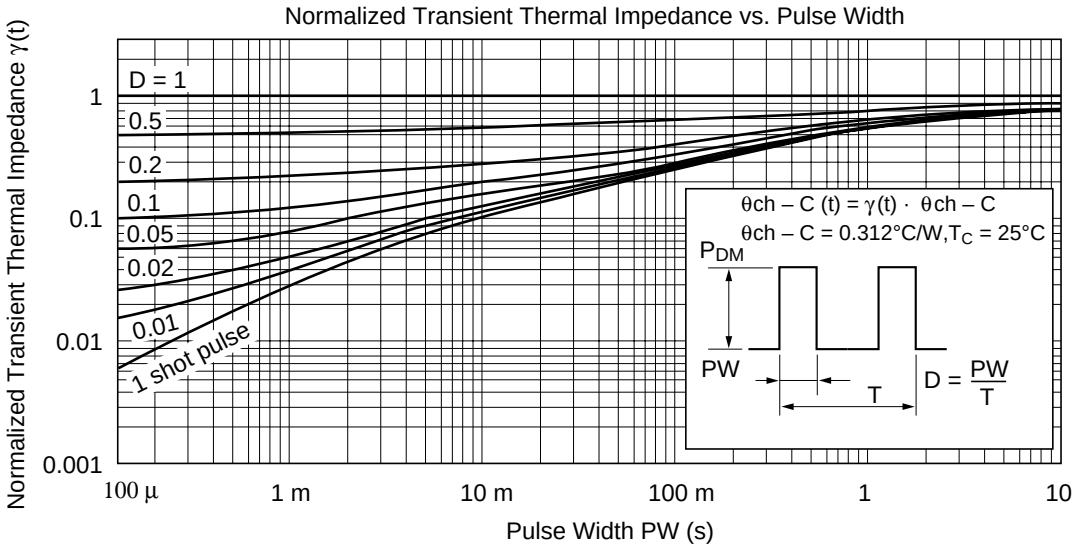
Dynamic Input Characteristics



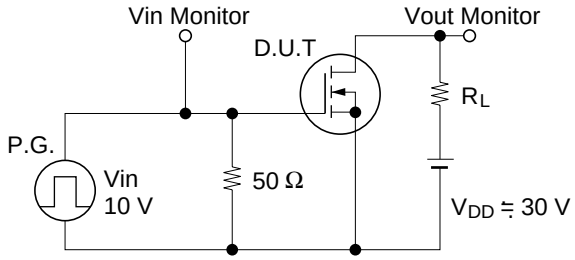
Switching Characteristics



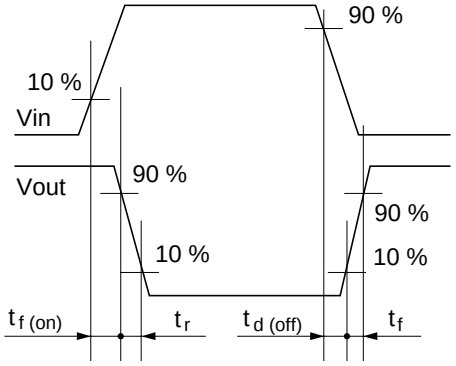

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ(t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
1
0.1
0.01
0.001
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
θch – C (t) = γ(t) · θch – C
θch – C = 0.312°C/W, T_C = 25°C
P_{DM}
PW
T
D = PW/T

Switching Time Test Circuit



Wave Forms



Package Dimensions

Unit: mm