DATA SHEET

PMBFJ174 to 177
P-channel silicon field-effect transistors

Product specification
File under Discrete Semiconductors, SC07

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Philips
Semiconductors

PHILIPS

P-channel silicon field-effect transistors PMBFJ174 to 177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT23 envelopes.They are intended for application with analogue switches, choppers, commutators etc. using SMD technology. A special feature is the interchangeability of the drain and source connections.

PINNING

1 = drain
2 = source
3 = gate

Note

1. Drain and source are interchangeable.

Marking codes:

174 : p6X
175 : p6W
176 : p6S
177 : p6Y

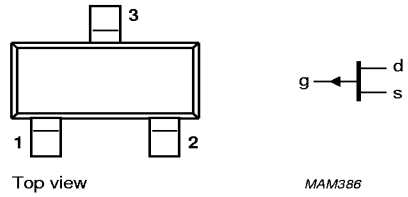

Fig.1 Simplified outline and symbol, SOT23.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation							
up to T_{amb} = 25 °C	P_{tot}	max.		300			mW
			PMBFJ174	**175**	**176**	**177**	
Drain current							
$-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance							
$-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\ on}$	<	85	125	250	300	Ω

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation				
up to T_{amb} = 25 °C[1]	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current							
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current							
$-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current							
$-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage							
I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage							
$-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\ off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance							
$-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\ on}$	<	85	125	250	300	Ω

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
V_{GS} = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF
Switching times (see Fig.2 + 3)		**PMBFJ174**	**175**	**176**	**177**	
Delay time	t_d	typ.	2	5	15	20 ns
Rise time	t_r	typ.	5	10	20	25 ns
Turn-on time	t_{on}	typ.	7	15	35	45 ns
Storage temperature	t_s	typ.	5	10	15	20 ns
Fall time	t_f	typ.	10	20	20	25 ns
Turn-off time	t_{off}	typ.	15	30	35	45 ns
Test conditions:	$-V_{DD}$		10	6	6	6 V
	$V_{GS\ off}$		12	8	6	3 V
	R_L		560	1200	2000	2900 Ω
	$V_{GS\ on}$		0	0	0	0 V

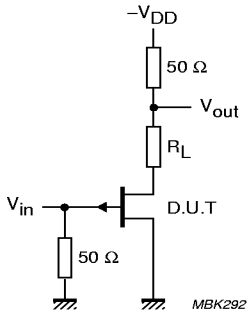
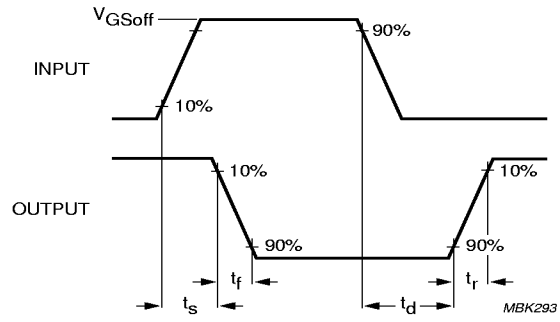


Fig.2 Switching times test circuit



Rise time input voltage < 1 ns

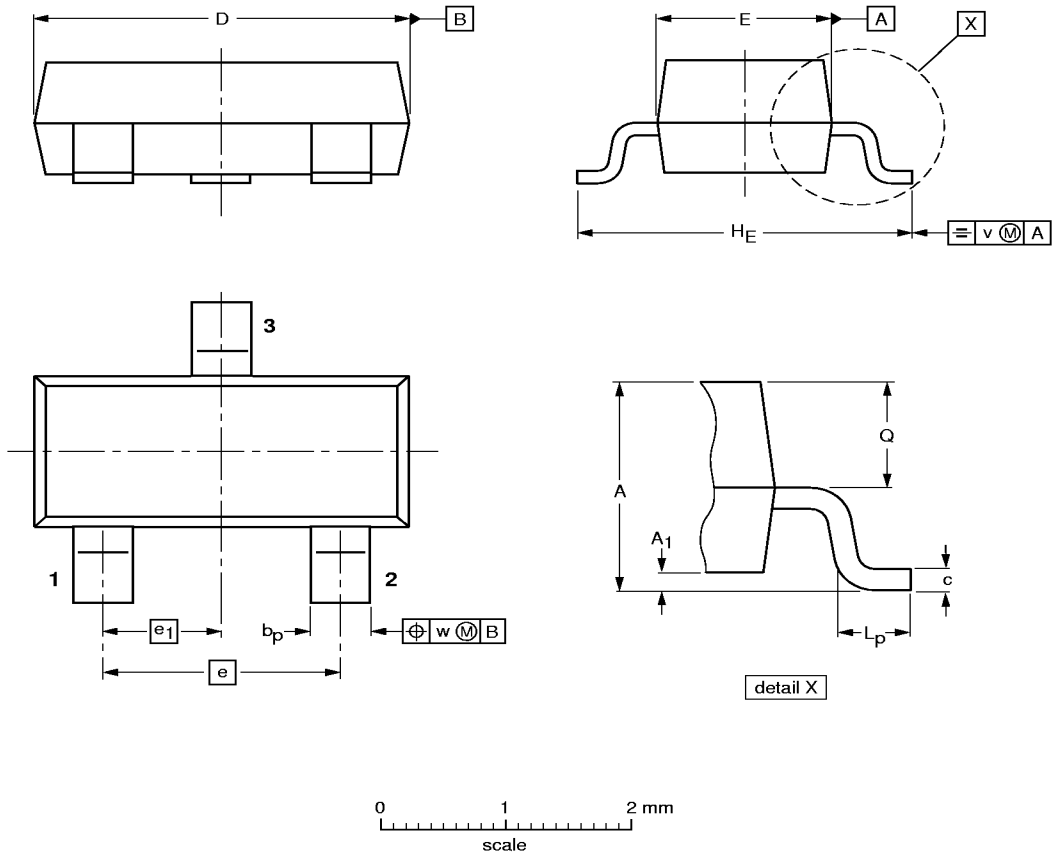
Fig.3 Input and output waveforms

$t_d + t_r = t_{on}$

$t_s + t_f = t_{off}$

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28