RC5052

High Performance Programmable Synchronous DC-DC Controller for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- Remote sense
- Active Droop
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- Drives N-channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components
- Adjustable deadtime, frequency
- Crowbar protection for overvoltage

Applications

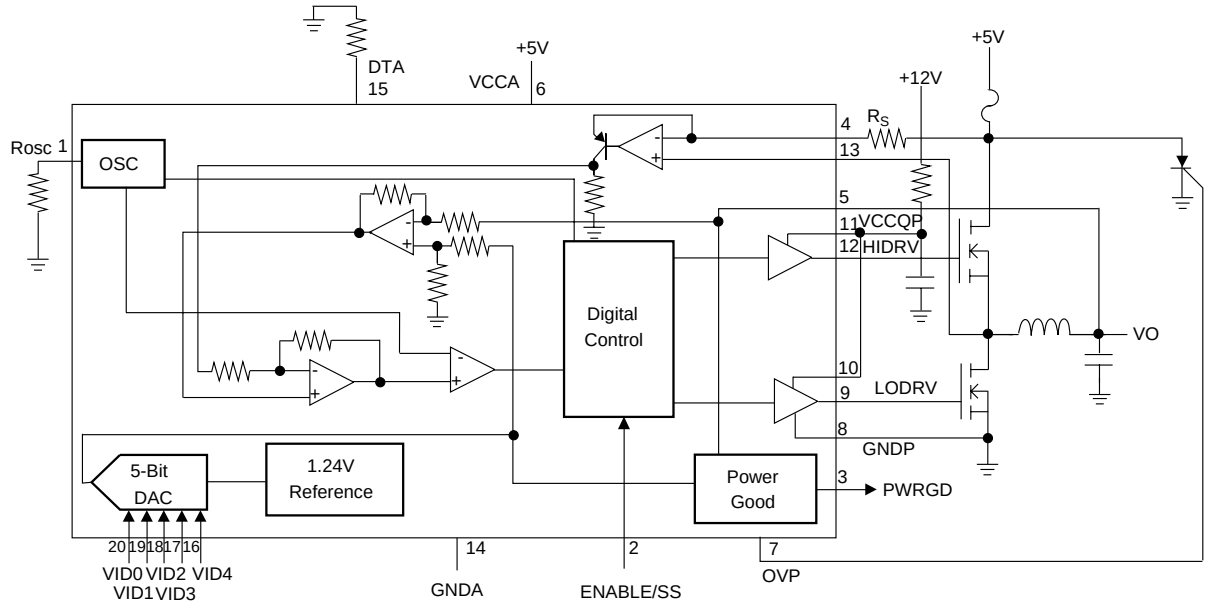
- Power supply for Pentium® II & III
- VRM for Pentium II & III processor
- Telecom line cards
- Routers, switches & hubs
- Programmable step-down power supply

Description

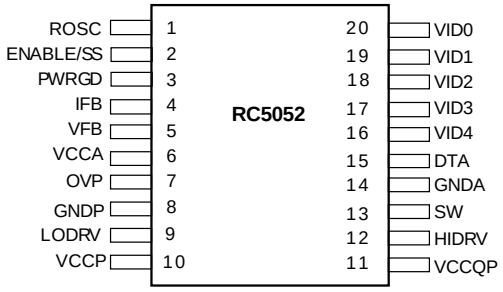
The RC5052 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable output voltage for all Pentium II & III CPU applications and other high-performance processors. The RC5052 features remote voltage sensing, adjustable current limit, and active droop for optimal converter transient response. The RC5052 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5052 uses a high level of integration to deliver load currents in excess of 16A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while active droop permits exact tailoring of voltage for the most demanding load transients. The RC5052 also offers integrated functions including Power Good, Output Enable/ Soft Start, current limiting, adjustable frequency, adjustable deadtime and overvoltage crowbar protection, and is available in a 20 pin SOIC package.

Preliminary Specification

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	ROSC	**Oscillator Resistor Connection.** Connect an external resistor to this pin to set the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE/SS	**Output Enable/Soft Start.** A logic LOW on this pin will disable the output. An internal current source allows for open collector control. This pin also doubles as soft start.
3	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
4	IFB	**Current Feedback.** Pin 4 is used in conjunction with pin 13, as the input for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback.** Pin 5 is used as the input for the voltage feedback control loop. See Application Information for details regarding correct layout.
6	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
7	OVP	**Over Voltage Protection.** This pin triggers the gate of an external SCR.
8	GNDP	**Power Ground.** Return pin for high currents flowing in pins 10 and 11. Connect to a low impedance ground.
9	LODRV	**Low Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
10	VCCP	**Power VCC.** For low side FET driver. Connect to either system 12V supply or 5V supply, and decouple with a 4.7µF tantalum and a 0.1µF ceramic capacitor.
11	VCCQP	**High Side Power VCC.** For high side FET driver. Connect to system 12V supply, and decouple with a 4.7µF tantalum and a 0.1µF ceramic capacitor.
12	HIDRV	**High Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
13	SW	**High side driver source and low side driver drain switching node.** Together with IFB pin allows FET sensing for current.
14	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
15	DTA	**Dead Time Adjust.** Connect an external resistor to this pin to set the dead time.
16–20	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.

Preliminary Specification

Absolute Maximum Ratings

Supply Voltages VCCA, VCCP, VCCQP to GND	13.5V
Supply Voltages (VCCQP, Charge Pump)	18V
Voltage Identification Code Inputs, VID0-VID4	VCCA
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Power Dissipation, P_D	750mW
Thermal Resistance Junction-to-case, Θ_{JC}	105°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP & VCCQP		11.4	12	13.2	V

Preliminary Specification

Electrical Specifications (V_{CCA} = 5V, V_{CCP} = V_{CCQP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{CCA} = 4.75V to 5.25V, V_{OUT} = 2.000V	•		±2		mV
Internal Droop[3]	V_{OUT} at I_{LOAD} = 0.8A to I_{max}		-44	-40	-36	mV
Output Ripple	20MHz BW, I_{LOAD} = I_{max}			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to I_{max},V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45		60	µA
Efficiency	I_{LOAD} = I_{max}, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 5 for t_R and t_F			50		nsec
Output Driver Deadtime	R_{OTA} = OPEN. See Figure 5 for t_{DT}			50		nsec
Oscillator Frequency	R_{OSC} = OPEN	•	255	300	345	kHz
Oscillator Range			80		1000	kHz
Duty Cycle			0		100	%
Dead Time Range			50		120	nsec
PWRGD Threshold	Logic HIGH Logic LOW	• •	93 88		107 112	%V_{out}
V_{CCA} UVLO		•	3.74	4	4.26	V
V_{CCP} UVLO		•	7.65	8.5	9.35	V
V_{CCA} Supply Current				19		mA
V_{CCP} Supply Current[4]				40		mA
Soft Start Current		•	5	10	17	µA
OVP Output Low Voltage	I = 1mA				200	mV
OVP Ouput High Current	V = 1.5V		30			mA
OVP Trigger Threshold			115	120	125	%V_{out}

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, -80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, -70mV at the capacitors will also be met.
4. Includes gate current.

Table 1. Output Voltage Programming Codes

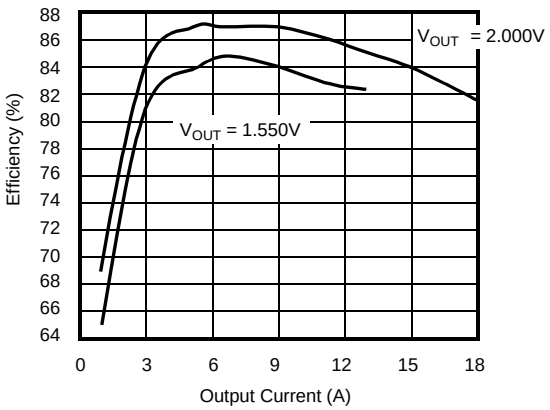
VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Note:

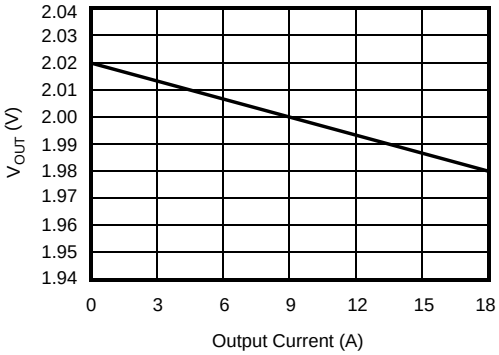
1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

Typical Operating Characteristics (V_{CCA} = 5V, V_{CCP} = V_{CCQP} = 12V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)

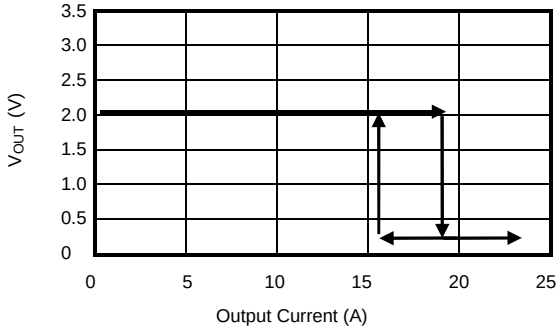
Efficiency vs. Output Current



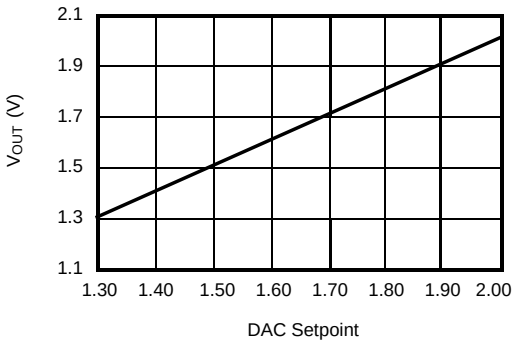
Droop, V_{OUT} = 2.0V



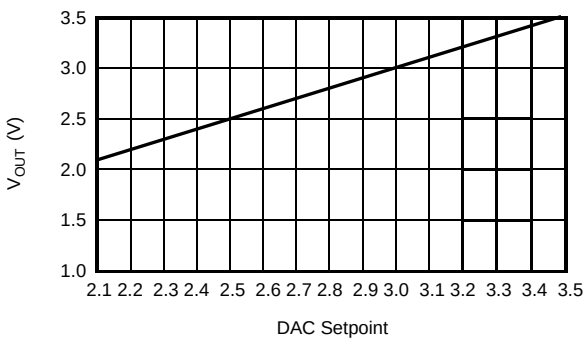
Output Voltage vs. Output Current



Output Programming, VID4 = 0



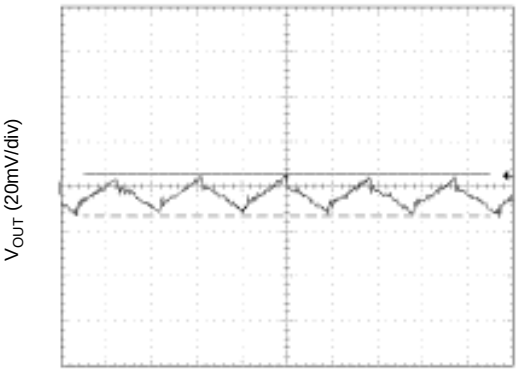
Output Programming, VID4 = 1



Preliminary Specification

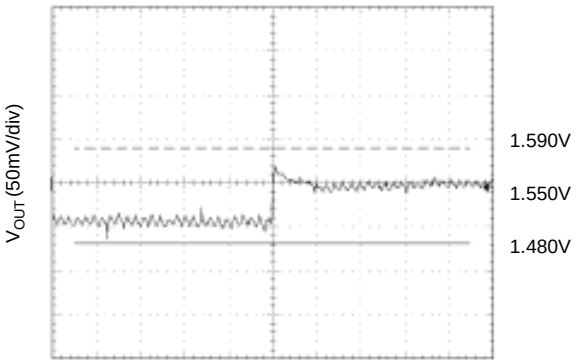
Typical Operating Characteristics (continued)

Output Ripple, 2.0V @ 18A



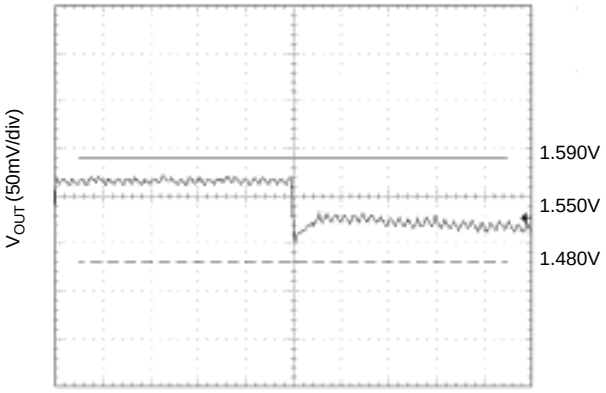
Time (1µs/division)

Transient Response, 12.5A to 0.5A



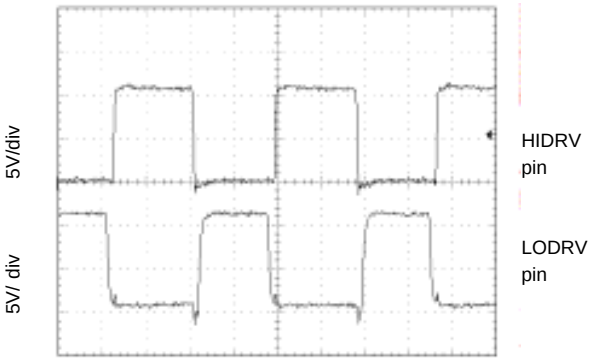
Time (20µs/division)

Transient Response, 0.5A to 12.5A



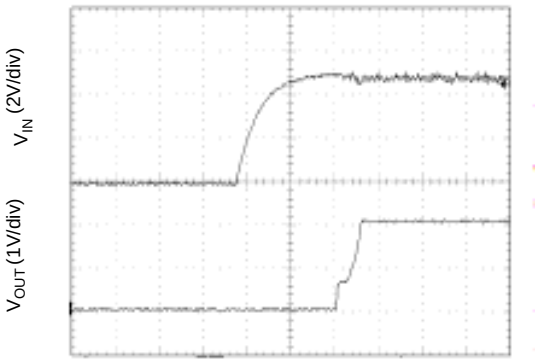
Time (20µs/division)

Switching Waveforms, 18A Load



Time (1µs/division)

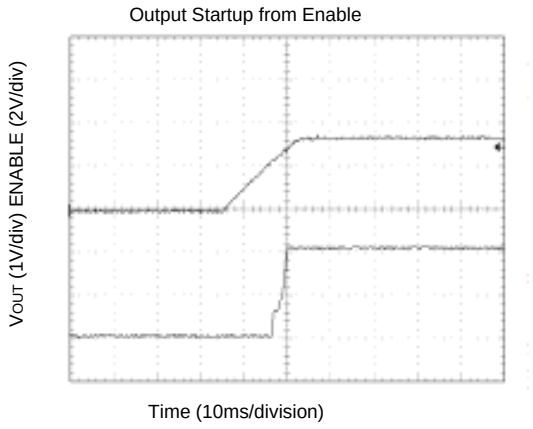
Output Startup, System Power-up

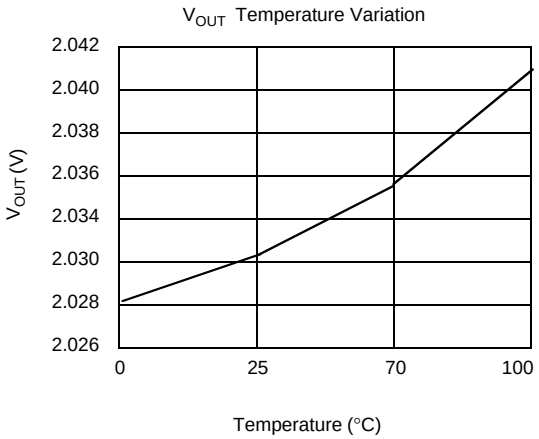


Time (10ms/division)

Preliminary Specification

Typical Operating Characteristics (continued)





Application Circuit

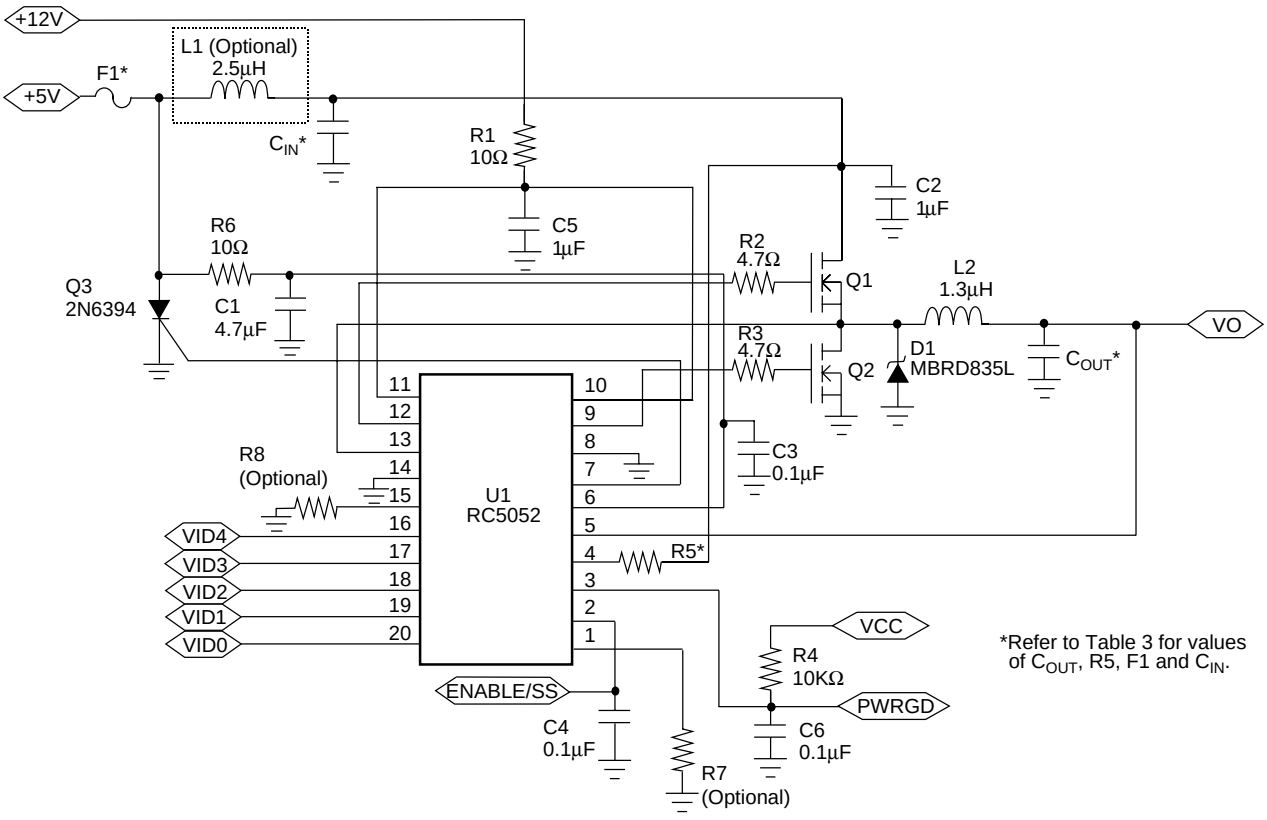


Figure 1. Application Circuit for Katmai, Mendocino, and Some Coppermine Processors
(*Worst Case Analyzed!* See Appendix for Details)

Preliminary Specification

Table 2. RC5052 Application Bill of Materials for Intel Pentium II Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	*	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
F1	Littelfuse	1	*	
U1	Fairchild RC5052M	1	DC/DC Controller	

*See Table 3.

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Table 3. Recommended Values for CPU-based Applications

Processor	Chipset	C_{IN}	C_{OUT}*	R5 (KΩ)	F1 (A)
Coppermine	Whitney	3	4	8.45	5
Katmai	Camino	4	6	13.0	10
Mendocino	Whitney	4	5	11.3	10
Katmai	BX	5	6	11.8	10

* Output capacitance requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details. See the Appendix to this datasheet for the method of calculation of these components. Pin 4 must be used to remote sense the voltage at the processor to achieve the specified performance.

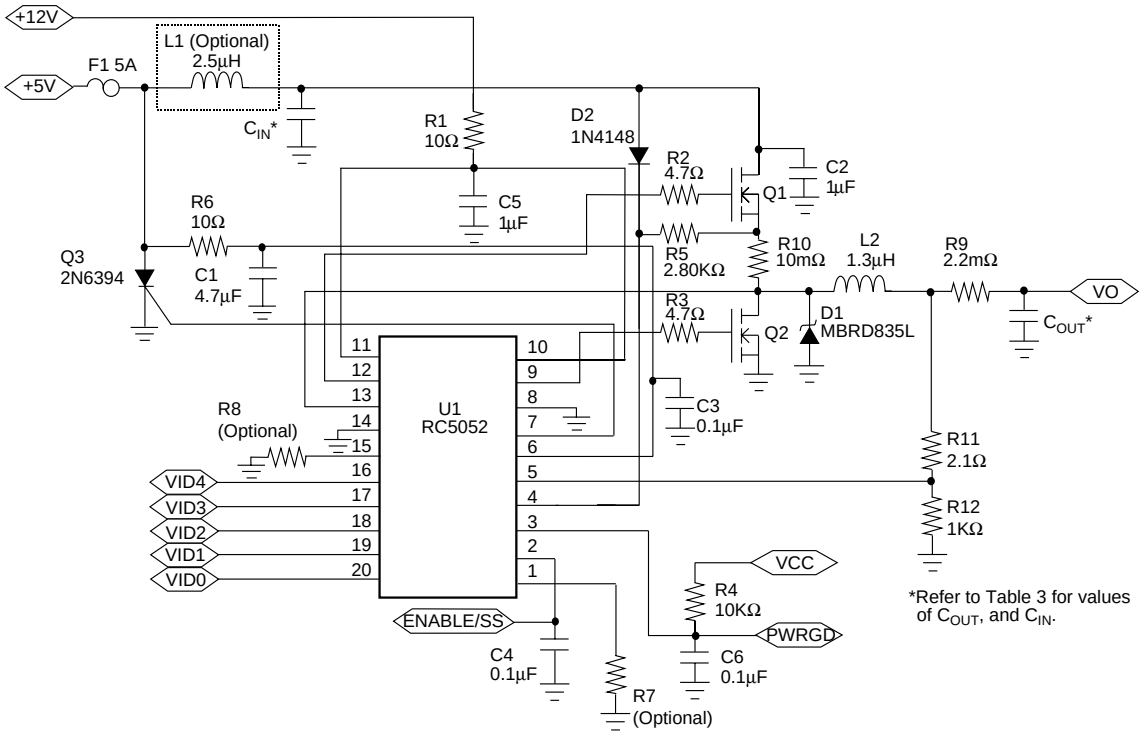


Figure 2. Application Circuit for Coppermine/Camino Processors
(*Worst Case Analyzed!* See Appendix for Details)

Table 4. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	10	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
D2	Fairchild 1N4148	1	Signal Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDP6030L or FDB6030L	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDP7030BL or FDB7030BL	1	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	2.80KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	Any	1	2.2mΩ	PCB Trace Resistor
R10	Dale WSL-2512-.01Ω	1	10mΩ, 1W Resistor	
R11	Any	1	2.1Ω	
R12	Any	1	1KΩ	
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

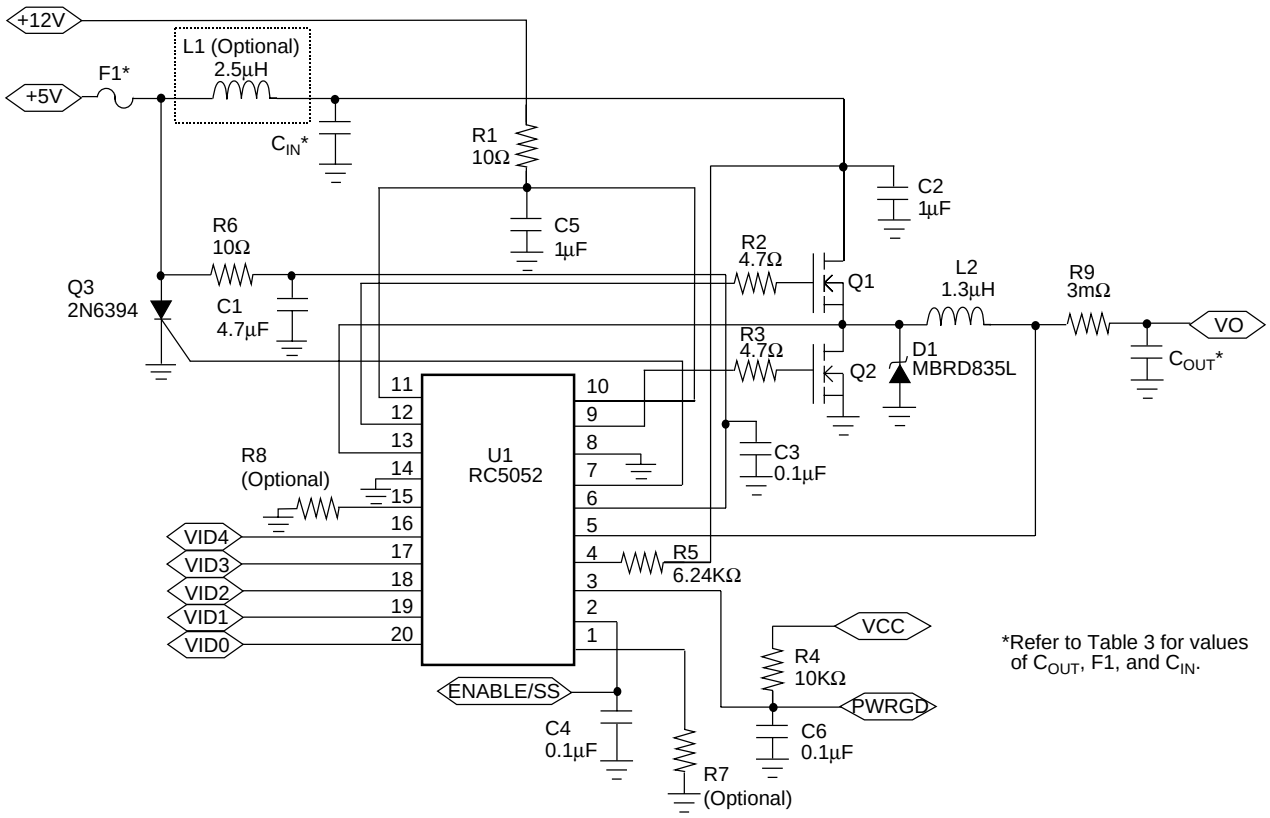


Figure 3. Application Circuit for Coppermine/Camino Processors
(*Typical Design*)

Table 5. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1-2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ VG_S = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6	Any	2	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	6.24KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	N/A	1	3.0mΩ	PCB Trace Resistor
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

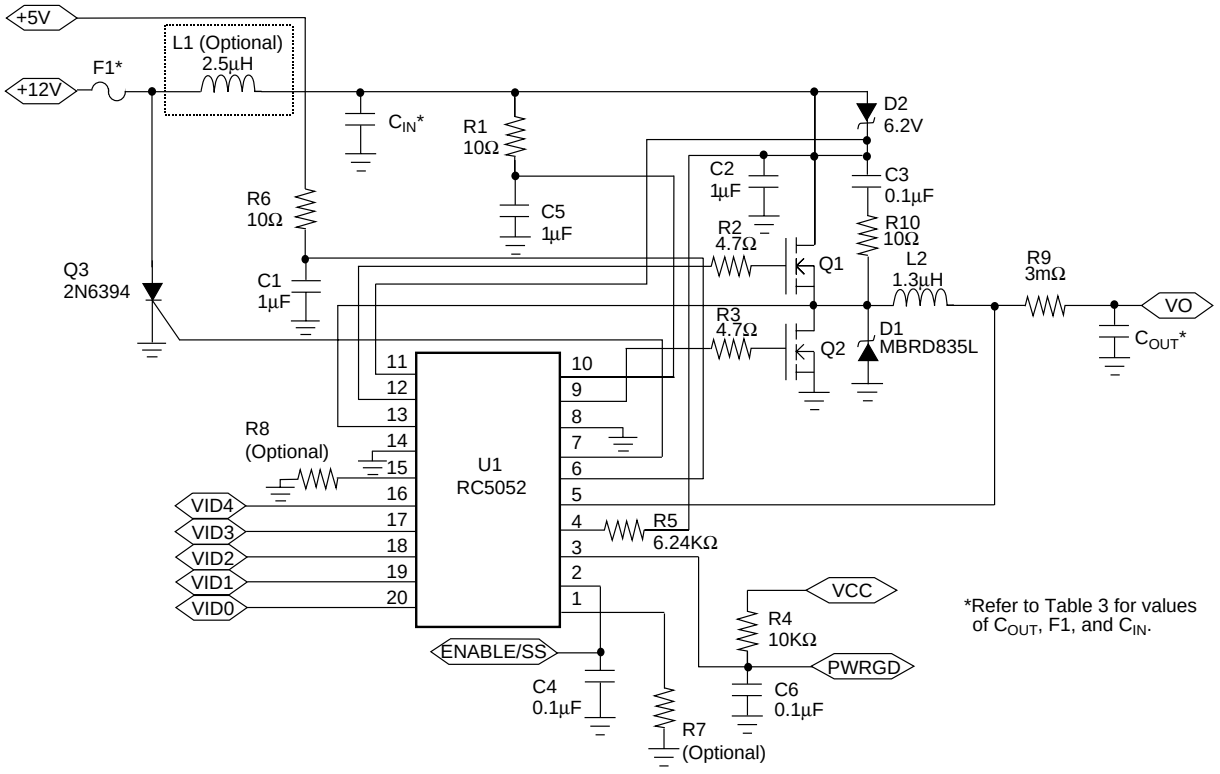


Figure 4. Application Circuit for Coppermine/Camino Processors
(*Typical Design*)

Table 6. RC5052 Application Bill of Materials for Coppermine/Camino Processors
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1-2, C5	AVX TAJB475M010R5	3	1µF, 16V Capacitor	
C3-4,6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	8	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MDRDS835L	1	8A Schottky Diode	
D2	Fairchild MMSZ5233B	1	6.2V Zener	
L1	Any	Optional	2.5µH, 10A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1-2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ VG_S = 4.5V See Note 2.
Q3	Motorola 2N6394	1	SCR	
R1, R6, R10	Any	3	10Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	6.24KΩ	
R7	Any	Optional		Sets frequency.
R8	Any	Optional		Sets deadtime.
R9	N/A	1	3.0mΩ	PCB Trace Resistor
F1	Littelfuse R251 005	1	5A Fast Fuse	
U1	Fairchild RC5052M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Test Parameters

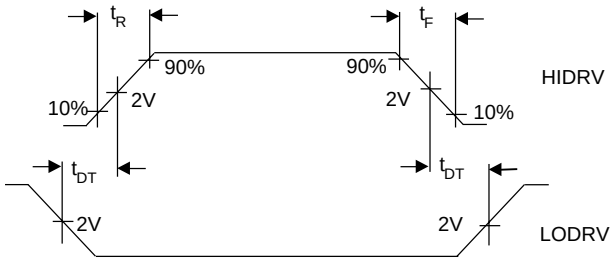


Figure 5. Output Drive Timing Diagram

Application Information

The RC5052 Controller

The RC5052 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5052 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The RC5052 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5052 Block Diagram on page 1. The RC5052 implements "summing mode control", which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the IFB and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the RC5052 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5052 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers' power and ground are separated from the chip's power and ground for switching noise immunity. The high-side driver's power supply pin, VCCQP, is supplied from an external 12V source through a series resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$. The low-side driver's power supply pin, VCCP, is supplied from either 5V or from the same source as VCCQP. Choosing 12V will ensure lowest possible $R_{DS,ON}$; choosing 5V will result in lower gate current, which may be important when operating the RC5052 at high frequency and lower output power. The VCCQP pin may also be run as charge pump for +12V Main Power, as shown in Figure 4.

Internal Voltage Reference

The reference included in the RC5052 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V. The output voltage may be changed while the converter is on by changing the VID codes; however, it is necessary to do so in 1-bit steps, to avoid triggering the overvoltage protection.

Power Good (PWRGD)

The RC5052 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The output is guaranteed open-collector high when the power supply voltage is within ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5052.

Output Enable/Soft Start (ENABLE/SS)

The RC5052 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to soft-start the switching.

Over-Voltage Protection

The RC5052 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the RC5052 disables the output drive signal to the external high-side MOSFET, and drives the OVP pin high. This is designed to drive the gate of an external SCR, which blows a fuse, disconnecting the short from the power bus.

Oscillator

The RC5052 oscillator free runs at 300 kHz, and may be adjusted from 80KHz to 1MHz as desired. Higher frequensies will permit smaller components, while decreasing efficiency. A typical operating frequency is 300KHz. The frequency may be adjusted upwith a resistor to ground on pin 1, according to the formula:

$$f = 300kHz^* \frac{40K\Omega}{R_{OSC}}$$

and may be adjusted down with aresistor to 5V on pin 1, according to the formula:

$$f = 300kHz^* \left(1- \frac{160K\Omega}{R_{OSC}}\right)$$

Dead Time

The RC5052 can control the deadtime, that is, the time between when the high-side MOSFET is turned off and the low-side MOSFET is turned on, and vice versa. Longer dead times are appropriate when using multiple MOSFETs in parallel, or when MOSFETs with larger gate capacitance are used. The dead time may be adjusted with a resistor to ground on pin 15, according to the formula:

$$T_{DT} = 100nsec^* \frac{R_{DTA}}{80K\Omega}$$

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance (RDS,ON) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply

V_{out} = Output Voltage

f = DC/DC converter switching frequency

ESR = Equivalent series resistance of all output capacitors in parallel

V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_0 \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:

C_o = The total output capacitance

I_{pp} = Maximum to minimum load transient current

V_{tb} = The output voltage tolerance budget allocated to load transient

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D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The RC5052 provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5052 Short Circuit Current Characteristics

The RC5052 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} \times *R_{DS,\,on}}{I_{Detect}}$$

with $I_{Detect} \approx 50\mu A$, I_{SC} the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET, as shown in Figure 6, eliminates this source of inaccuracy in the current limit. Note one addition of one diode, which is necessary for proper operation of this circuit.

As an example, Figure 6 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

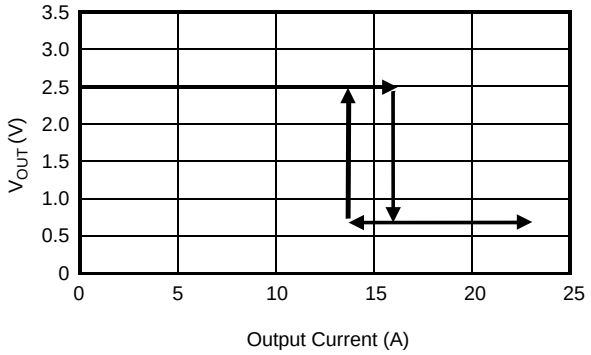


Figure 6. RC5052 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C. This is the reason for using the external sense resistor.) At this point, the internal comparator trips and signals the controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

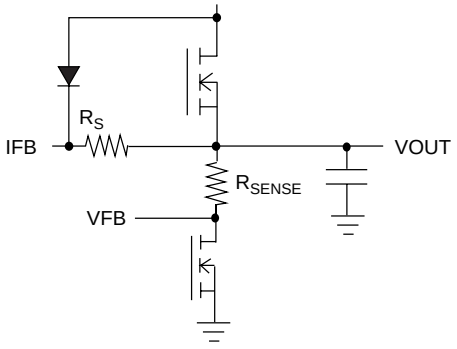


Figure 7. Precision Current Sensing

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 8. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 8 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A RMS of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

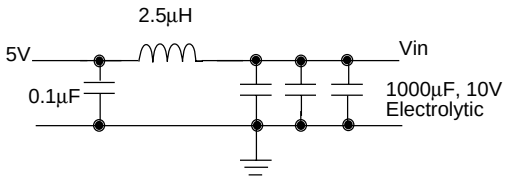


Figure 8. Input Filter

Active Droop

The RC5052 includes active droop: as the output current increases, the output voltage drops. This is done in order to allow maximum headroom for transient response of the converter. The current is sensed by measuring the voltage across the high-side MOSFET during its on time. Note that this makes the droop dependent on the temperature of the MOSFET. However, when the formula given for selecting R_S (current limit) is used, there is a maximum droop possible (-40mV), and when this value is reached, additional drop across the MOSFET will not cause any increase in droop—until current limit is reached.

Additional droop can be added to the active droop using a discrete resistor (typically a PCB trace) outside the control loop, as shown in Figure 1. This is typically only required for the most demanding applications, such as for the next generation Intel processor (tolerance = +40/-70mV), as shown in Figure 1.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5052 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5052 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5052. That is, traces that connect to pins 9, 10, 11, 12 and 13 (LODRV, VCCP, VCCQP, HIDRV and SW) should be kept far away from the traces that connect to pins 4 through 6, and pin 14.
- Place the 0.1µF decoupling capacitors as close to the RC5052 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5052 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-968-9211 x7624.

RC5052 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the RC5052. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-968-9211 x7624 for an evaluation board.

Additional Information

For additional information contact Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-968-9211 x7624.

Appendix

Worst-Case Formulae for the Calculation of C_{out}, R5, and C_{in} (Circuit of Figure 1 Only)

The following formulae design the RC5052 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, active droop tolerance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

ESR, the ESR of the output caps, per cap (44mΩ for the Sanyo parts shown in this datasheet);

R_D, the on-resistance of the MOSFET (20mΩ for the FDB6030);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature).

I_{rms}, the rms current rating of the input caps (2A for the Sanyo parts shown in this datasheet).

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R5 = \frac{I_O * R_D * (1 + \Delta R_D) * 1.10}{50 * 10^{-6}}$$

Number of capacitors needed for C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}|}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - 0.004 * V_{nom} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing and the usual caps. We have V_{T+} = $|V_{T-}|$ = 0.134, I_O = 14.2, V_{nom} = 2.000, and ΔR_D = 0.67. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R5 = \frac{14.2 * 0.020 * (1 + 0.67) * 1.10}{50 * 10^{-6}} = 10.4K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134} = 4.66$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.004 * 2.000 + \frac{14400 * 14.2 * 0.020}{18 * 10400 * 1.1}} = 4.28$$

Since X > Y, we choose X, and round up to find we need 5 capacitors for C_{OUT}.

A detailed explanation of this calculation, and the calculations used for Figure 2, may be found Applications Bulletin AB-XX.

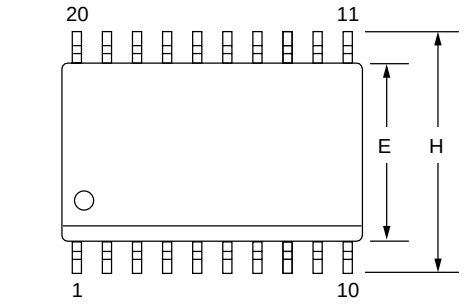
Mechanical Dimensions

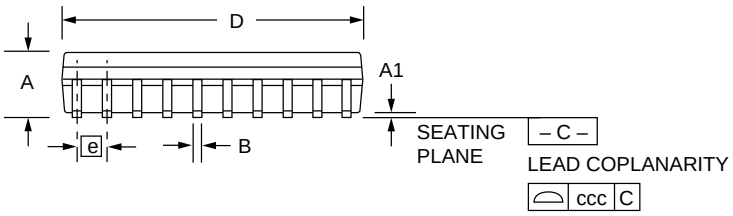
20 Lead SOIC

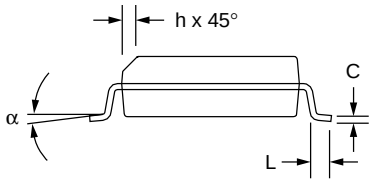
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
RC5052M	20 pin SOIC

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