RC5060

ACPI Switch Controller

Features

- Implements ACPI control with PWROK, SLP_S3# and SLP_S5#
- Switch and linear regulator controller for 3.3V Dual (PCI)
- Linear regulator controller and linear regulator for 2.5V Dual (RAMBUS)
- Two switch controller for 5V Dual (USB)
- Switch controller and linear regulator for 3.3V SDRAM
- Provides SDRAM and RAMBUS power simutaneously
- Adaptive Break-before-Make
- Integrated Power Good
- Drives all N-Channel MOSFETs plus NPN
- Latched overcurrent protection for outputs, functional during startup too
- Power-up softstarts for the linear regulators
- UVLO guarantees correct operation for all conditions
- 20 pin SOIC package

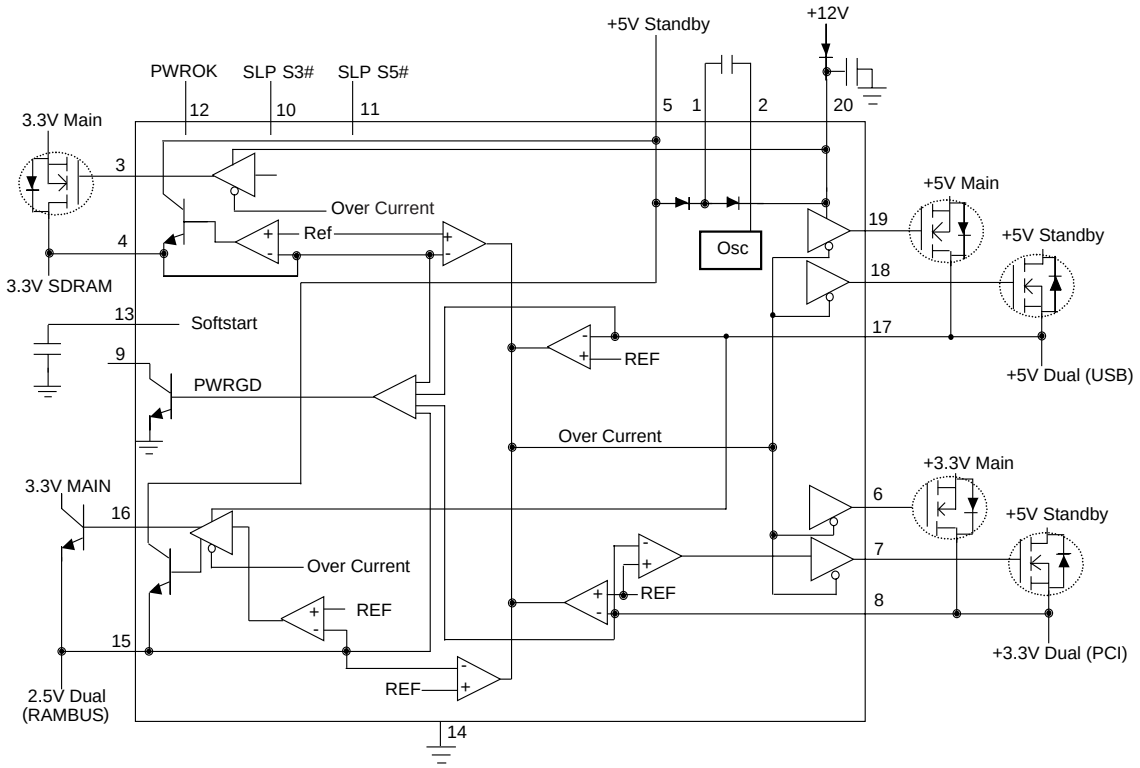
Applications

- Camino Platform ACPI Controller
- Whitney Platform ACPI Controller

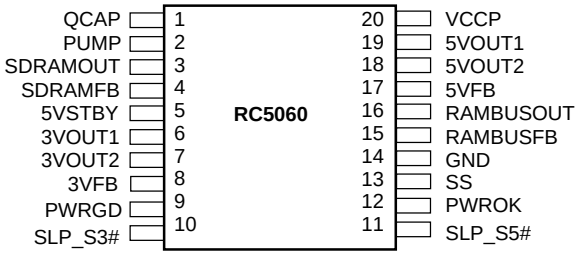
Description

The RC5060 is an ACPI Switch Controller for the Camino and Whitney Platforms. It is controlled by PWROK, SLP_S3# and SLP_S5#, and provides 3.3V Dual for PCI, 3.3V for SDRAM, 2.5V Dual for RAMBUS, and 5V Dual voltages. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5060 also offers integrated Power Good and Current Limiting that protects each output, and softstart for the linear regulators. The RC5060 is available in a 20 pin SOIC.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	QCAP	**Charge pump cap.** Attach flying capacitor between this pin and PUMP to generate high voltage from standby power.
2	PUMP	**Charge pump switcher.**
3	SDRAMOUT	**3.3V SDRAM gate control.** Attach this pin to a transistor powering 3.3V SDRAM from the 3.3V main supply.
4	SDRAMFB	**3.3V SDRAM voltage feedback.** Pin 4 is used as the input for the voltage feedback control loop for 3.3V SDRAM, and also sources 3.3V SDRAM in standby.
5	5VSTBY	**5V Standby.** Apply +5V standby on this pin to run the circuit in standby mode.
6	3VOUT1	**3.3V main gate control.** Attach this pin to a transistor powering 3.3V dual from the 3.3V main supply.
7	3VOUT2	**3.3V standby gate control.** Attach this pin to a transistor powering 3.3V dual from the 5V standby supply.
8	3VFB	**3.3V voltage Feedback.** Pin 8 is used as the input for the voltage feedback control loop for 3.3V dual.
9	PWRGD	**Power Good.** Open collector output is high when all outputs are valid.
10	SLP_S3#	**SLP_S3#.** Control signal governing the Soft Off state S3. Internal current source pulls this line high if left open.
11	SLP_S5#	**SLP_S5#.** Control signal governing the Soft Off state S5. Internal current source pulls this line high if left open.
12	PWROK	**PWROK.** Control signal for switches. Internal current source pulls this line high if left open.
13	SS	**Softstart.** Attach a capacitor to this pin to determine the softstart rate.
14	GND	**Ground.** Connect this pin to ground.
15	RAMBUSFB	**2.5V feedback.** Pin 15 is used as the input for the voltage feedback control loop for 2.5V dual (RAMBUS), and also sources 2.5V dual in standby.
16	RAMBUSOUT	**2.5V base drive control.** Attach this pin to an NPN transistor powering 2.5V dual (RAMBUS) from the 3.3V main supply.
17	5VFB	**5V Voltage Feedback.** Pin 17 is used to sense undervoltage to protect the 5V dual from overcurrent.
18	5VOUT2	**5V standby gate control.** Attach this pin to a transistor powering 5V dual from the 5V standby supply.
19	5VOUT1	**5V main gate control.** Attach this pin to a transistor powering 5V dual from the 5V main supply.
20	VCCP	**Main Power.** Apply +12V through a diode on this pin to run the circuit in normal mode. Bypass with a 0.1µF capacitor. When 12V is not present, this pin produces voltage doubled 5V standby.

Absolute Maximum Ratings

All Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction to Ambient Θ_{JA}	85°C/W
Thermal Resistance Junction-to-case, Θ_{JC}	24°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
+3.3VMAIN		3.135	3.3	3.465	V
+5VMAIN		4.75	5	5.25	V
+5VSTBY		4.75	5	5.25	V
+12V		11.4	12	12.6	V
Ambient Operating Temperature		0		70	°C

Preliminary Specification

Preliminary Specification

Electrical Specifications

($V_{+5VSTBY}$ = $V_{+5VMAIN}$ =5V, $V_{+3.3V}$ = 3.3V, V_{+12V} = 12V and T_A = +25°C using circuit in Figure 3, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
+5V DUAL						
V_{Out1}, On		•	10			V
V_{Out1}, Off		•			200	mV
$V_{GS, Out2}$	Standby	•	2.7			V
V_{Out2}, Off		•			200	mV
Maximum Drive Current, Each		•	10			mA
Overcurrent Limit: Undervoltage				80		$\%V_{out}$
Overcurrent Delay Time				30		µsec
Output Driver Overlap Time	See Figure 2	•	1		5	µsec
+3.3V DUAL						
V_{Out1}, On		•	10			V
V_{Out1}, Off		•			200	mV
Total Output Voltage Variation[1]	3VOUT2 On	•	3.135	3.3	3.465	V
Maximum Drive Current		•	100			mA
Minimum Load Current	3VOUT2 On	•			50	mA
Overcurrent Limit: Undervoltage				80		%Vout
Overcurrent Delay Time				30		µsec
Output Driver Deadtime	See Figure 2: Main → Standby	•	2		6	µsec
	: Standby → Main	•	200		1000	nsec
+2.5V DUAL						
I_B, On	RAMBUSOUT On	•	200			mA
I_{Out}	RAMBUSOUT Off	•	144			mA
Total Output Voltage Variation[1]		•	2.375	2.5	2.625	V
Overcurrent Limit				80		%Vout
Overcurrent Delay Time				30		µsec
Output Driver Overlap Time	See Figure 2	•	1		5	µsec
+3.3V SDRAM						
V_{out}, On		•	10			V
V_{out}, Off		•			200	mV
I_{Out}	SDRAMOUT Off	•	100			mA
Overcurrent Limit				80		%Vout
Total Output Voltage Variation[1]	SDRAMFB On	•	3.135	3.3	3.465	V
Overcurrent Delay Time				30		µsec
Output Driver Dead Time		•	200		1500	nsec
Common Functions						
PWRGD Threshold				80		%Vout
PWRGD Delay Time				30		µsec
PWRGD Sink Current		•	1			mA
Charge Pump Frequency				200		KHz
+5VSTBY UVLO				4.5		V
+5VSTBY UVLO Hysteresis				0.5		V

Electrical Specifications (continued)

($V_{+5VSTBY}$ = $V_{+5VMAIN}$ =5V, $V_{+3.3V}$ = 3.3V, V_{+12V} = 12V and T_A = +25°C using circuit in Figure 3, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
+12V UVLO				7.5		V
+12V UVLO Hysteresis				1		V
+5VSTBY Current	MAIN Power Present			10	25	mA
+12V Current				2.5	10	mA
Input Logic HIGH		•	2.0			V
Input Logic LOW		•			0.8	V
Softstart Current				10		µA
Control Line Input Current	SLP_S5#, SLP_S3#, PWROK	•			10	µA
Over Temperature Shutdown				150		°C

Note:
1. Voltage Regulation includes Initial Voltage Setpoint and Output Temperature Drift.

Table 1. Static Power Descriptors

PWROK	SLP_S3#	SLP_S5#	Main	5 & 3.3V Duals	2.5V Dual/3.3V SDRAM	State
0	0	0	OFF	ON	OFF	S5
0	0	1	OFF	ON	ON	S3
1	0	0	OFF	ON	OFF	S0 → S5
1	0	1	OFF	ON	ON, Powered from STBY	S0 → S3
1	1	1	ON	ON	ON, Powered from MAIN	S0

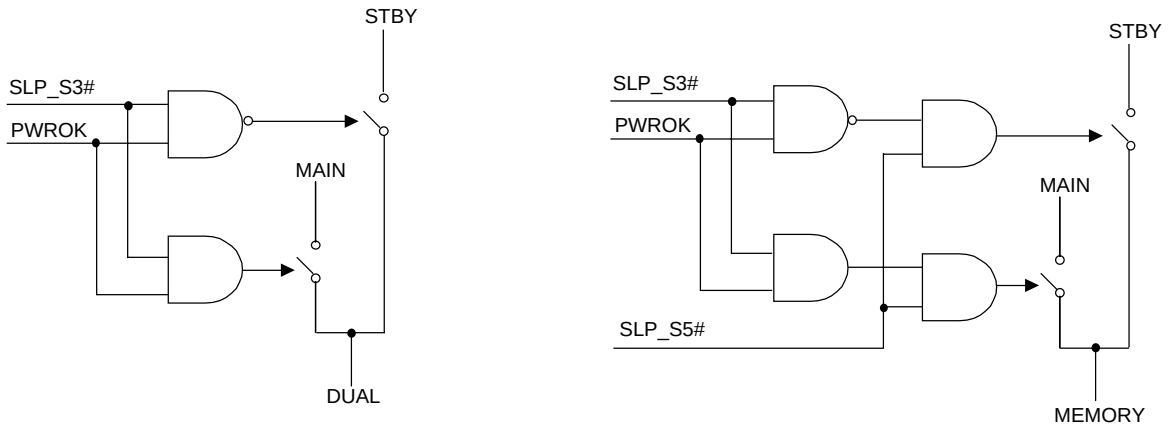


Figure 1. Control Logic for Dual Voltages and Memory Voltages

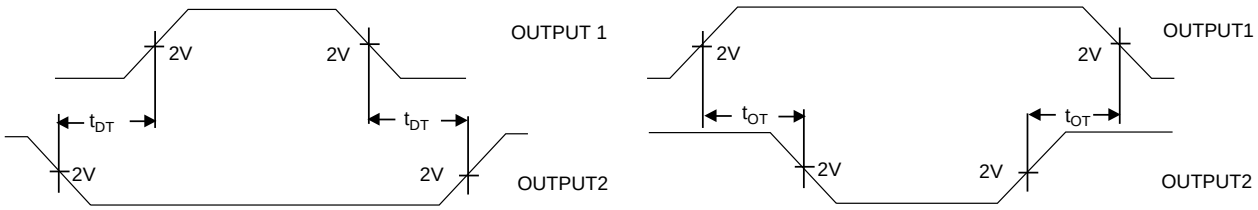


Figure 2. Deadtime and Overlap Time Measurements

Application Circuits

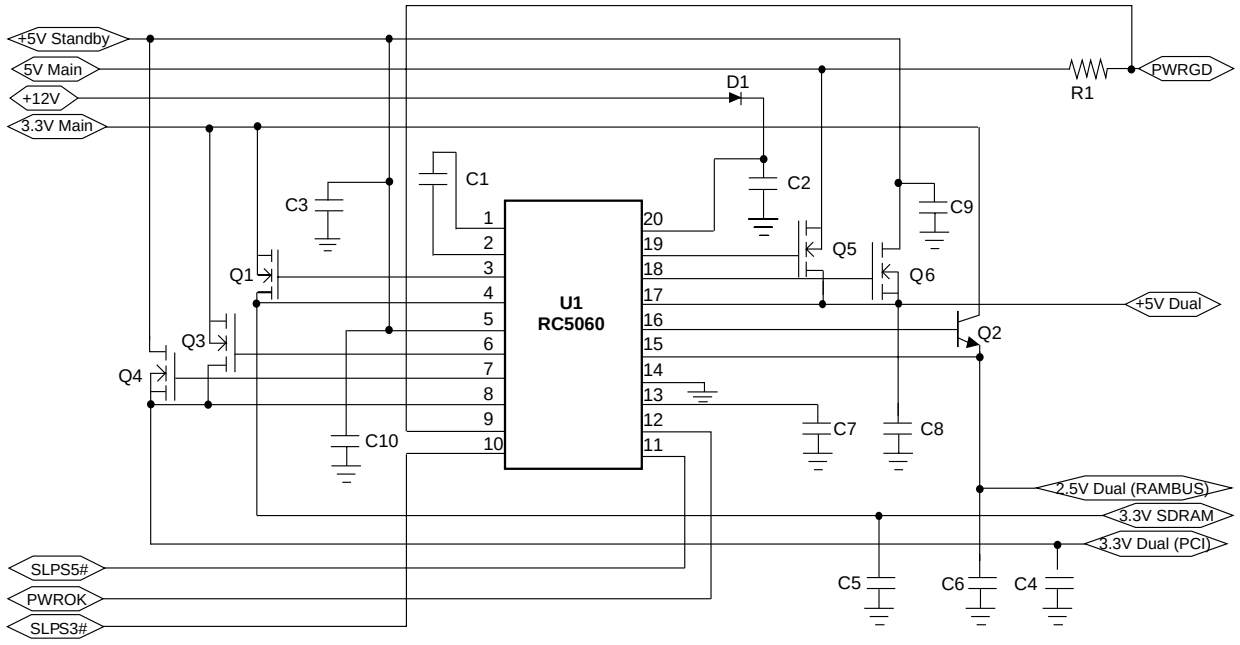


Figure 3. Camino ACPI Selector

Table 2. RC5060 Application Bill of Materials for Camino

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-3, C8	Various	4	100nF, 25V	Ceramic
C4–6, C9	Various	4	220µF, 6V	Tantalum, ESR ~ 0.1Ω
C7	Various	1	10nF, 50V	Ceramic
C10	Various	1	47µF, 10V	Tantalum
R1	Various	1	10KΩ Resistor	
D1	Fairchild MBR0520L	1	20V, 1/2A Schottky	
Q1, Q3	Fairchild FDS4410DY	2	N-channel MOSFET	$R_{ds,on}$ = 20mΩ @ V_{gs} = 4.5V
Q2	Fairchild TIP41A	1	NPN	V_{CE} ~0.4V @ I_C = 2A, I_B = 100mA
Q4	Fairchild NDS9956A	1	N-channel MOSFET	$R_{ds,on}$ = 110mΩ @ V_{gs} = 4.5V
Q5-6	Fairchild NDH833N	2	N-channel MOSFET	$R_{ds,on}$ = 25mΩ @ V_{gs} = 2.7V
U1	Fairchild RC5060	1	ACPI Switch Controller	

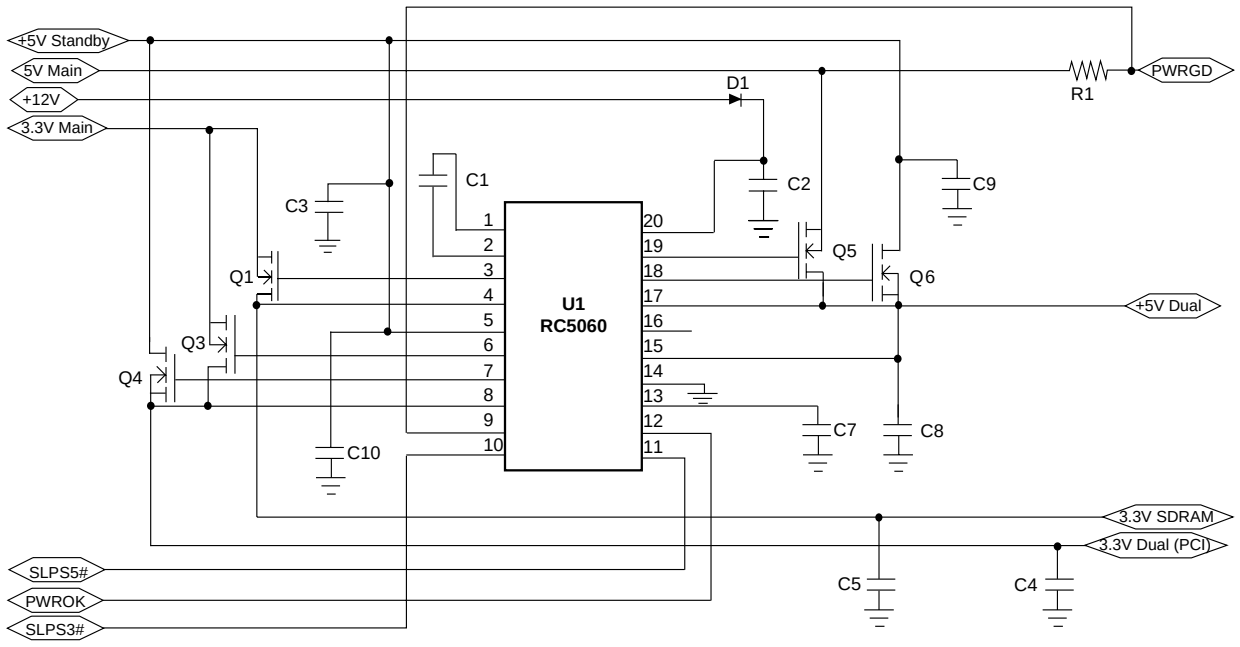


Figure 4. Whitney ACPI Selector

Table 3. RC5060 Application Bill of Materials for Whitney

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-3, C8	Various	4	100nF, 25V	Ceramic
C4-5, C9	Various	3	220µF, 6V	Tantalum, ESR ~ 0.1Ω
C7	Various	1	10nF, 50V	Ceramic
C10	Various	1	47µF, 10V	Tantalum
R1	Various	1	10KΩ Resistor	
D1	Fairchild MBR0520L	1	20V, 1/2A Schottky	
Q1, Q3	Fairchild FDS4410DY	2	N-channel MOSFET	$R_{ds,on}$ = 20mΩ @ V_{gs} = 4.5V
Q4	Fairchild NDS9956A	1	N-channel MOSFET	$R_{ds,on}$ = 110mΩ @ V_{gs} = 4.5V
Q5-6	Fairchild NDH833N	2	N-channel MOSFET	$R_{ds,on}$ = 25mΩ @ V_{gs} = 2.7V
U1	Fairchild RC5060	1	ACPI Switch Controller	

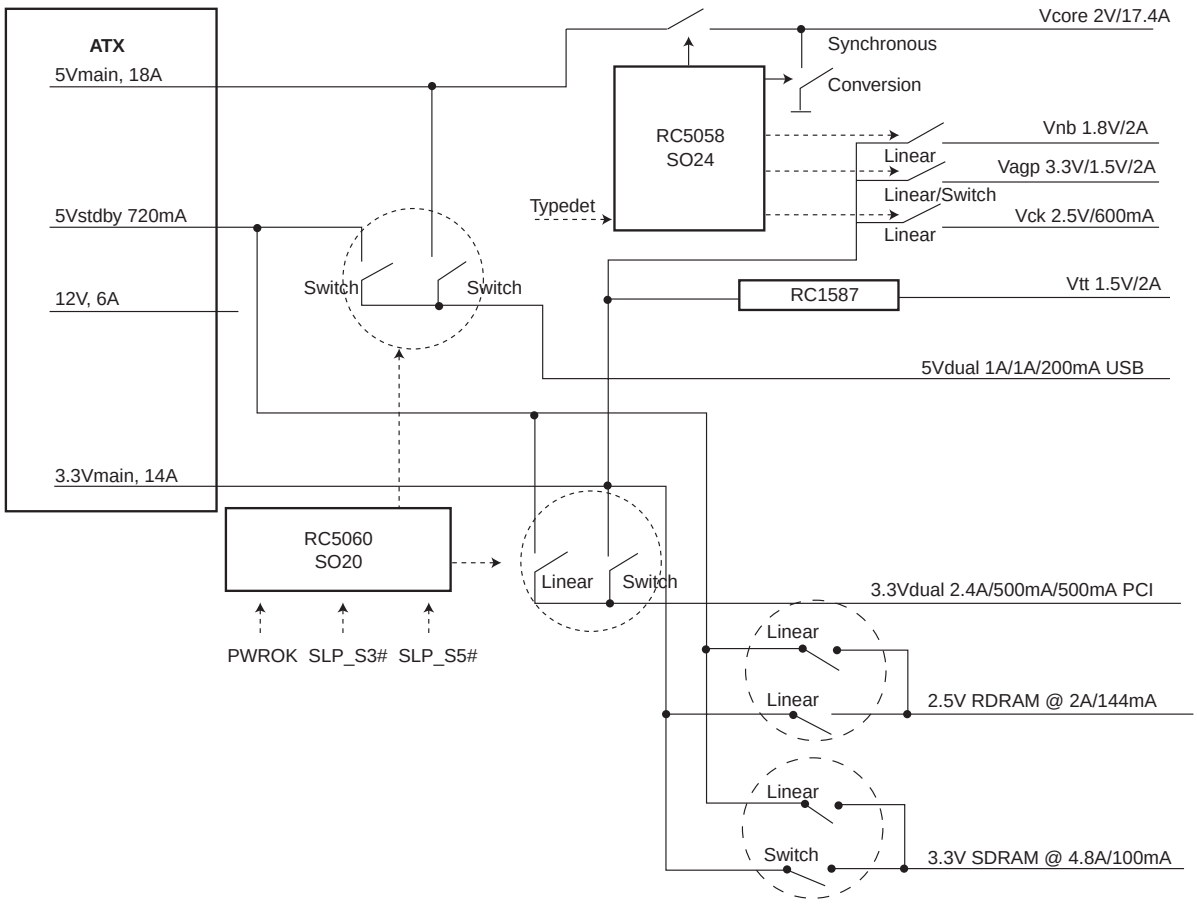


Figure 5. Camino System Architectural Block Diagram (Power Paths Only)

Application Information

The RC5060 Controller

The RC5060 is a fully compliant ACPI controller IC. Used with an ATX power supply, it generates a 5V Dual voltage, a 3.3V Dual for PCI, and power for both SDRAM and RAMBUS, and has a large array of additional protection functions integrated in. Used in conjunction with Fairchild's RC5058, it provides the complete set of control and power functions necessary to implement a Camino or Whitney motherboard.

Overview of ACPI

The Advanced Configuration and Power Interface, or ACPI, is a system for controlling the use of power in a computer. It enables the computer manufacturer and the computer user to determine the computer's power usage dynamically. For example, when the computer has been unused for a certain time, the monitor and peripherals could be turned off, and their states saved to memory. After a longer period, the processor could be turned off, and the memory saved to disk. A peripheral could then re-awaken the entire system on the occurrence of an event, such as the arrival of a FAX on a modem.

As shown in Figure 5, the available power inputs to the computer system from the ATX power supply are +5V main, +12V main, +3.3V main, and +5V standby. "Main" means that these power outputs are available under full-power operation of the system, but can be turned off in some of the power-saving modes. "Standby" means that this power output is always present.

The most general ACPI system requires four dual outputs: 5V dual, 3.3V dual, 3.3V SDRAM, and 2.5V RAMBUS (or 2.5V dual). "Dual" means that the power can be (but is not necessarily) present whether the main power supplies are present or not. To ensure the presence of these outputs, while not overloading the standby power, they have dual inputs, from both main power and standby. The presence or absence of the dual outputs is determined by the control signals to the RC5060.

ACPI States

As shown in Table 1, there are three ACPI states that are of primary concern to the system designer, designated S0, S3 and S5. S0 is the full-power state, the state of the computer when it is being actively used. The other two states are sleep states, reflecting differing levels of power-down.

S3 is a state in which the processor is powered down, but its last state is being preserved in IC memory, which is kept on. Since memory is fast, the computer can quickly come back up to full operation. However, this state continues to draw moderate power, due to the memory being kept

S5 is a state in which memory is off, and the last state of the processor has been written to the hard disk. Since the disk is slow, the computer takes longer to come back to full operation. However, since memory is off, this state draws minimal power.

It is anticipated that only the following state transitions will occur: S0 → S3, S0 → S5, S3 → S5, S5 → S0, and S3 → S0; the transition S5 → S3 will not occur, as going from save-to-disk to save-to-memory will not be activated by any mechanism.

5V Dual Output

The RC5060 controls four separate dual outputs, the first of which is the 5V dual. This output is intended to run subsystems such as the USB ports. A typical application that would require the use of 5V dual rather than +5V main for a USB port would be the use of a USB mouse: if the system needs to be able to awaken from sleep when the mouse is moved, then the mouse must be powered from dual, because main power is off.

5V dual is generated by two MOSFET switches, one from +5V main, the other from +5V standby, as shown in Figures 3 or 4. When main power is present, the first switch is on and the second off, and the opposite when main power is absent. Note carefully the polarity of the MOSFET Q5 that delivers power from the +5V main to the 5V dual: opposite to the connection of Q6, the source is connected to the +5V main input, and the drain is connected to the 5V dual output. This connection must be done this way because of Q5's body diode. When +5V main is not present, 5V dual is still on, and if Q5 were connected with the same polarity as Q6, the dual voltage would conduct through the body diode of Q5, attempting to power up the entire +5V main line. It is to avoid this overload that Q5 must be connected as shown.

The state of the switches is controlled by the SLP_ S3# and PWROK lines, as shown in Figure 1. When both SLP_ S3# and PWROK are asserted, the main switch is on, and the standby switch is off. If either line is de-asserted, the main switch is off and the standby switch is on.

Note that Q5 and Q6 should be low-gate-voltage type MOSFETs, with guaranteed operation at 2.7V V_{gs}, in order to ensure full enhancement in worst case. In a typical system, it is anticipated that full-power current will be about 1A maximum, and standby current will be about 200mA maximum.

3.3V Dual Output

The 3.3V dual output is intended to power subsystems such as the computer's PCI slots. A typical application that would require the use of 3.3V dual rather than +3.3V main for a PCI slot would be the use of a modem: if the system needs to be able to awaken from sleep when the modem receives incoming data, then that slot must be powered from dual, because main power is off. Other slots not requiring dual power can be configured using the control signals.

3.3V dual is generated by two MOSFETs, one from +3.3V main, the other from +5V standby, as shown in Figures 3 or 4. When main power is present, the MOSFET Q3 is turned on as a switch, so that input and output are connected together. When main power is absent, the MOSFET Q4 is controlled by the RC5060 as a linear regulator, generating a regulated 3.3V from +5V standby. As with the 5V dual, the MOSFET Q3 must be connected as shown in the figures, to avoid back-feed.

The state of the MOSFETs is controlled by the SLP_S3# and PWROK lines, as shown in Figure 1. When both SLP_S3# and PWROK are asserted, the main switch is on, and the linear regulator is off. If either line is de-asserted, the main switch is off and the linear regulator is on.

Q3 and Q4 as shown in Tables 2 or 3 have different $R_{DS,on}$ ratings. In a typical system, it is anticipated that full-power current will be about 2.4A maximum, and standby current will be about 500mA maximum. The difference in maximum currents means that Q4 can be a less expensive device than Q3.

3.3V SDRAM Output

3.3V SDRAM output is intended to provide power to SDRAM memory. Most systems will use this power. Those systems using RAMBUS may also use the SDRAM power, possibly piped to the same slots, to ensure backward compatibility or even mixed operation of SDRAM with RAMBUS.

3.3V SDRAM is generated by one external MOSFET switch from +3.3V main, and one linear regulator internal to the RC5060 from +5V standby, as shown in Figures 3 or 4, and in the block diagram on the front page. When main power is present, the MOSFET Ql is turned on as a switch, so that input and output are connected together. When main power is absent, the internal linear regulator is on, generating a regulated 3.3V from +5V standby. As with the other duals, the MOSFET Ql must be connected as shown in the figures, to avoid back-feed.

The state of the external MOSFET and the internal linear regulator is controlled by the SLP_S3# and PWROK lines, and additionally the SLP_S5# line, as shown in Figure 1. When SLP_S5# is de-asserted, both the external MOSFET and the internal linear regulator are off, and there is no output voltage on the 3.3V SDRAM line.

If the SLP_S5# line is asserted, the 3.3V SDRAM output is on. In this condition, if either the SLP_S3# or the PWROK line, or both, are de-asserted, the linear regulator is on and the MOSFET is off. Only in the case if both the SLP_S3# and the PWROK lines are asserted, the MOSFET is on and the linear regulator is off.

In a typical system, it is anticipated that standby current will be about 100mA maximum. Full power current will be as high as 4.8A maximum, so that Ql must have a low $R_{DS,on}$ in order to prevent excessive voltage drop across it.

2.5V Dual Output

The 2.5V dual output is intended to provide power to RAMBUS memory. Only high-end systems will use this power. Those systems using RAMBUS may also use the SDRAM power, possibly piped to the same slots, to ensure backward compatibility or even mixed operation of SDRAM with RAMBUS.

2.5V dual is generated by one external NPN bipolar acting as a linear regulator from +3.3V main, and one linear regulator internal to the RC5060 from +5V standby, as shown in Figure 3, and in the block diagram on the front page. When main power is present, the NPN Q2 linear regulates, and when main power is absent, the internal linear regulator is on. Q2 cannot be substituted with a MOSFET. If used in one direction, the MOSFET's body diode would permit backfeed; if used in the other direction, it would short-circuit the linear regulator action.

2.5V dual output is controlled in the same way and by the same lines as the 3.3V SDRAM output. In a typical system, it is anticipated that standby current will be a maximum of 144mA, and full-power current may be as high as 2A. This places some significant constraints on the selection of Q2. Since its input may be as low as (3.3V - 5%) = 3.135V, there is only 3.135V -2.5V = 635mV of V_{CE} headroom for its operation as a linear regulator. For this reason the RC5060 can provide up to 200mA of steady-state base current. The TIP41 device shown has a sufficiently low $V_{CE,\ sat}$ to guarantee worst-case regulation even at 2A I_E with this base current.

RC5060 ACPI Control Lines

As already discussed, the RC5060 outputs are controlled by the three ACPI control lines, SLP_S3#, SLP_S5# and PWROK, as summarized in Table 1. System designers must in particular be careful to ensure that their system is designed with SLP_S5#, not SLP_S5#; if SLP_S5 is used, it must be inverted before being used with the RC5060.

The control lines have internal pull-ups of approximately 10µA, and so can be controlled by open collector drivers if desired. In a noisy system, it may be desirable to filter these lines, which can be done with a 1KΩ resistor and a small capacitor.

RC5060 Dynamic Operation

The RC5060 is designed to minimize the output capacitance required to hold up the various output lines during transitions between different states. Thus in particular, the 5V dual and 2.5V dual outputs have guaranteed minimum overlap times, the time (as shown in Figure 2) during a state transition during which both main and standby are connected to the output. This overlap time guarantees that a power source is always connected to the output, so that there will be no dip in the output voltage during state transitions. There is also a maximum overlap time, to ensure that the standby power doesn't have to source main power very long, thus minimizing thermal stress on the standby device.

The 3.3V dual and 3.3V SDRAM are different than the other outputs, because they are powered by both a linear regulator and a switch. If the linear regulator were to turn on while the switch is on (or vice versa) the linear regulator would supply power to the main line through the switch. For this reason, the linear regulator must be off before the switch is on, and vice versa. Thus, these two outputs have guaranteed minimum deadtime when both linear regulator and switch are off. During this time, the output capacitors must hold up the load, and so there is also a specified maximum deadtime, allowing a maximum necessary capacitance to be selected, see below.

Stability

As with all linear regulators, the RC5060's linear regulators require a minimum load. With the exception of the 3.3V dual output, however, all of these minimum loads are internal to the RC5060. The 3.3V dual output requires a minimum load of 50mA; if a situation may occur in which the load is less than 50mA, additional steps may be necessary to ensure stability.

Furthermore, depending on location, it may be necessary to bypass the drain (or collector) of the linear regulator with a low ESR capacitor for stability. As a rule of thumb, if the pass element is more than 1" from its power source, it should have a bypass.

Softstart

Pin 13 of the RC5060 functions as a softstart. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of the RC5060. providing a softstart for the linear regulators. The actual state of the RC5060 on power up will be determined by the state of its control lines.

The switches in the system must be either on or off, and so softstart has no effect on their characteristics: if the appropriate control signals are asserted, they will turn on at once.

The softstart is effective only during power on. During a transition between states, such as from S5 → S0, the linear regulators are not softstarted.

It is important to note that the softstart pin is not an enable; pulling it low will not necessarily turn off all outputs.

Charge Pump

In main power operation, the RC5060 is run from the +12V main supply. This supply also provides voltage to the various MOSFET gates. However, during standby, this supply is off. To provide power to the chip and the appropriate gates, the RC5060 incorporates a free-running charge pump. As shown in Figures 3 and 4, and in the block diagram on the front page, a capacitor attached between pins 1 and 2 of the RC5060 acts as a charge pump with internal diodes. The charge pump output is internally diode or'red with the 12V input. The 12V input must have a series diode to prevent back-feeding the charge pump to the + 12V main when in standby. The 12V input line needs a bypass capacitor for high-frequency noise rejection.

Overcurrent

The RC5060 does not directly detect current through the eight devices that power its outputs. Instead, it monitors the four output voltages. In the event of a hard short, the voltage drops below 80% of nominal, and all outputs are latched off, and remain off until 5V standby power is recycled. The overcurrent latch off is delayed by 30µsec to prevent nuisance trips.

During softstart, the overcurrent voltage monitors are kept proportional to the reference, to avoid tripping overcurrent during startup. The monitors are kept active during softstart, to avoid turning on into a short.

In the S5 state, when the memory outputs are off, the voltage monitors on the memory lines are disabled, to prevent tripping the overcurrent. When turning these lines back on from the S5 state, the delay prevents overcurrent from tripping.

If the 2.5V dual is not used, its feedback line, pin 15, must be connected to 5V dual as shown in Figure 4, to prevent an overcurrent trip.

UVLO

If the +5V standby is below approximately 4.5V, the RC5060 will leave off or turn off all outputs. Similar comments apply to the +12V main at 7.5V. The +5V standby UVLO has approximately 0.5V hysteresis, the +12V main UVLO 1V.

Power Good

The Power Good is an open collector that pulls low if any of the outputs are less than 80% of nominal.

Over Temperature

The RC5060 is capable of sourcing substantial current, 200mA minimum to the RAMBUS transistor's base during S0, 144mA to the RAMBUS line during S3, and 100mA to SDRAM during S3. As a result, there can be heavy power dissipation in the IC. While the RC5060 is designed to accept this power dissipation, any overloading of outputs can cause excessive heating. If the RC5060 die temperature exceeds about 150°, all outputs are shut off. Outputs remain off until the die temperature returns to its safe area.

Transistor Selection

External transistor selection depends on usage, differing for the linear regulators and the switches.

The MOSFET switches, Ql, Q3, Q5 and Q6 should be sized based on regulation requirements and power dissipation. Since the ATX outputs are ±5%, the outputs driven from them must be wider. As an example, if we want to hold 3.3V SDRAM to -10%, we can drop only 5% = 165mV across Q1. At 4.8A, this means Ql must have a maximum $R_{DS,on}$ of 165mV/4.8A = 34mΩ, including tolerance and self-heating effects. We thus choose a Fairchild FDS4410Y, which has 20mΩ maximum $R_{DS,\ on}$ at 4.5V V_{GS} at 25°C. We can estimate power dissipation as $(4.8A)^2 * 20m\Omega = 460mW$, which should be acceptable for this package. Similar calculations apply to the other MOSFET switches.

Q4 is a MOSFET functioning as a linear regulator. Since it delivers only 500mA, it is easy to select a MOSFET, it need only have $R_{DS,on}$ less than (5V–5%–3.3V)/500mA = 2.9Ω. We select the Fairchild NDS9956A which has maximum $R_{DS,\ on}$ of 110mΩ at 4.5V V_{GS} at 25°C. Power dissipation will be a maximum of $(0.5A)^2 * 110m\Omega = 27mW$.

Q2 is an NPN bipolar functioning as a linear regulator. As already discussed, it must have a $V_{CE,sat}$ lower than 635mV at I_E = 2A and I_B = 200mA. Its power dissipation can be as high as (3.3V + 5%–2.5V) * 2A = l.9W.

Output Capacitor Selection

Output capacitor selection depends on whether the line has overlap time or not.

For both the 5V dual and the 2.5V dual, there is guaranteed overlap time between when one source is turned on and the other source turned off. For these outputs, the output capacitor is not needed to hold up the supply, but only for noise filtering and to respond to transient loading.

The 3.3V dual and 3.3V SDRAM outputs have deadtime between when one source is turned off and the other source turned on. During the time when both are off, the output current must be supplied by the output capacitor. Mitigating this, it must be realized that the system will be designed in such a way that the current has gone to its sleep value before the transition occurs. For example, the 3.3V dual has a sleep current of 500mA maximum. Maximum deadtime is 6µsec, and so charge depletion is 500mA * 6µsec = 3µC. Suppose that we have a total of 8% drop due to the source tolerance and the MOSFET drop, and we are trying to hold 10% regulation. The remaining 2% = 66mV implies a minimum capacitance of 3µC/66mV = 45µF.

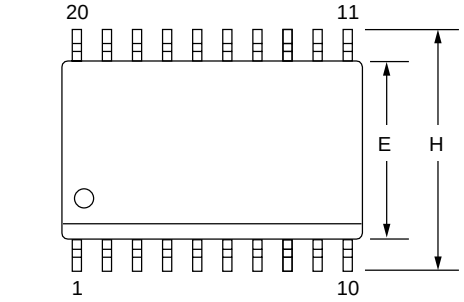
Mechanical Dimensions

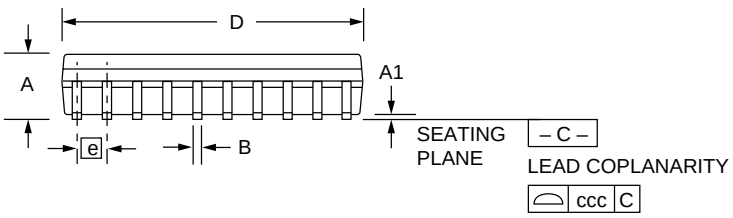
20 Lead SOIC

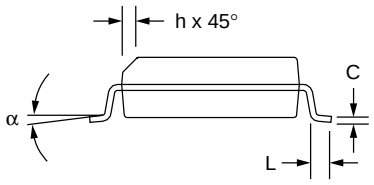
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Specification

Ordering Information

Product Number	Package
RC5060M	20 pin SOIC

Preliminary Specification