RC7108

133MHz Spread Spectrum Clock for Motherboards

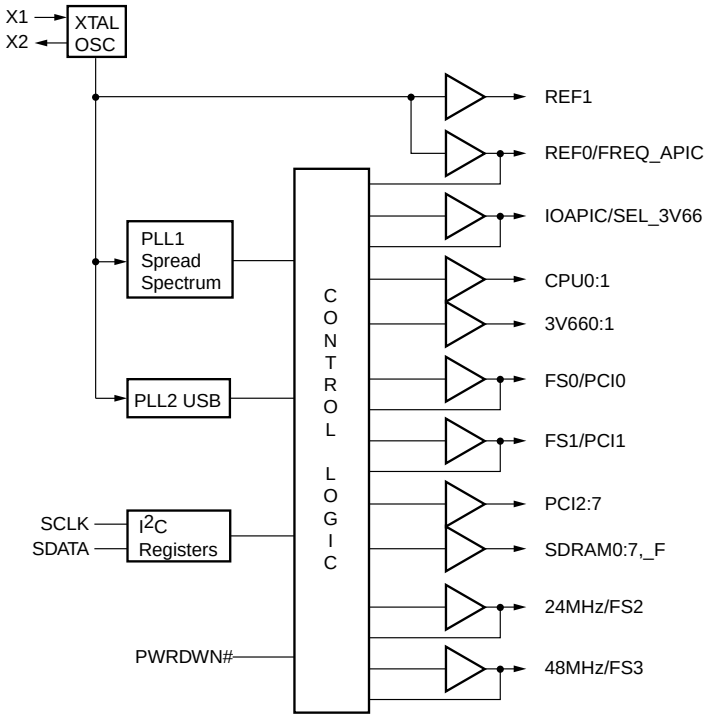
Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 150MHz
- Two skew-controlled copies of the CPU clock
- I^2C programmable
- Two copies of 3V66 clock
- One copy 24MHz clock
- One copy 48MHz clock
- One copy IOAPIC
- Two copy REF 14.318MHz clock (3.3V)
- Eight copies PCI clock
- Nine copies of SDRAM clock with one Free-running
- Power down capability

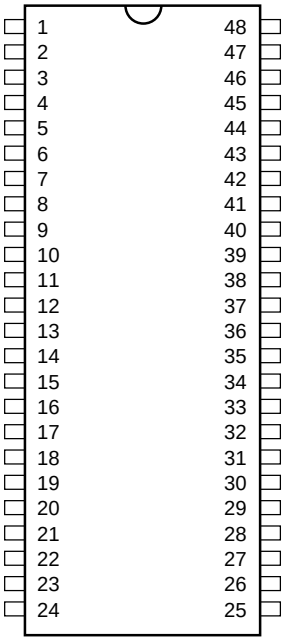
Description

The RC7108 is a clock synthesizer for motherboard applications. It meets the requirements for 133MHz Whiting chipset. The clock frequencies can be set with the 4 select pins and/or be set via the I^2C interface.

Block Diagram



Pin Assignments



Pin Assignments

Pin #	Pin Name	Pin #	Pin name	Pin #	Pin Name
1	REF1	17	PCI5	33	VSS
2	VDD	18	VDD	34	SDRAM5
3	X1	19	PCI6	35	SDRAM4
4	X2	20	PCI7	36	SDRAM3
5	VSS	21	VSS	37	VDD
6	VSS	22	PWRDWN#	38	SDRAM2
7	3V66-0	23	SCLK	39	SDRAM1
8	3V66-1	24	SDATA	40	SDRAM0
9	VDD	25	VDD	41	VSS
10	VDD	26	48MHz/FS3	42	VSSL
11	FS0/PCI0	27	24MHz/FS2	43	CPU1
12	FS1/PCI1	28	VSS	44	CPU0
13	PCI2	29	VDD	45	VDDL
14	VSS	30	SDRAM_F	46	IOAPIC/SEL_3V66
15	PCI3	31	SDRAM7	47	VDDL
16	PCI4	32	SDRAM6	48	REF0/FREQ_APIC

PWRDWN#

PWRDWN#	CPU	SDRAM	IOAPIC	3V66	PCI	REF, 24MHz, 48MHz	OSC.	PLL
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Frequency Selection

FS3	FS2	FS1	FS0	CPU MHz	SDRAM MHz	PCI MHz	3V66 (MHz)		IOAPIC (MHz)	
							3V66_SYNC =0	3V66_SYNC =1	FREQ_APIC =0	FREQ_APIC =1
0	0	0	0	100.3	100.3	33.3	66.6	66.6	16.67	33.3
0	0	0	1	100.9	100.9	33.67	67.34	67.34	16.84	33.67
0	0	1	0	105	105	35	70	70	17.5	35
0	0	1	1	115	115	38.33	64*	76.66	19.17	38.33
0	1	0	0	120	120	40	64*	80	20	40
0	1	0	1	124	124	41.33	64*	82.66	20.67	41.33
0	1	1	0	133.3	133.3	44.33	64*	88.66	22.17	44.33
0	1	1	1	133.3	133.3	33.3	66.6	66.6	16.67	33.3
1	0	0	0	140	140	35	70	70	17.5	35
1	0	0	1	150	150	37.5	64*	75	18.75	37.5
1	0	1	0	66.8	100.2	33.4	66.6	66.6	16.67	3.3
1	0	1	1	70	105	35	70	70	17.5	35
1	1	0	0	75	112.5	37.5	64*	75	18.75	37.5
1	1	0	1	83.3	124.5	41.5	64*	83	20.75	41.5
1	1	1	0	90	90	30	60	60	15	30
1	1	1	1	95	95	31.67	63.34	63.34	15.84	31.67

***Note:** These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
CPU0:1	44,43	OUT	CPU Clock Outputs: These two CPU clocks are determined by the 4 select pins FS0:3
PCI2:7	13,15,16, 17,19,20	OUT	PCI BUS Clock Outputs: These 6 PCI clock outputs run synchronously to the CPU.
PCI0/FS0	11	OUT/IN	I/O Dual Function PCI0 and FS0 pin: See table for frequency selection. After power-on, this pin becomes a normal PCI clock.
PCI1/FS1	12	OUT/IN	I/O Dual Function PCI1 and FS1 pin: See table for frequency selection. After power-on, this pin becomes a normal PCI clock.
3V66-0:1	7,8	OUT	3V66 Clock Outputs: These 2 outputs are fixed at 66MHz operating from 3.3V.
REF1	1	OUT	REF Clock Output: This output provides a 14.318MHz high drive clock .
REF0/ FREQ_APIC	48	OUT/IN	I/O Dual Function REF0 and FREQ_APIC Pin: During power-up, if the input is “0”, the IOAPIC output would operate at 16.67MHz. If the input is latched “1”, the IOAPIC output would operate at 33.3MHz. After power-on, this pin becomes a REF0 output. There is an internal pull-up resistor on this pin.
IOAPIC/ SEL_3V66	46	OUT/IN	I/O Dual Function IOAPIC and SEL_3V66 Pin: See table for frequency selection.
SDRAM0:7 SDRAM_F	40,39,38,36, 35,34,32,31, 30	OUT	SDRAM Clock Outputs: SDRAM0:7 clocks are determined by FS0:FS3. SDRAM_F is a free-running clock which is not controlled by the I^2C.
24MHz/FS2	27	OUT/IN	I/O Dual Function 24MHz and FS2 pin: See table for frequency selection. After power-on the pin becomes a normal 24MHz clock.
48MHz/FS3	26	OUT/IN	I/O Dual Function 48MHz and FS3 pin: See table for frequency selection. After power-on the pin becomes a normal 48MHz clock.
X1	3	IN	Crystal Connection: An input connection for an external14.318MHz crystal. If using an external reference, this pin must be left unconnected.
X2	4	OUT	Crystal Connection or External Reference Frequency Input: Connect to either a 14.318MHz crystal or other reference signal.
PWRDWN#	22	IN	Power-down Input pin: This pin shuts down the clock PLL bring all clocks to a low state.
SCLK	23	IN	I^2C Clock Pin: The I^2C clock should be applied to this input as described in the I^2C section of this datasheet.
SDATA	24	IN/OUT	I^2C Data Pin: Data should be presented to this input as described by the I^2C section of this datasheet. There is an internal pull-up resistor on this pin.
VDD	2,9,10,18,25, 29,37	POWER	3.3V Power Pins:
VDDL	45,47	POWER	2.5V Power Pins:
VSS	5,6,14,21,28, 33,41,42	POWER	Ground Pins:

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 11 FS0/PCI0, act as a logic input upon power up. This allows the determination of assigned device function. For this example, FS0 along with the other three select pins will determine the clock frequencies as shown in the table. A short time after power up, the logic state is latched and the pin becomes a clock output pin. In this case, pin 11 becomes a PCI clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10kohm “strapping” resistor is connected between the I/O pin and VDD or VSS (ground). A connection to ground sets a “0” bit and a connection to VDD sets a “1” bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic “0” or “1” condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when VDD reaches 2.0V. The input bits can only be reset by turning the VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

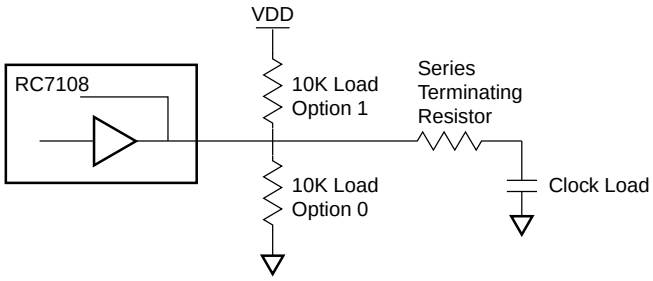


Figure 1. Input Logic Selection through Resistor Load Option

Serial Data Interface

The RC7108 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7108 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLK. In motherboard applications, SDATA and SCLK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 133MHz provided upon power-on. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

The RC7108 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7108 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7108 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7108, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7108, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 5	The data bits in these bytes set internal RC7108 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function except for the “reserved bits”. These must be preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 1-4.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 7 shows the mode select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 1-4 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 1						
7	-	-	(Reserved)	-	-	0
6	-	-	(Reserved)	-	-	0
5	-	-	(Reserved)	-	-	0
4	27	24MHz	Clock Output Disable	Disable	Enable	1
3	26	48MHz	Clock Output Disable	Disable	Enable	1
2	-	-	(Reserved)	-	-	0
1	-	-	(Reserved)	-	-	0
0	-	-	(Reserved)	-	-	0
Data Byte 2						
7	31	SDRAM7	Clock Output Disable	Disable	Enable	1
6	32	SDRAM6	Clock Output Disable	Disable	Enable	1
5	34	SDRAM5	Clock Output Disable	Disable	Enable	1
4	35	SDRAM4	Clock Output Disable	Disable	Enable	1
3	36	SDRAM3	Clock Output Disable	Disable	Enable	1
2	38	SDRAM2	Clock Output Disable	Disable	Enable	1
1	39	SDRAM1	Clock Output Disable	Disable	Enable	1
0	40	SDRAM0	Clock Output Disable	Disable	Enable	1
Data Byte 3						
7	20	PCI7	Clock Output Disable	Disable	Enable	1
6	19	PCI6	Clock Output Disable	Disable	Enable	1
5	17	PCI5	Clock Output Disable	Disable	Enable	1
4	16	PCI4	Clock Output Disable	Disable	Enable	1
3	15	PCI3	Clock Output Disable	Disable	Enable	1
2	13	PCI2	Clock Output Disable	Disable	Enable	1
1	12	PCI1	Clock Output Disable	Disable	Enable	1
0	11	PCI0	Clock Output Disable	Disable	Enable	1
Data Byte 4						
7	-	-	(Reserved)	-	-	0
6	8	3V66-1	Clock Output Disable	Disable	Enable	1
5	7	3V66-0	Clock Output Disable	Disable	Enable	1
4	-	-	(Reserved)	-	-	0
3	46	IOAPIC	Clock Output Disable	Disable	Enable	1
2	-	-	(Reserved)	-	-	0
1	43	CPU1	Clock Output Disable	Disable	Enable	1
0	44	CPU0	Clock Output Disable	Disable	Enable	1

Table 5. Byte 0: Functionality and frequency select register (Default = 0)

Bit	Description								Default
Bit 7	0- ±0.25% Center Spread Spectrum								0
	1- Down Spread Spectrum 0 to -0.5%								
Bit (2, 6:4)					3V66		IOAPIC		Note 1
	Bit(2,6:4)	CPU	SDRAM	PCI	3V66_SEL =0	3V66_SEL =1	FREQ_APIC =0	FREQ_APIC =1	
	0000	100.3	100.3	33.3	66.6	66.6	16.67	33.3	
	0001	100.9	100.9	33.67	67.34	67.34	16.84	33.67	
	0010	105	105	35	70	70	17.5	35	
	0011	115	115	38.33	64*	76.66	19.17	38.33	
	0100	120	120	40	64*	80	20	40	
	0101	124	124	41.33	64*	82.66	20.67	41.33	
	0110	133.3	133.3	44.33	64*	88.66	22.17	44.33	
	0111	133.3	133.3	33.3	66.6	66.6	16.67	33.3	
	1000	140	140	35	70	70	17.5	35	
	1001	150	150	37.5	64*	75	18.75	37.5	
	1010	66.8	100.2	33.4	66.6	66.6	16.67	3.3	
	1011	70	105	35	70	70	17.5	35	
	1100	75	112.5	37.5	64*	75	18.75	37.5	
	1101	83.3	124.5	41.5	64*	83	20.75	41.5	
	1110	90	90	30	60	60	15	30	
	1111	95	95	31.67	63.34	63.34	15.84	31.67	
Bit 3	0- frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,6:4								0
Bit 1	0- Normal 1- Spread Spectrum								0
Bit 0	0- Enabled 1- Tristate all outputs								0

Note 1: Default at power-up will be for latched logic inputs to define frequency, Bit 2, 6:4 are defaulted to 0000.
*These output frequencies are not synchronous to the CPU Clock and do not have Spread Spectrum modulation.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to V_{SS}	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	^{o}C
T_B	Ambient Temperature	-55 to +125	^{o}C
T_A	Operating Temperature	0 to +70	^{o}C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics

T_A = 0°C to +70°C; VDD = 3.3V±5%; VDDL = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
IDD3	Combined 3.3V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
IDD2	Combined 2.5V Supply Current	CPU = 133MHz Outputs Loaded		TBD		mA
Logic Inputs						
V_{IL}	Input Low Voltage		VSS-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+0.3	V
I_{IL}	Input Low Current[1]				-25	µA
I_{IH}	Input High Current[1]				10	µA
I_{IL}	Input Low Current				-5	µA
I_{IH}	Input High Current				5	µA
Clock Outputs[2]						
V_{OL}	Output Low Voltage	I_{OL}=1mA			0.4	V
V_{OH}	Output High Voltage CPU and IOAPIC	I_{OH}=-1mA	2.0			V
	PCI, SDRAM, 3V66, 24MHz,48MHz,REF		2.4			
I_{OL}	Output Low Current CPU	V_{OL}=1.2V	27		93	mA
	IOAPIC		40		138	
	PCI, 3V66	V_{OL}=1.4V	26.5		139	
	REF, 24MHz,48MHz		25		76	
	SDRAM		61		152	

DC Electrical Characteristics (Continued)

T_A = 0°C to +70°C; VDD = 3.3V±5%; VDDL = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
I_{OH}	Output High Current CPU	V_{OH}=1.2V	-26		-101	mA
	IOAPIC		-39		-150	
	PCI, 3V66	V_{OH}=1.4V	-31		-189	
	REF, 24MHz,48MHz		-27		-94	
	SDRAM		-68		-188	
Crystal oscillator						
V_{TH}	X1 Input Threshold Voltage[3]	VDD=3.3V		1.5		V
C_{LOAD}	Load Capacitance, as seen by external Xtal.[4]			18		pF
C_{IN}	X1 Input Capacitance[5]	X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	PF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	NH

Notes:

1. RC7108 logic inputs have internal pull-up resistors.
2. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
3. X1 input threshold voltage (typical) is VDD/2
4. The RC7108 contains an internal crystal load capacitor between X1 and VSS and another between X2 and VSS. The total load placed on the crystal is 18pF; this includes typical stray capacitance of short PCB traces to the crystal.
5. X1 input capacitance is applicable when X1 is driven with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A=0°C to 70°C; VDD=3.3V±5%; VDDL=2.5V±5%; f_{XTL}=14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (C_{LOAD}=20pF)

Parameter		CPU=133MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	7.5		8	nS	Meas. at rising edge at 1.25V.
t_H	High Time		2		nS	Duration of clock cycle above 2V.
t_L	Low Time		1.8		nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_{JC}	Jitter, Cycle to Cycle			250	pS	Measured on rising edge at 1.25V.
t_{SK}	Output Skew			175	pS	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	mS	Assumes full supply voltage reached within 1mS from power-up. Short cycles exist prior to frequency stabilization.
Z_O	AC output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI0:7 (Lump Capacitance Test Load = 30pF)

Parameter		PCI = 33.3MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
t_P	Period	30			nS	Meas. at rising edge at 1.5V.
t_H	High Time	12.0			nS	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			nS	Duration of clock cycle below 0.4V
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{JC}	Jitter, Cycle to Cycle			500	pS	Measured on rising edge at 1.5V.
t_{SK}	Output Skew			500	pS	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	nS	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.

3V66 Clock Outputs (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			500	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			250	pS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

SDRAM Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		66.6		MHz	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			250	pS	Measured on rising edge at 1.5V
t_{SK}	Output Skew			250	pS	Measured at 1.5V
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

24MHz and 48MHz Clock Outputs (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		48.008 24.004		MHz	Determined by PLL divider ratio.
f_D	Frequency deviation		+167		ppm	(48.008-48)/48
n/m			57/17, 114/17		-	
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.4		1.6	nS	0.4V to 2.0V
t_F	Output Fall Time	0.4		1.6	nS	2.0V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.25V
t_A	Jitter, Absolute			500	pS	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up			1.5	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
f	Frequency		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Time	0.5		2	nS	0.4V to 2.4V
t_F	Output Fall Time	0.5		2	nS	2.4V to 0.4V
t_D	Duty Cycle	45		55	%	Measured at 1.5V
t_{jc}	Jitter, Cycle-to-cycle			500	nS	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up			3	mS	Assumes full supply voltage reached within 1mS from power-up.
Z_O	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

Group Skews (CPU and IOAPIC load = 20pF; PCI, SDRAM, 3V66 load = 30pF)

Parameter		CPU = 133MHz			Units	Test Condition/Comment
		Min.	Typ.	Max.		
$t_{CPU-3V66}$	CPU (66.6MHz) to 3V66			500	pS	CPU @ 1.25V and 3V66 @ 1.5V Note 180^{o} offset between outputs
$t_{CPU-SDRAM}$	CPU (133MHz) to SDRAM			500	pS	CPU @ 1.25V and SDRAM @1.5V Note 180^{o} offset between outputs
$t_{3V66-PCI}$	3V66 to PCI	1.5	2.1	4	nS	3V66 and PCI @ 1.5V (prefer 2.0 to 2.5nS)
$t_{IOAPIC-PCI}$	IOAPIC to PCI			500	pS	IOAPIC @ 1.25V and PCI @ 1.5V

Mechanical Dimensions

48 pin SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.