SEFP5N05
SEFP5N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

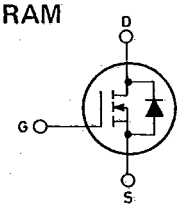
V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	0.6 Ω	5 A

ABSOLUTE MAXIMUM RATINGS

		SEFP 5N05	SEFP 5N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
I_{DM}(•)	Drain current (pulsed)	10A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	50W	
	Derating factor	0.4W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

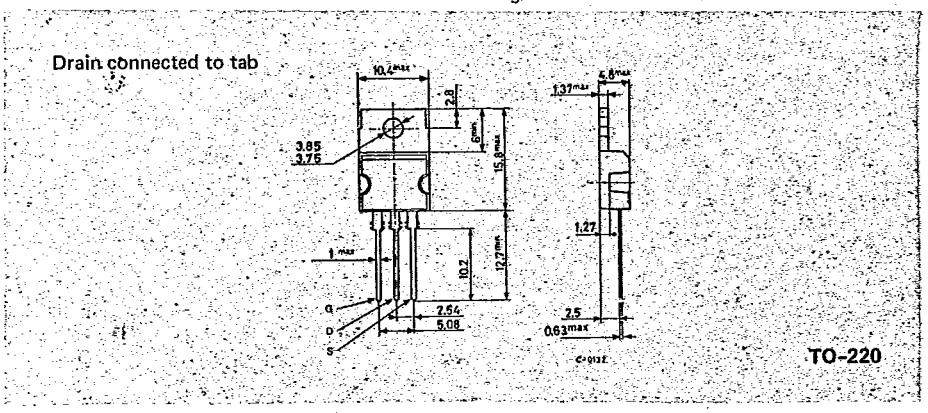
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



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THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	2.5°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 V for **SEFP5N05** for **SEFP5N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2.5 A			0.6	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10 V I_D = 5 A V_{GS} = 10V I_D = 2.5 A T_j = 100°C			3.75 3	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 2.5 A	0.75			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		180	250 100 40	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

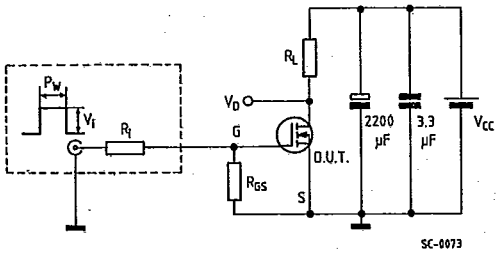
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		30		ns
t_r	Rise time	I_D = 0.5 Rated I_D		50		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		50		ns
t_f	Fall time	(see test circuit)		30		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		2.5		V
t_{on}	Forward Turn-on time			150		ns
t_{rr}	Reverse recovery time			250		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP351 Datasheet.

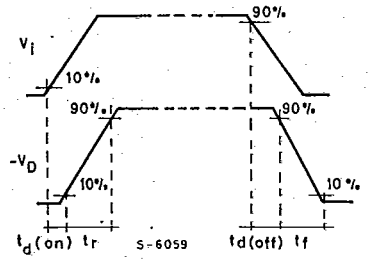
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms



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