

SSM2018T/SSM2118T*

FEATURES

- 117 dB Dynamic Range**
- 0.006% Typical THD+N (@ 1 kHz, Unity Gain)**
- 140 dB Gain Range**
- No External Trimming Required**
- Differential Inputs**
- Complementary Gain Outputs**
- Buffered Control Port**
- I-V Converter On-Chip (SSM2018T)**
- Differential Current Outputs (SSM2118T)**
- Low External Parts Count**
- Low Cost**

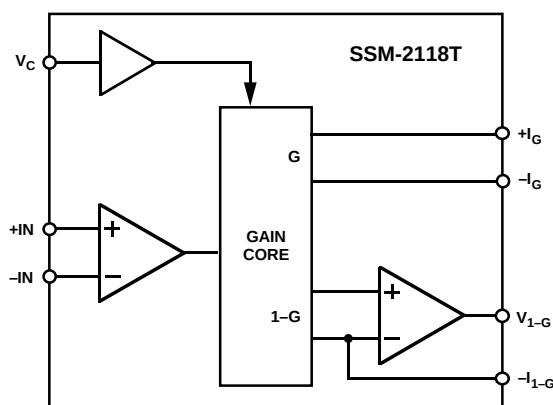
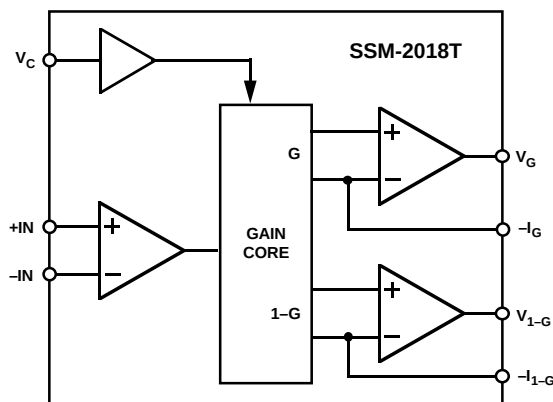
GENERAL DESCRIPTION

The SSM2018T and SSM2118T represent continuing evolution of the Frey Operational Voltage Controlled Element (OVCE) topology that permits flexibility in the design of high performance volume control systems. Voltage (SSM2018T) and differential current (SSM2118T) output versions are offered, both laser-trimmed for gain core symmetry and offset. As a result, the SSM2018T is the first professional audio quality VCA to offer trimless operation. The SSM2118T is ideal for low noise summing in large VCA based systems.

Due to careful gain core layout, the SSM2018T/SSM2118T combine the low noise of Class AB topologies with the low distortion of Class A circuits to offer an unprecedented level of sonic transparency. Additional features include differential inputs, a 140 dB gain range, and a high impedance control port. The SSM2018T provides an internal current-to-voltage converter; thus no external active components are required. The SSM2118T has fully differential current outputs that permit high noise-immunity summing of multiple channels.

Both devices are offered in 16-pin plastic DIP and SOIC packages and guaranteed for operation over the extended industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAMS



*Protected by U.S. Patent Nos. 4,471,320 and 4,560,947.

REV. A

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SSM1018T/SSM2118T—SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

[$V_S = \pm 15\text{ V}$, $A_V = 0\text{ dB}$, $R_L = 100\text{ k}\Omega$, $f = 1\text{ kHz}$, $0\text{ dBu} = 0.775\text{ V rms}$, simple VCA application circuit with $18\text{ k}\Omega$ resistors, $-V_{IN}$ floating, and Class AB gain core bias ($R_B = 150\text{ k}\Omega$), $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, unless otherwise noted. Typical specifications apply at $T_A = +25^\circ\text{C}$.]

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE¹					
Noise	$V_{IN} = \text{GND}$, 20 kHz Bandwidth		−95	−93	dBu
Headroom	Clip Point = 1% THD+N		+22		dBu
Total Harmonic Distortion plus Noise	2nd and 3rd Harmonics Only (+25°C to +85°C)				
	$A_V = 0\text{ dB}$, $V_{IN} = +10\text{ dBu}$		0.006	0.025	%
	$A_V = +20\text{ dB}$, $V_{IN} = -10\text{ dBu}$		0.013	0.04	%
	$A_V = -20\text{ dB}$, $V_{IN} = +10\text{ dBu}$ ²		0.013	0.04	%
INPUT AMPLIFIER					
Bias Current	$V_{CM} = 0\text{ V}$		0.25	1	μA
Offset Voltage	$V_{CM} = 0\text{ V}$		1	15	mV
Offset Current	$V_{CM} = 0\text{ V}$		10	100	nA
Input Impedance			4		M Ω
Common-Mode Range			± 13		V
Gain Bandwidth	VCA Configuration		0.7		MHz
	VCP Configuration		14		MHz
Slew Rate			5		V/ μs
OUTPUT AMPLIFIER (SSM2018T)					
Offset Voltage	$V_{IN} = 0\text{ V}$, $V_C = +4\text{ V}$		1.0	15	mV
Output Voltage Swing	$I_{OUT} = 1.5\text{ mA}$				
	Positive	+10	+13		V
	Negative	−10	−14		V
Minimum Load Resistance	For Full Output Swing		9		k Ω
CONTROL PORT					
Bias Current			0.36	1	μA
Input Impedance			1		M Ω
Gain Constant	Device Powered in Socket > 60 sec		−30		mV/dB
Gain Constant Temperature Coefficient			−3500		ppm/ $^\circ\text{C}$
Control Feedthrough	0 dB to −40 dB Gain Range		± 1	± 4	mV
Maximum Attenuation	$V_C = +4\text{ V}$		100		dB
POWER SUPPLIES					
Supply Voltage Range		± 5		± 18	V
Supply Current			11	15	mA
Power Supply Rejection Ratio			80		dB

NOTES

¹SSM2118T tested and characterized using OP275 as current-to-voltage converter, see figure next page.

²Guaranteed by characterization data and testing at $A_V = 0\text{ dB}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage

Dual Supply ± 18 VInput Voltage $\pm V_S$ Operating Temperature Range -40°C to $+85^{\circ}\text{C}$ Storage Temperature -65°C to $+150^{\circ}\text{C}$ Junction Temperature (T_J) $+150^{\circ}\text{C}$ Lead Temperature (Soldering, 60 sec) $+300^{\circ}\text{C}$ **THERMAL CHARACTERISTICS**Thermal Resistance²

16-Pin Plastic DIP

 θ_{JA} 76°C/W θ_{JC} 33°C/W

16-Pin SOIC

 θ_{JA} 92°C/W θ_{JC} 27°C/W **TRANSISTOR COUNT**

Number of Transistors

SSM2018T 125

SSM2118T 108

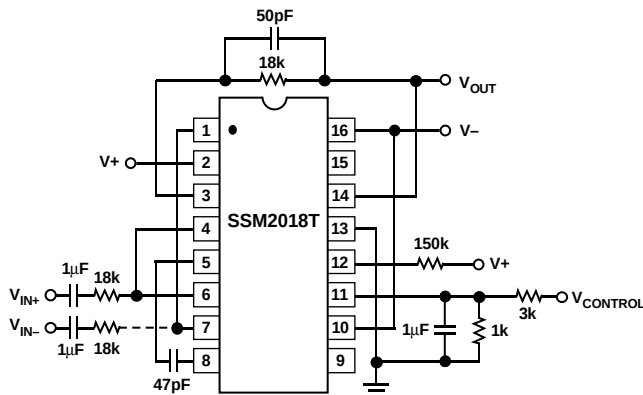
ESD RATINGS

883 (Human Body) Model 500 V

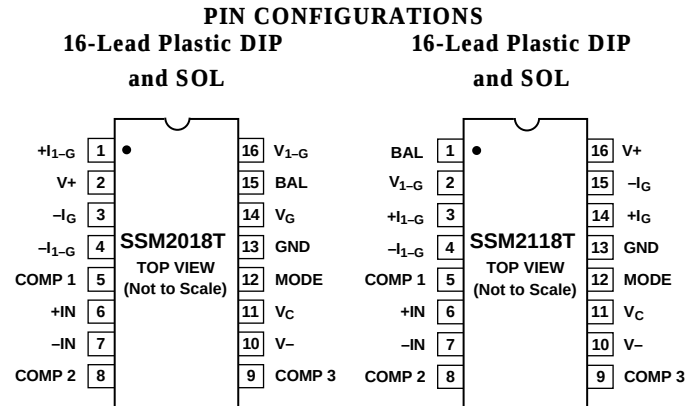
EIAJ Model 100 V

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

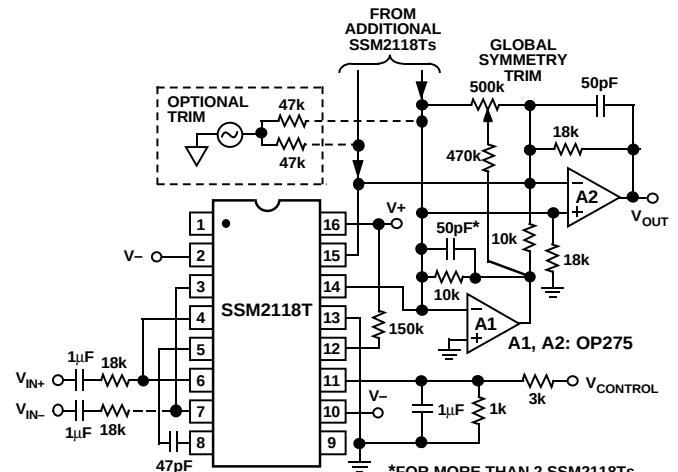


SSM2018T Typical Application Circuit

**ORDERING GUIDE**

Model	Temperature Range	Package Option*
SSM2018TP	-40°C to $+85^{\circ}\text{C}$	N-16
SSM2018TS	-40°C to $+85^{\circ}\text{C}$	R-16
SSM2118TP	-40°C to $+85^{\circ}\text{C}$	N-16
SSM2118TS	-40°C to $+85^{\circ}\text{C}$	R-16

*N = Plastic DIP; R = SOL.



SSM2118T Typical Application Circuit

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2018T/SSM2118T features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



SSM2018T/SSM2118T–Typical Characteristics

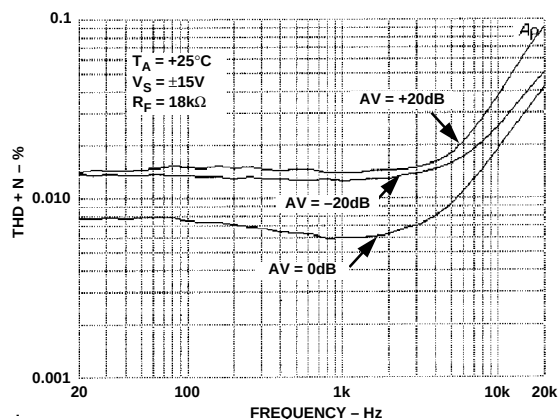


Figure 1. SSM2018T THD + N Frequency (80 kHz Low-Pass Filter, for $A_V = 0$ dB, $V_{IN} = 3$ V rms; for $A_V = +20$ dB, $V_{IN} = 0.3$ V rms; for $A_V = -20$ dB, $V_{IN} = 3$ V rms)

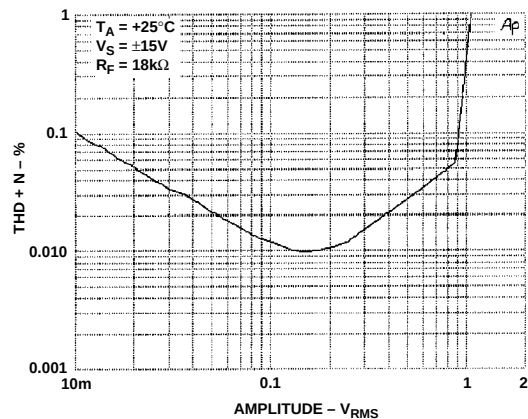


Figure 4. SSM2018T THD + N vs. Amplitude (Gain = +20 dB, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

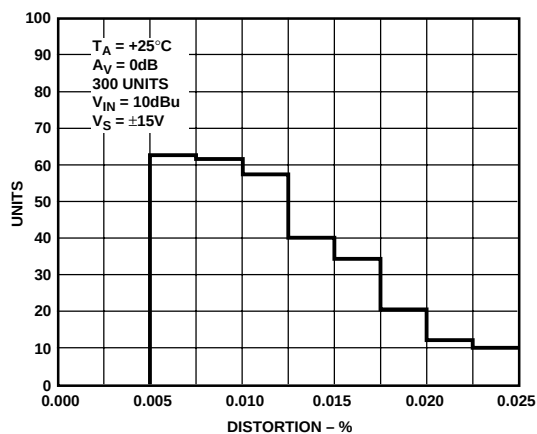


Figure 2. SSM2018T Distortion Distribution

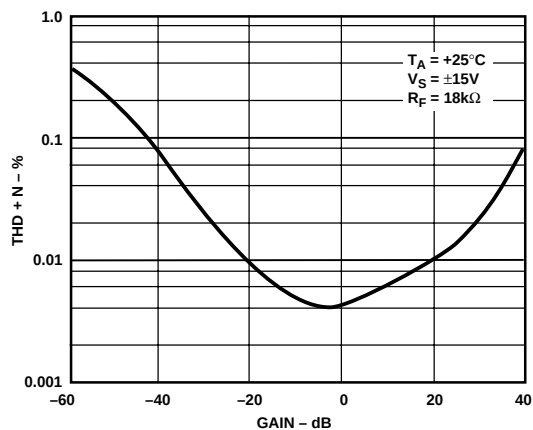


Figure 5. SSM2018T THD + N vs. Gain ($f_{IN} = 1$ kHz; for -60 dB $\leq A_V \leq -20$ dB, $V_{IN} = 10$ V rms; for 0 dB $\leq A_V \leq +20$ dB, $V_{IN} = 1$ V rms)

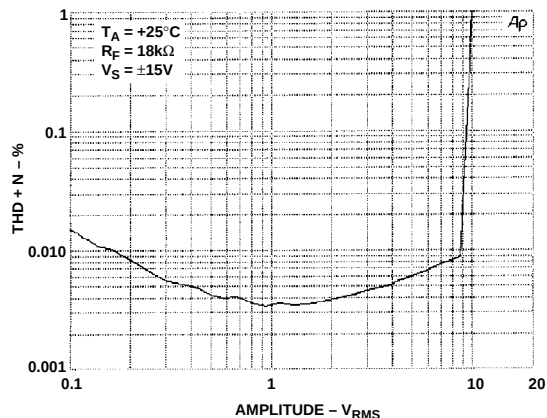


Figure 3. SSM2018T THD + N vs. Amplitude (Gain = 0 dB, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

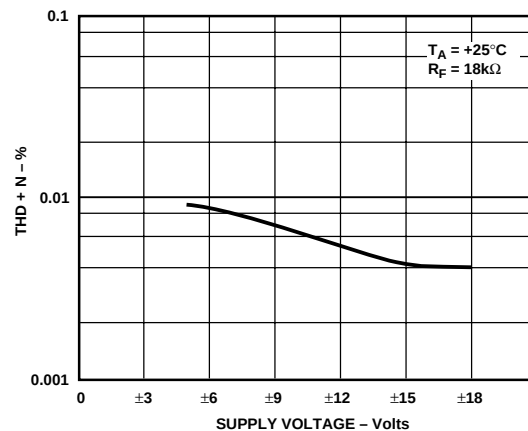


Figure 6. SSM2018T THD + N vs. Supply Voltage ($A_V = 0$ dB, $V_{IN} = 1$ V rms, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

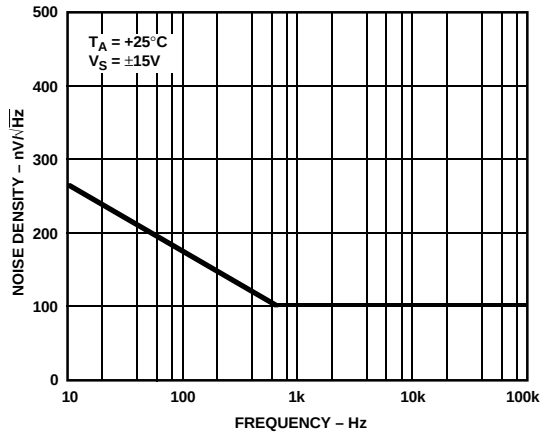


Figure 7. SSM2018T Noise Density vs. Frequency

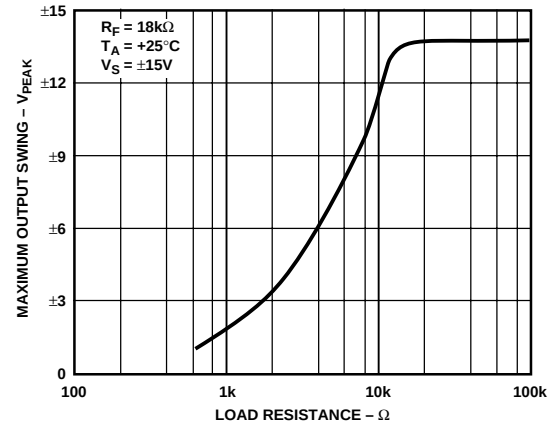


Figure 10. SSM2018T Maximum Output Swing vs. Load Resistance, (THD = 1 % max)

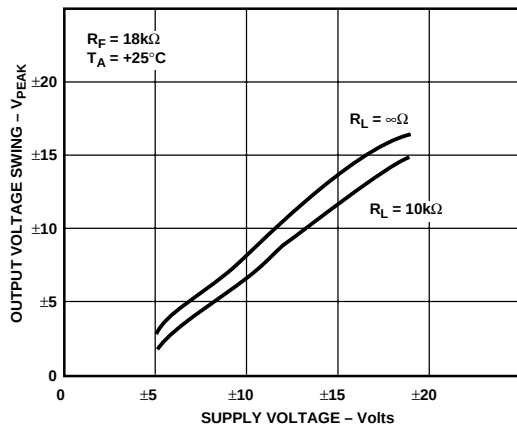


Figure 8. SSM2018T Maximum Output Swing vs. Supply Voltage (THD = 1% max)

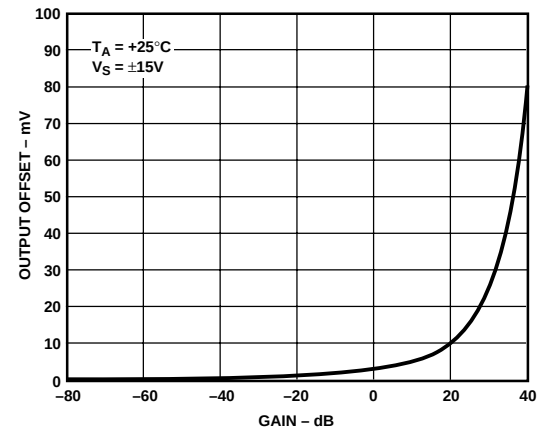


Figure 11. SSM2018T Output Offset vs. Gain

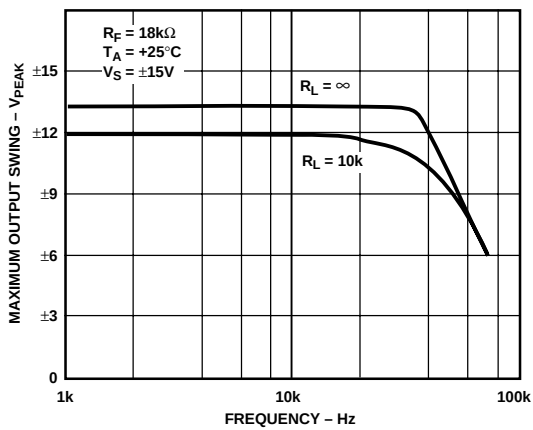


Figure 9. SSM2018T Maximum Output Swing vs. Frequency (THD = 1 % max)

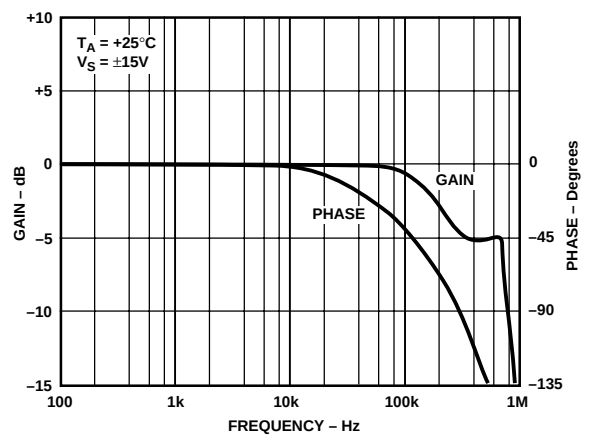


Figure 12. SSM2018T Gain/Phase vs. Frequency

SSM2018T/SSM2118T–Typical Characteristics

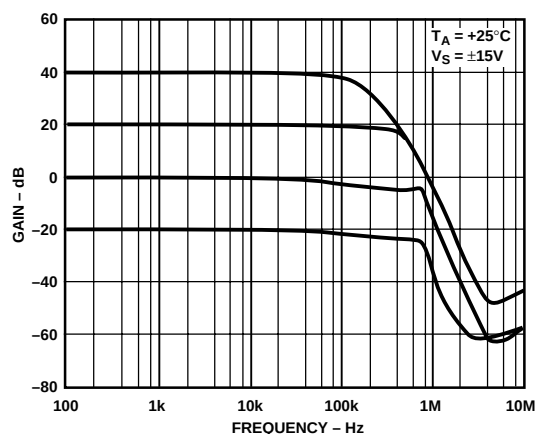


Figure 13. SSM2018T Gain vs. Frequency

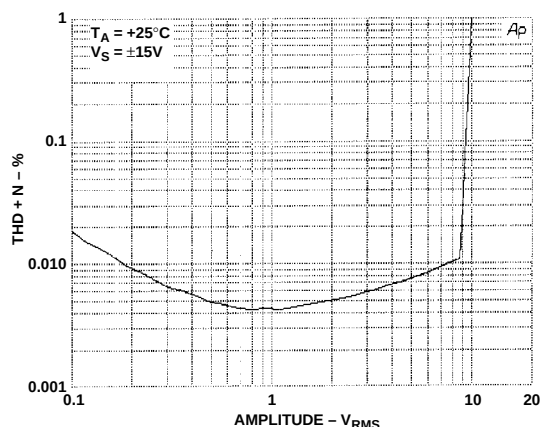


Figure 16. SSM2118T THD + N vs. Amplitude (Gain = 0 dB, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

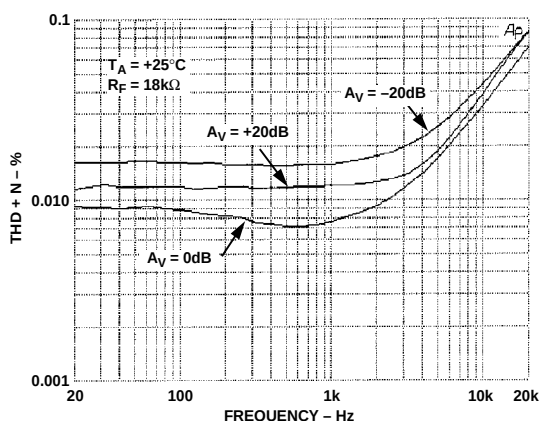


Figure 14. SSM2118T THD + N Frequency (80 kHz Low-Pass Filter, for $A_V = 0$ dB, $V_{IN} = 1$ V rms; for $A_V = +20$ dB, $V_{IN} = 0.1$ V rms; for $A_V = -20$ dB, $V_{IN} = 10$ V rms)

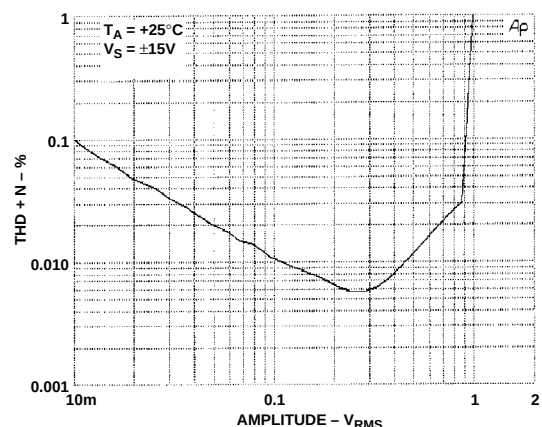


Figure 17. SSM2118T THD + N vs. Amplitude (Gain = +20 dB, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

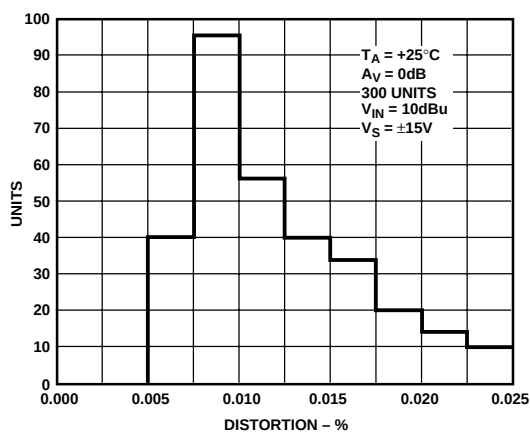


Figure 15. SSM2118T Distortion Distribution

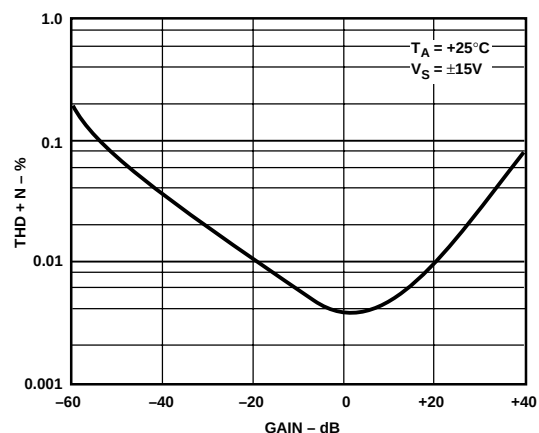


Figure 18. SSM2118T THD + N vs. Gain ($f_{IN} = 1$ kHz; for -60 dB $\leq A_V \leq -20$ dB, $V_{IN} = 10$ V rms; for 0 dB $\leq A_V \leq +20$ dB, $V_{IN} = 1$ V rms)

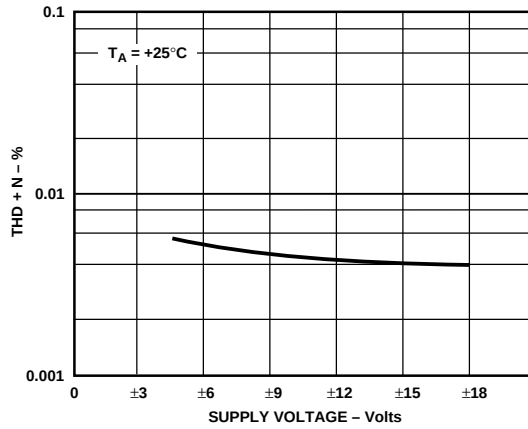


Figure 19. SSM2118T THD + N vs. Supply Voltage ($A_V = 0$ dB, $V_{IN} = 1$ V rms, $f_{IN} = 1$ kHz, 80 kHz Low-Pass Filter)

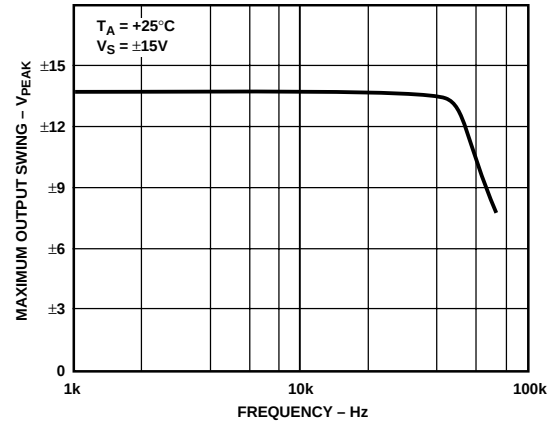


Figure 22. SSM2118T Maximum Output Swing vs. Frequency (THD = 1 % max)

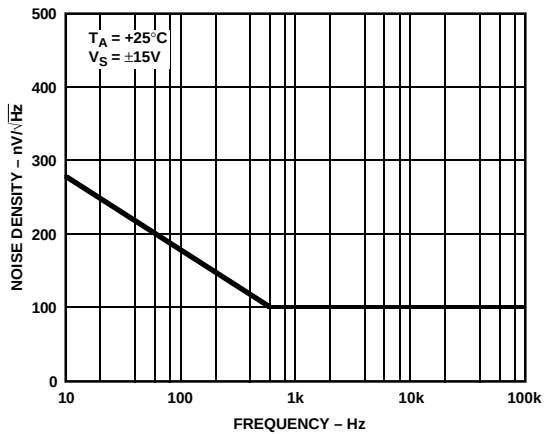


Figure 20. SSM2118T Noise Density vs. Frequency

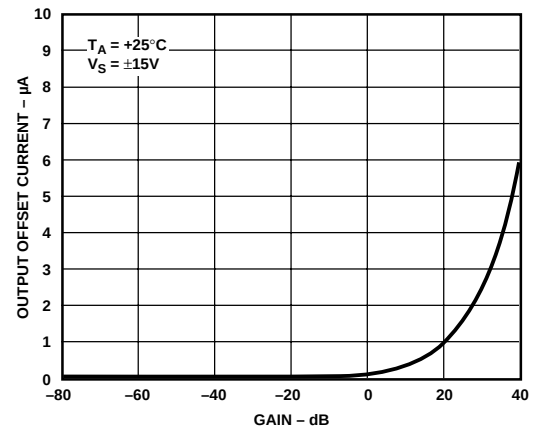


Figure 23. SSM2118T Output Offset Current vs. Gain

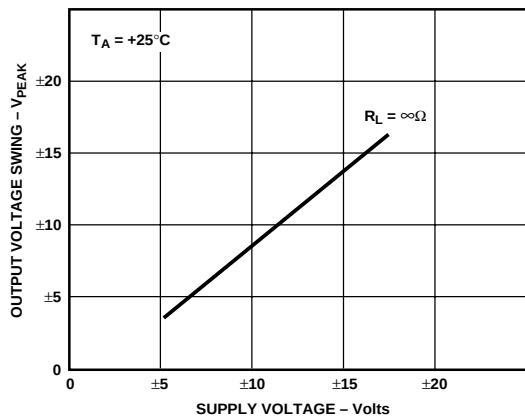


Figure 21. SSM2118T Maximum Output Swing vs. Supply Voltage (THD = 1% max)

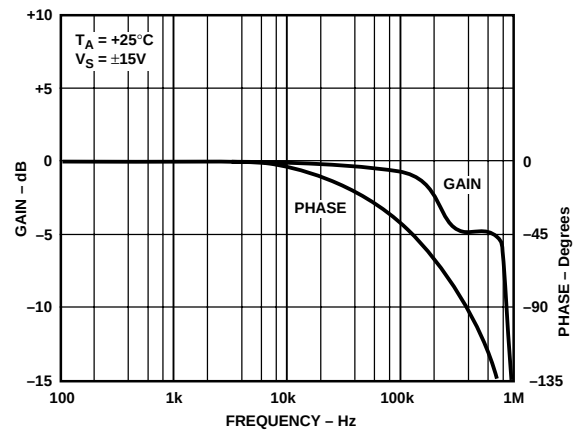


Figure 24. SSM2118T Gain/Phase vs. Frequency

SSM2018T/SSM2118T

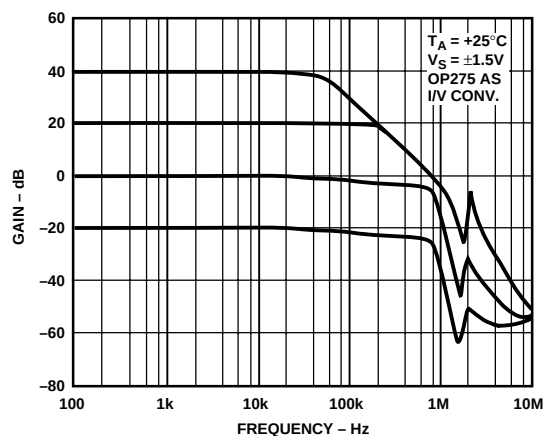


Figure 25. SSM2118T Gain vs. Frequency

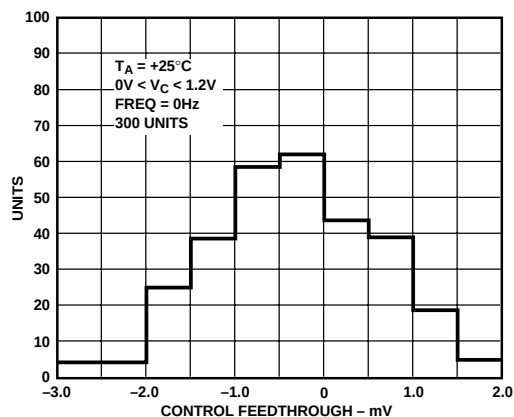


Figure 28. SSM2018T Control Feedthrough Distribution

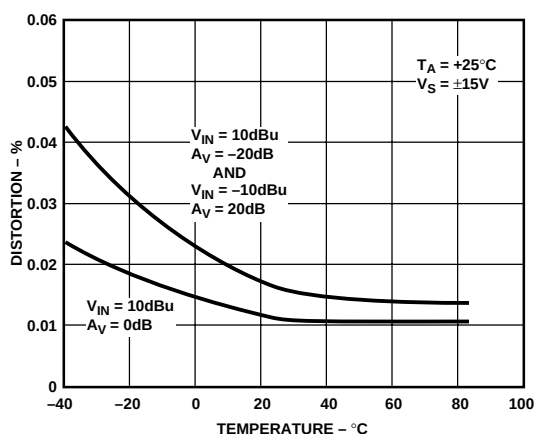


Figure 26. SSM2018T and SSM2118T Distortion vs. Temperature

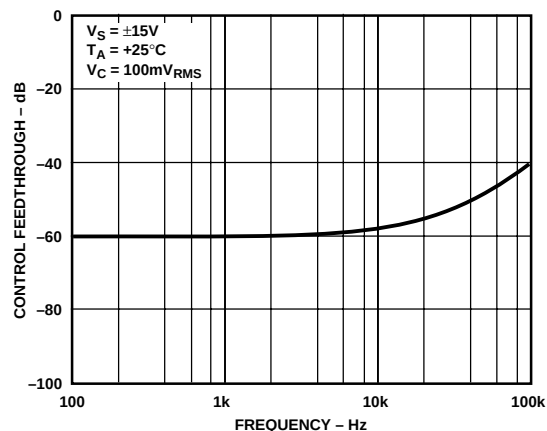


Figure 29. SSM2018T and SSM2118T Control Feedthrough vs. Frequency

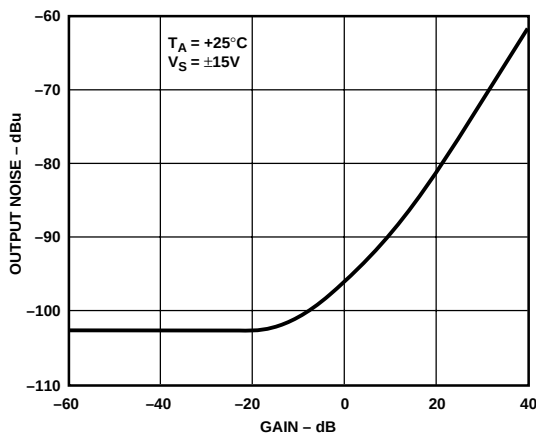


Figure 27. SSM2018T and SSM2118T Output Noise vs. Gain ($V_{IN} = GND$, 20 kHz Bandwidth)

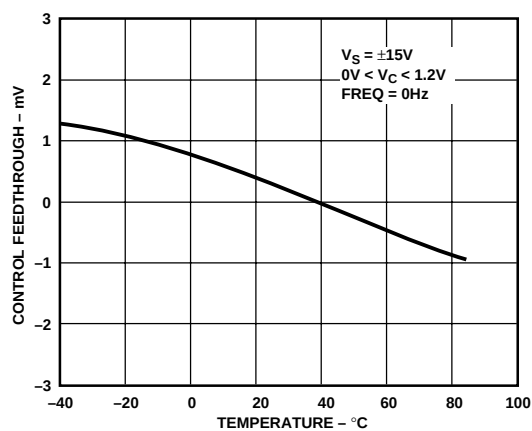


Figure 30. SSM2018T and SSM2118T Control Feedthrough vs. Temperature

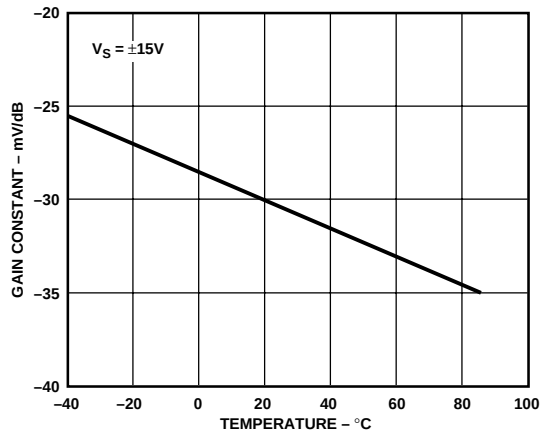


Figure 31. SSM2018T and SSM2118T Gain Constant vs. Temperature

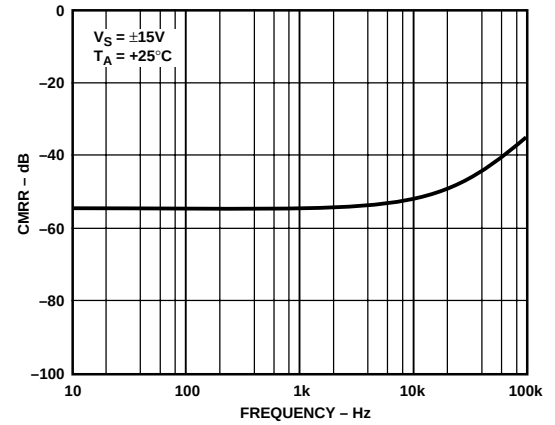


Figure 34. SSM2018T and SSM2118T CMRR vs. Frequency

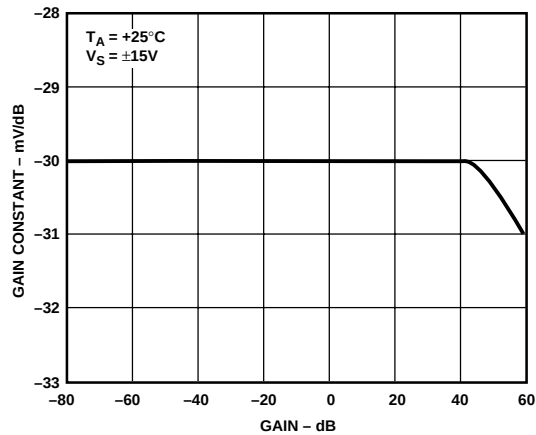


Figure 32. SSM2018T and SSM2118T Gain Constant Linearity vs. Gain

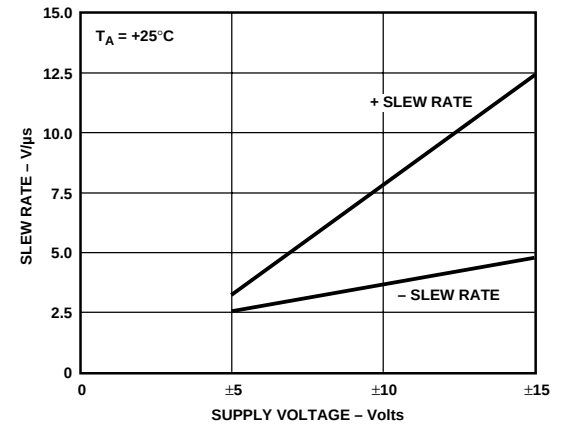


Figure 35. SSM2018T and SSM2118T Slew Rate vs. Supply Voltage

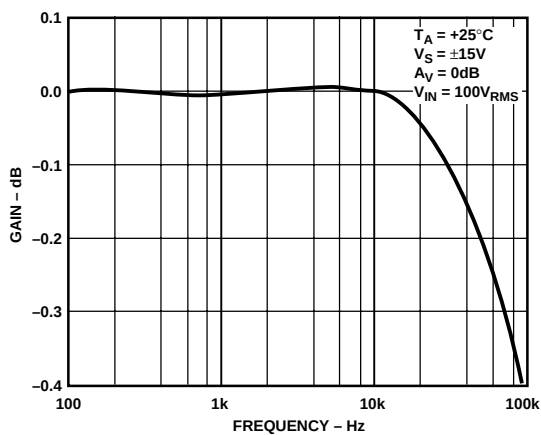


Figure 33. SSM2018T and SSM2118T Gain Flatness vs. Frequency

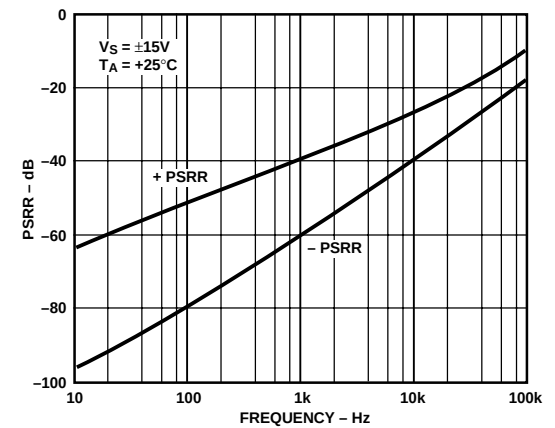


Figure 36. SSM2018T and SSM2118T PSRR vs. Frequency

SSM2018T/SSM2118T

APPLICATIONS

The SSM2018T is a *trimless* Voltage Controlled Amplifier (VCA) for volume control in audio systems. The SSM2018T is identical to the original SSM2018 in functionality and pinout; however, it is the first professional quality audio VCA in the marketplace that does not require an external trimming potentiometer to minimize distortion. Instead, the SSM2018T is laser trimmed before it is packaged to ensure the specified THD and control feedthrough performance. This has a significant savings in not only the cost of external trimming potentiometers, but also the manufacturing cost of performing the trimming during production.

The SSM2118T is identical to the SSM2018T except that differential current outputs are provided as opposed to a voltage output. This output configuration is ideal for bus summing applications where multiple audio signals are summed together. These signals often require long lead lengths or cable runs to reach the summing stage. Transmitting the signals in a differential current mode minimizes the chance for noise pickup and for line impedances to upset the balance of the system. The SSM2118T is also factory trimmed to minimize distortion and control feedthrough. Thus, no individual trim is required for each part. One global trim at the summing amplifier stage may be necessary to properly balance the resistors in this stage, as explained later.

Basic VCA Configuration

The primary application circuit for the SSM2018T is the basic VCA configuration, which is shown in Figure 37. This configuration uses differential current feedback to realize the VCA. A complete description of the internal circuitry of the VCA and this configuration is given in the Theory of Operation section below. *The SSM2018T and SSM2118T are trimmed at the factory for operation in the basic VCA configuration with class AB biasing.* Thus, for optimal distortion and control feedthrough performance, the same configuration and biasing should be used. All of the graphs for the SSM2018T in the data sheet have been measured using the circuit of Figure 37.

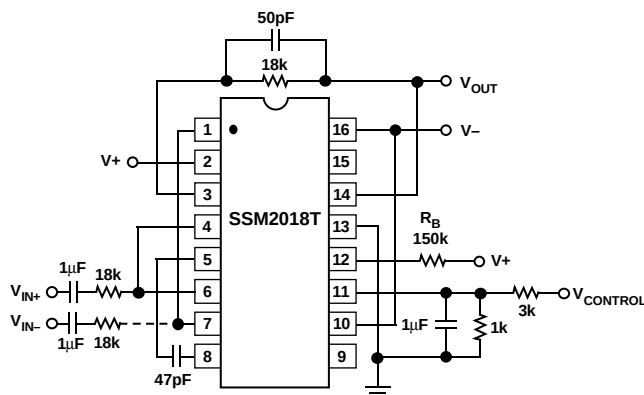


Figure 37. SSM2018T Basic VCA Application Circuit

In the simple VCA configuration, the SSM2018T inputs are at a virtual ground. Thus, 18 k Ω resistors are required to convert the input voltages to input currents. The schematic also shows ac coupling capacitors. These are inserted to minimize dc offsets generated by bias current through the resistors. Without the capacitors, the dc offset due to the input bias current is typically 5 mV. The input stage has the flexibility to run either inverting, noninverting, or balanced. The most common configuration is

to run it in the noninverting single-ended mode. If either input is unused, the associated 18 k Ω resistor and coupling capacitor should be removed to prevent any additional noise.

The common-mode rejection in balanced mode is typically 55 dB up to 1 kHz, decreasing at higher frequencies as shown in Figure 34. To ensure good CMRR in the balanced configuration, the input resistors must be balanced. For example, a 1% mismatch results in a CMRR of 40 dB. To achieve 55 dB, these resistors should have an absolute tolerance match of 0.1%.

The output of the basic VCA is taken from Pin 14, which is the output of an internal amplifier. Notice that the second voltage output (Pin 16) is connected to the negative supply. This is normal and actually disables that output amplifier ensuring that it will not oscillate and cause interference problems. Shorting the output to the negative supply does not cause the supply current to increase. This amplifier is only used in the “OVCE” application explained later.

The control port follows a 30 mV/dB control law. The application circuit shows a 3 k Ω and 1 k Ω resistor divider from a control voltage. The choice of these resistors is arbitrary and could be any values to properly scale the control voltage. In fact, these resistors could be omitted if the control voltage is already properly scaled. The 1 μ F capacitor is in place to provide some filtering of the control signal. Although the control feedthrough is trimmed at the factory, the feedthrough increases with frequency (Figure 29). Thus, high frequency noise can feedthrough and add to the noise of the VCA. Filtering the control signal helps minimize this source of noise.

Theory of Operation of the SSM2018T

The SSM2018T has the same internal circuitry as the original SSM2018. The detailed diagram in Figure 38 shows the main components of the VCA. The essence of the SSM2018T is the gain core, which is comprised of two differential pairs (Q1–Q4). When the control voltage, V_C , is adjusted, current through the gain core is steered to one side or the other of the two differential pairs. The tail current for these differential pairs is set by the mode bias of the VCA (Class A or AB), which is labeled as I_M in the diagram. I_M is then modulated by a current proportional to the input voltage, labeled I_S . For a positive input voltage, more current is steered (by the “Splitter”) to the left differential pair, and the opposite is true for a negative input.

To understand how the gain control works, a simple example is best. Take the case of a positive control voltage on Pin 11. Notice that the bases of Q2 and Q3 are connected to ground via a 200 Ω resistor. A positive control voltage produces a positive voltage on the bases of Q1 and Q4. Concentrating on the left most differential pair, this raises the base voltage of Q1 above that of Q2. Thus, more of the tail current is steered through Q1 than through Q2. The current from the collector of Q2 flows through the external 18 k Ω feedback resistor around amplifier A3. When this current is reduced, the output voltage is also reduced. Thus, a positive control voltage results in an attenuation of the input signal, which explains why the gain constant is negative.

The collector currents of Q2 and Q3 produce the output voltage. The output of Q3 is mirrored by amplifier A1 to add to the overall output voltage. On the other hand, the collector currents of Q1 and Q4 are used for feedback to the differential inputs. Because Pins 6 and 4 are shorted together, any input voltage produces an input current which flows into Pin 4. The

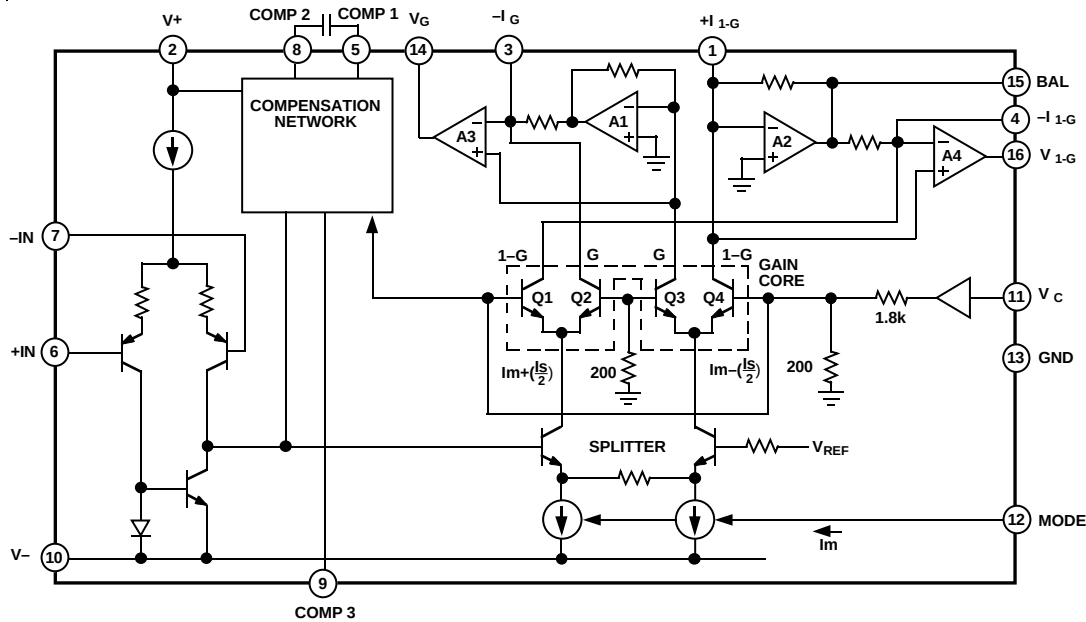


Figure 38. SSM2018T Detailed Functional Diagram

same is true for the inverting input, which is connected to Pin 1. The overall feedback ensures that the current flowing through the input resistors is balanced by the collector currents in Q1 and Q4.

Basic VCA Configuration for the SSM2118T

The SSM2118T behaves very much in the same way as the SSM2018T except that it has differential current outputs instead of a voltage output. The basic VCA configuration is shown in Figure 39. A dual output amplifier is needed to replace the internal amplifiers in the SSM2018T. However, multiple SSM2118Ts can share the output amplifiers. The op amps are configured so that the SSM2118T's output current is flowing into a virtual ground. This same virtual ground is presented to all the VCAs, allowing their currents to be summed without interaction.

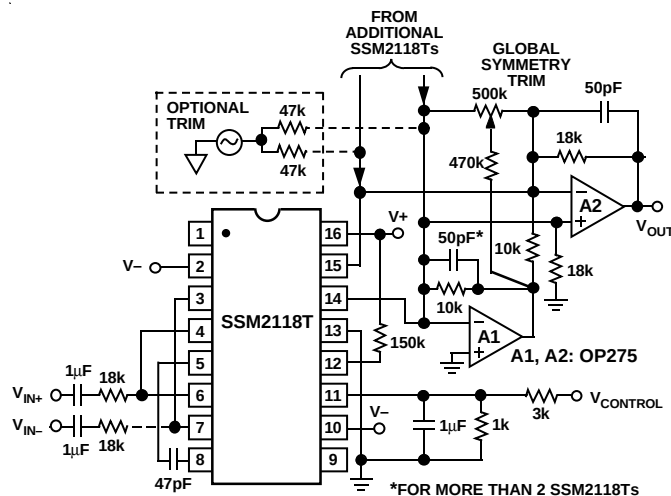


Figure 39. SSM2118T Typical Bus Summing Application

A global symmetry trim may be necessary, but since it is at the output amplifiers, only one trim is needed for any number of SSM2118Ts connected to the summing bus. This trim balances the resistors around the two amplifiers. If precision, matched resistors are used, the trim can be removed. However, to achieve 0.006% distortion, these resistors need to be matched to approximately 0.01%.

If the choice is made to perform the trim, then one of two methods may be used. The first method minimizes the distortion of an audio signal with the SSM2118T in the circuit. To perform the trim, a 0 dBu, 1 kHz sine wave is applied to one of the VCAs, and the output distortion is monitored. As the symmetry trim is adjusted, the output distortion will vary. The optimal adjustment produces the lowest distortion over the entire trim range. The second method is to insert a common mode signal by connecting two 47 kΩ resistors (matched to 0.01%) to the inverting inputs of each amplifier, as shown in the Figure 39. The signal is typically a 0 dBu, 1 kHz sine wave, although other signals can be used. The output is monitored with an oscilloscope, and the potentiometer is adjusted to achieve a minimum output signal.

The SSM2118T has the exact same input and gain core construction as the SSM2018T. Thus, any discussion of these portions of the SSM2018T apply equally to the SSM2118T. The main difference, which is apparent by comparing Figure 40 to Figure 38, is the removal of two output amplifiers, A1 and A3. Instead, the output currents come directly from the collectors of Q2 and Q3. Notice that the two external amplifiers in Figure 39 are configured the same as the internal amplifiers in the SSM2018T.

Two important characteristics of these current outputs must be considered: the output compliance and the effects of capacitive loading. Normally, the outputs are connected to a virtual ground node at the summing stage, which is biased at ground. This bias point can be altered somewhat. The part maintains good distortion performance for an output compliance from

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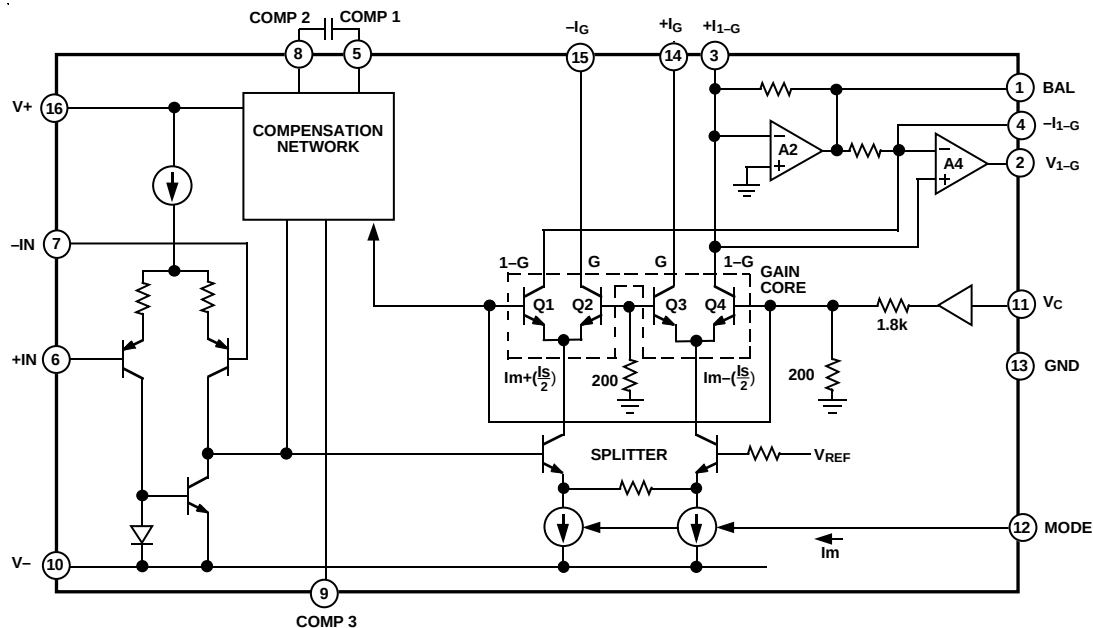


Figure 40. SSM2118T Detailed Functional Diagram

–0.1 V to +6.0 V. The negative compliance is much smaller because the gain core transistors (Q1 and Q3) begin to saturate when the collector potential is brought below their base potential. These outputs have high immunity to capacitive loads. In fact, the load on either or both outputs can be as large as 10 nF with no change in the distortion performance. For values above 10 nF, the distortion does start to increase. For example, a 100 nF load causes the distortion to increase from 0.006% to 0.02% at 1 kHz.

The noise performance of a single SSM2118T with an OP275 output amplifier is shown in Figure 20. When multiple SSM2118T parts are operated in parallel, the noise does increase by a factor equal to the square root of the number of parts paralleled. For example, if five parts are in parallel, the total output noise is $100 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{5} = 220 \text{ nV}/\sqrt{\text{Hz}}$.

Compensating the SSM2018T and SSM2118T

Both parts employ the same compensation network. This network uses an adaptive compensation scheme that adjusts the optimum compensation level for a given gain. The control voltage not only adjusts the gain core steering, it also adjusts the compensation. The SSM2018T and SSM2118T have three compensation pins: COMP1, COMP2, and COMP3. COMP3 is normally left open. Grounding this pin actually defeats the adaptive compensation circuitry, giving the VCA a fixed compensation point. The only time that this is desirable is when the VCA has fixed feedback, such as the Voltage Controlled Panner (VCP) circuit shown later in the data sheet. Thus, for the Basic VCA circuit or the OVCE circuit, COMP3 should be left open.

A compensation capacitor does need to be added between COMP1 and COMP2. Because the VCA operates over such a wide gain range, ideally the compensation should be optimized for each gain. When the VCA is in high attenuation, there is very little “loop gain,” and the part needs to have high compensation. On the other hand, at high gain, the same compensation capacitor would overcompensate the part and roll off the high frequency performance. Thus, the SSM2018T and SSM2118T

employ a patented adaptive compensation circuit. The compensation capacitor is “Miller” connected between the base and collector of an internal transistor. By changing the gain of this transistor via the control voltage, the compensation is changed.

Increasing the compensation capacitor causes the frequency response and slew rate to decrease, which will tend to cause high frequency distortion to increase. For the basic VCA circuit, 47 pF was chosen as the optimal value. The OVCE circuit described later uses a 220 pF capacitor. The reason for the increase is to compensate for the extra phase shift from the additional output amplifier used in the OVCE configuration. The compensation capacitor can be adjusted over a practical range from 47 pF to 220 pF, if desired. Below 47 pF, the parts may oscillate, and above 220 pF the frequency response is significantly degraded.

Control Section

As mentioned before, the control voltage on Pin 11 steers the current through the gain core transistors to set the gain. The output gain formula is as follows:

$$V_{OUT} = V_{IN} \times e^{(-aV_c)}$$

The exponential term arises from the standard Ebers-Moll equation describing the relationship of a transistor’s collector current as a function of the base-emitter voltage:

$$I_C = I_S \times e^{(V_{BE}/V_T)}$$

The factor “a” is a function of not only V_T but also the scaling due to the resistor divider of the 200 Ω and 1.8 k Ω resistors shown in Figures 38 and 40. The resulting expression for “a” is as follows: $a = 1/(10 \times V_T)$ which is approximately equal to four at room temperature. Substituting $a = 4$ in the above equation results in a –28.8 mV/dB control law at room temperature.

The –28.8 mV/dB number is slightly different from the data sheet specification of –30 mV/dB. The difference arises from the temperature dependency of the control law. The term V_T is known as the thermal voltage, and it has a direct dependency

on temperature: $V_T = kT/q$ (k = Boltzmann's constant = $1.38\text{E-}23$, q = electron charge = $1.6\text{E-}19$, and T = absolute temperature in Kelvin). This temperature dependency leads to the -3500 ppm/ $^{\circ}\text{C}$ drift of the control law. It also means that the control law changes as the part warms up. Thus, our specification for the control law states that the part has been powered up for 60 seconds.

When the part is initially turned on, the temperature of the die is still at the ambient temperature (25°C for example), but the power dissipation causes the die to warm up. With ± 15 V supplies and a supply current of 11 mA, 330 mW is dissipated. This number is multiplied by θ_{JA} to determine the rise in the die's temperature. In this case, the die increases from 25°C to approximately 50°C . A 25°C temperature change causes a 8.25% increase in the gain constant, resulting in a gain constant of 30 mV/dB. The graph in Figure 31 shows how the gain constant varies over the full temperature range.

Proper Operating Mode for the SSM2018T and SSM2118T

Both parts have the flexibility of operating in either Class A or Class AB. This is accomplished by adjusting the amount of current flowing in the gain core (I_M in Figure 38). The traditional trade-off between the two classes is that Class A tends to have lower THD but higher noise than Class AB. However, by utilizing well matched gain core transistors, distortion compensation circuitry, and laser trimming, the SSM2018T and SSM2118T have excellent THD performance in Class AB. Thus, the parts offer the best of both worlds in having the low noise of Class AB with low THD.

Because the parts operate optimally in Class AB, the distortion trim is performed for this class. To guarantee conformance to the data sheet THD specifications, both the SSM2018T and SSM2118T must be operated in Class AB. This does not mean that the parts cannot be operated in Class A, but the optimal THD trim point is different for the two classes. Using Class A operation results in a shift of THD performance from a typical value of 0.006% to 0.05% without trim. An external potentiometer could be added to change the trim back to its optimal point as shown in the OVCE application circuit, but this adds the expense and time in adjusting a potentiometer.

The class of operation is set by selecting the proper value for R_B shown in Figure 37. R_B determines the current flowing into the MODE input (Pin 12). For class AB operation with ± 15 V supplies, R_B should be 150 k Ω . This results in a current of 95 μA . For other supply voltages, adjust the value of R_B such that current remains at 95 μA . This current follows the formula:

$$I_{MODE} = \frac{(V_{CC} - 0.7\text{ V})}{R_B}$$

The factor of 0.7 V arises from the fact that the dc bias on Pin 12 is a diode drop above ground.

Output Drive

The SSM2018T is buffered by an internal op amp to provide a low impedance output. This output is capable of driving to within 1.2 V of either rail at 1% distortion for a 100 k Ω load. (Note: This 100 k Ω load is in parallel with the feedback resistor of 18 k Ω , so the effective load is 15.3 k Ω .) For better than 0.01% distortion, the output should remain about 3.5 V away from either rail as shown in Figure 3. As the graph of output

swing versus load resistance shows (Figure 10), to maintain less than 1% distortion, the output current should be limited to approximately ± 1.3 mA. If higher current drive is required, then the output should be buffered with a high quality op amp such as the OP176 or AD797.

The internal amplifiers are compensated for unity gain stability and are capable of driving a capacitive load up to 4700 pF. Larger capacitive loads should be isolated from the output of the SSM2018T by the use of a 50 Ω series resistor.

Upgrading SSM2018 Sockets

The SSM2018T easily replaces the SSM2018 in the basic VCA configuration. The parts are pin for pin compatible allowing direct replacement. At the same time, the trimming potentiometers for symmetry and offset should be removed, as shown in Figure 41. Upgrading to the SSM2018T immediately saves the expense of the potentiometers and the time in production of trimming for minimum distortion and control feedthrough.

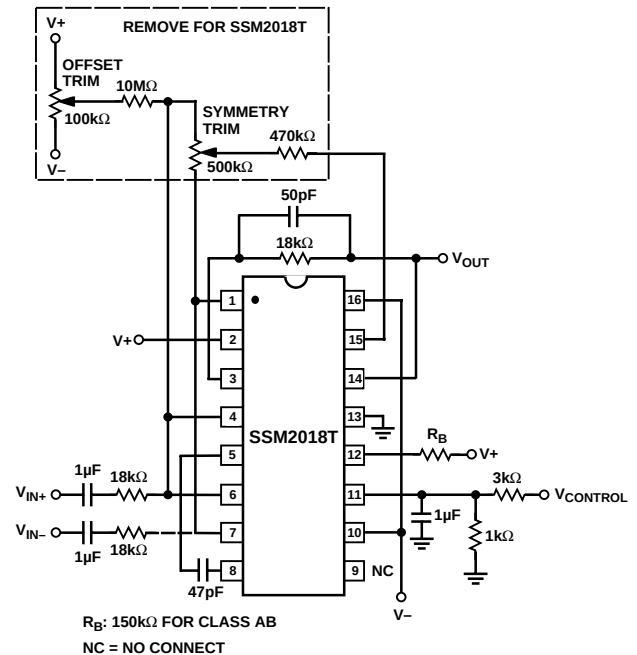


Figure 41. Upgrading SSM2018 Sockets

If the SSM2018 is used in the OVCE or VCP configuration, the SSM2018T can still directly replace it. However, the potentiometers cannot necessarily be removed, as explained in the OVCE and VCP sections.

Temperature Compensation of the Gain Constant

As explained above, the gain constant has a 3500 ppm/ $^{\circ}\text{C}$ temperature drift due to the inherent nature of the control port. Over the full temperature range of -40°C to $+85^{\circ}\text{C}$, the drift causes the gain to change by 7 dB if the part is in a gain of ± 20 dB. If the application requires that the gain constant be the same over a wide temperature range, then external temperature compensation should be employed. The simplest form of compensation is a temperature compensating resistor (TCR), such as the PT146 from Precision Resistor Co. These elements are different from a standard thermistor in that they are linear over temperature to better match the linear drift of the gain constant.

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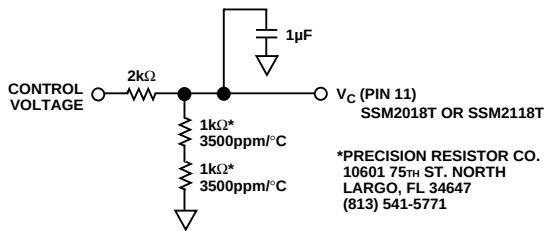


Figure 42. Two TCRs Compensate for Temperature Drift of Gain Constant

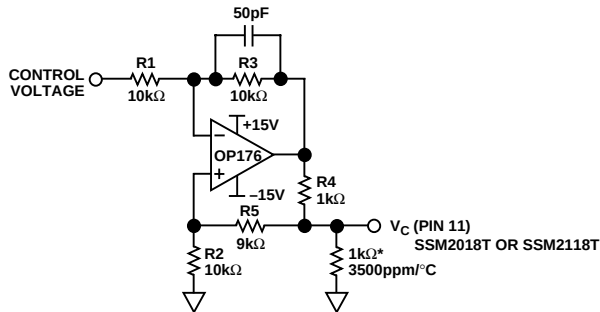


Figure 43. Current Source Allows Temperature Compensation with One TCR

One of the resistors in the divider to the control port can be substituted with an appropriately chosen TCR to compensate the SSM2018T or the SSM2118T as shown in Figure 42. Because the resistor divider effectively cuts the temperature coefficient in half, two TCRs must be used. The combined drift of the two is 7000 ppm/°C, given an effective drift for to the control voltage of -3500 ppm/°C. Of course, a single TCR with the appropriate coefficient can be used. The 3500 ppm parts were chosen because they are a standard item and do not need to be special ordered.

In many applications, an op amp is used to drive the control voltage. If this is the case, it may be more economical to use the op amp and a single TCR for temperature compensation. The op amp is configured as a Howland current source as shown in Figure 43. The current then flows through a single TCR to create the control voltage. Because the resistor divider is not present, the temp coefficient is equivalent to the TCR's coefficient. Using this technique, the drift was reduced from -3500 ppm/°C to -150 ppm/°C, which results in a total compensated gain shift of 0.4 dB over the full temperature range at a gain of ±20 dB.

Digital Control of the Gain

A common method of controlling the gain of a VCA is to use a digital-to-analog converter to set the control voltage. Figure 44 shows a 12-bit DAC, the DAC8512, controlling the SSM2018T (or SSM2118T). The DAC8512 is a complete 12-bit converter in an 8-pin package. It includes an on board reference and a output amplifier to produce an output voltage from 0 V to +4.095 V, which is 1 mV/bit. Since the voltage is always positive, this circuit only provides attenuation. The resistor divider on the output of the DAC8512 is set to scale the output voltage

such that full scale produces 80 dB of attenuation. The resistor divider can be adjusted to provide other attenuation ranges. If a parallel interface is needed, then the DAC8562 may be used, or for a dual DAC, the AD8582.

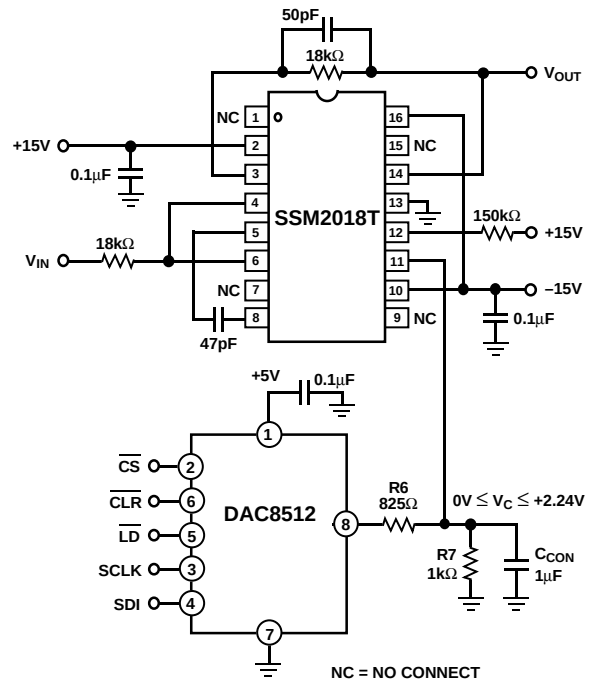


Figure 44. 12-Bit DAC Controls the VCA Gain

Supply Considerations and Single Supply Operation

The SSM2018T and SSM2118T have a wide operating supply range. Many of the graphs in this data sheet show the performance of the part from ±5 V to ±18 V. These graphs offer typical performance specifications and are a good indication of the parts capabilities. The minimum operating supply voltage is ±4.5 V. Below this voltage, the parts are inoperable. Thus, to account for supply variations, the recommended minimum supply is ±5 V.

The circuits in the data sheet do not show supply decoupling for simplicity; however, to ensure best performance, each supply pin should be decoupled with a 0.1 μF ceramic (or other low resistance and inductance type) capacitor as close to the package as possible. This minimizes the chance of supply noise feeding through the part and causing excessive noise in the audio frequency range.

The SSM2018T and SSM2118T can be operated in single supply mode as long as the circuit is properly biased. Figure 45 shows the proper configuration, which includes an amplifier to create a false ground node midway between the supplies. A high quality, wide bandwidth audio amplifier such as the OP176 or AD797 should be used to ensure a very low impedance ground over the full audio frequency range. The minimum operating supply for the SSM2018 is ±5 V, which gives a minimum single supply of +10 V and ground. The performance of the circuit with +10 V is identical to graphs that show operation of the SSM2018T with ±5 V supplies.

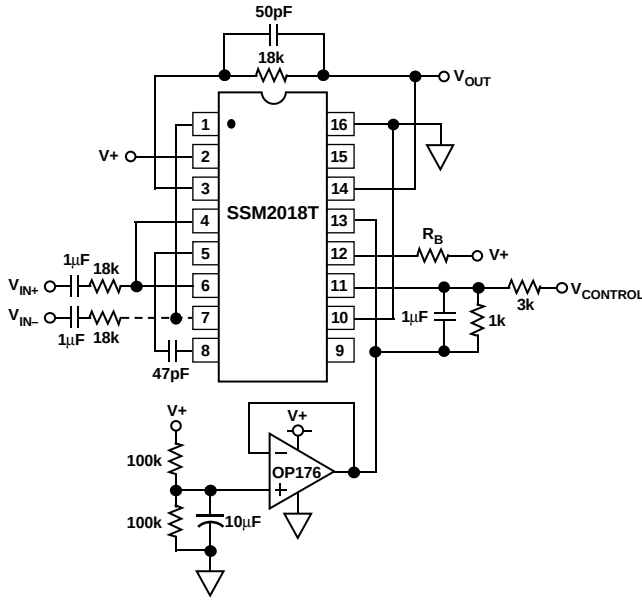


Figure 45. Single Supply Operation of SSM2018T

Operational Voltage Controlled Element

The SSM2018T has considerable flexibility beyond the basic VCA circuit utilized throughout this data sheet. The name “Operational Voltage Controlled Element” comes from the fact that the part behaves much like an operational amplifier with a second voltage controlled output. The symbol for the OVCE connected as a unity gain follower/VCA is shown in Figure 46. The voltage output labeled V_{1-G} is fed back to the inverting input just as for an op amp’s feedback. The V_G output is amplified or attenuated depending upon the control voltage. Because the OVCE works just like an op amp, the feedback could just as easily have included resistors to add gain, or a filter network to add frequency shaping. The full circuit for the OVCE is shown in Figure 47. Notice that the amplifier whose output (Pin 16) was originally connected to V_{MINUS} is now the output for feedback. As mentioned before, because the SSM2018T is trimmed for the basic VCA configuration, potentiometers are needed for the OVCE configuration to ensure the best THD and control feedthrough performance.

If a symmetry trim is to be performed, it should precede the control feedthrough trim and be done as follows:

1. Apply a 1 kHz sine wave of +10 dBu to the input, with the control voltage set for unity gain.
2. Adjust the symmetry trim potentiometer to minimize distortion of the output signal.

Next the control feedthrough trim is done as follows:

1. Ground the input signal port and apply a 60 Hz sine wave to the control port. The sine wave should have its high and low peaks correspond to the highest gain to be used in the application and 30 dB of attenuation, respectively. For example, a range of +20 dB gain to 30 dB attenuation requires that the sine wave amplitude ranges between -560 mV and +840 mV on Pin 11.
2. Adjust the control feedthrough potentiometer to null the signal seen at the output.

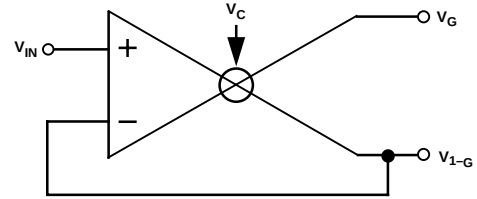


Figure 46. OVCE Follower/VCA Connection

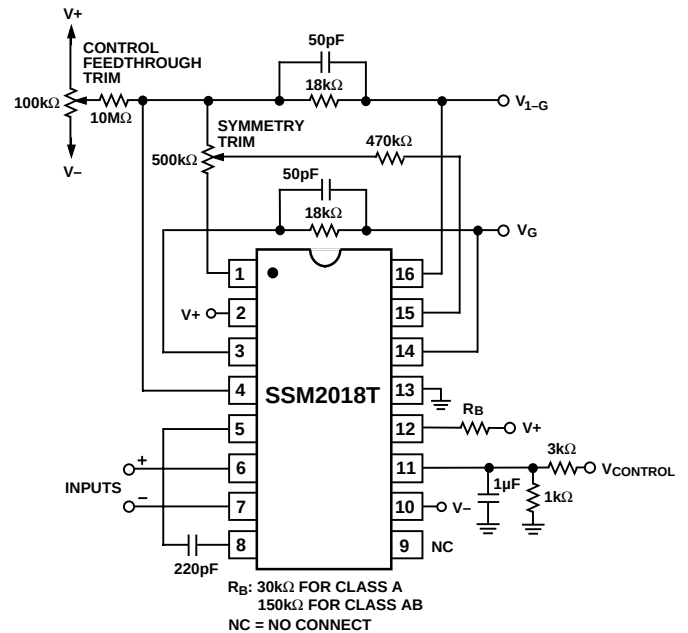


Figure 47. OVCE Application Circuit

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Voltage Controlled Panner

An interesting circuit that is built with the OVCE building block is a voltage controlled panner. Figure 48 shows the feedback connection for the circuit. Notice that the average of both outputs is fed back to the input. Thus, the average must be equal to the input voltage. When the control voltage is set for gain at V_G , this causes V_{1-G} to attenuate (to keep the average the same). On the other hand, when V_G is attenuated, V_{1-G} is amplified. The result is that the control voltage causes the input to “pan” from one output to the other. The following expressions show how this circuit works mathematically:

$$V_G = 2 K \times V_{IN} \text{ and } V_{1-G} = 2 (1 - K) \times V_{IN}$$

where K varies between 0 and 1 as the control voltage is changed from full attenuation to full gain respectively. When $V_C = 0$, then $K = 0.5$ and $V_G = V_{1-G} = V_{IN}$. Again, trimming is required for best performance. Pin 9 should be grounded. This is possible because the feedback is constant and the adaptive network is not needed. The VCP is the only application shown in this data sheet where Pin 9 is grounded.

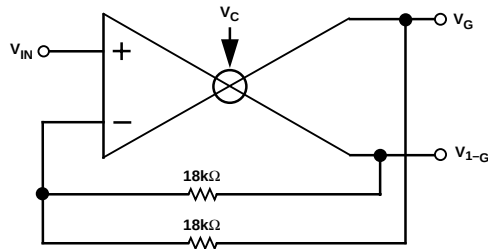
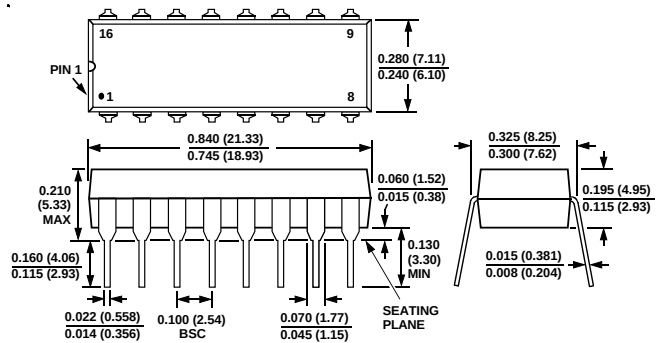


Figure 48. Basic VCP Connection

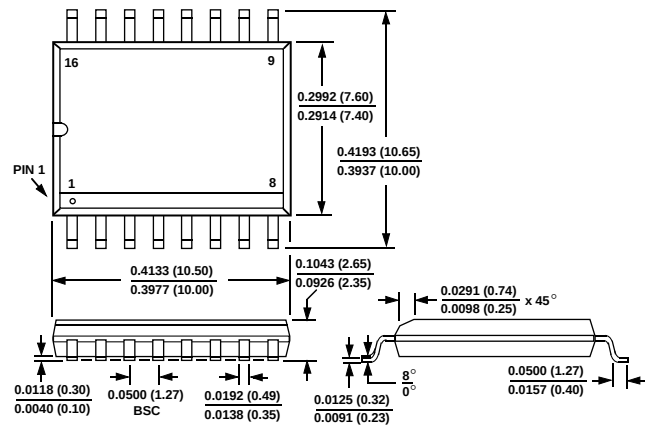
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic DIP (N-16) Package



16-Pin SOIC (R-16) Package



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