

SSP4N60B/SSS4N60B

600V N-Channel MOSFET

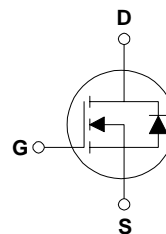
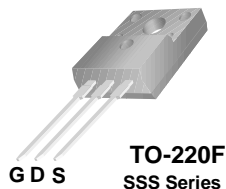
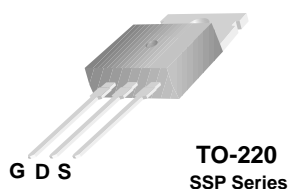
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 4.0A, 600V, $R_{DS(on)} = 2.5\Omega @ V_{GS} = 10V$
- Low gate charge (typical 22 nC)
- Low Crss (typical 14 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	SSP4N60B	SSS4N60B	Units
V _{DSS}	Drain-Source Voltage	600		V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	4.0	4.0 *	A
		2.5	2.5 *	A
I _{DM}	Drain Current - Pulsed (Note 1)	16	16 *	A
V _{GSS}	Gate-Source Voltage	± 30		V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	240		mJ
I _{AR}	Avalanche Current (Note 1)	4.0		A
E _{AR}	Repetitive Avalanche Energy (Note 1)	10		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P _D	Power Dissipation (T _C = 25°C) - Derate above 25°C	100	33	W
		0.8	0.26	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150		°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	SSP4N60B	SSS4N60B	Units
R _{θJC}	Thermal Resistance, Junction-to-Case Max.	1.25	3.79	°C/W
R _{θCS}	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	°C/W

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.65	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	--	2.0	2.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.0\text{ A}$ (Note 4)	--	4.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	710	920	pF
C_{oss}	Output Capacitance		--	65	85	pF
C_{riss}	Reverse Transfer Capacitance		--	14	19	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 4.0\text{ A},$ $R_G = 25\ \Omega$	--	20	50	ns
t_r	Turn-On Rise Time		--	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	150	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	55	120
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 4.0\text{ A},$ $V_{GS} = 10\text{ V}$	--	22	29	nC
Q_{gs}	Gate-Source Charge		--	4.8	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	8.5	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.0	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A},$	--	330	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	2.67	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 27.5\text{mH}, I_{AS} = 4.0\text{A}, V_{DD} = 50\text{V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.0\text{A}, di/dt \leq 300\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

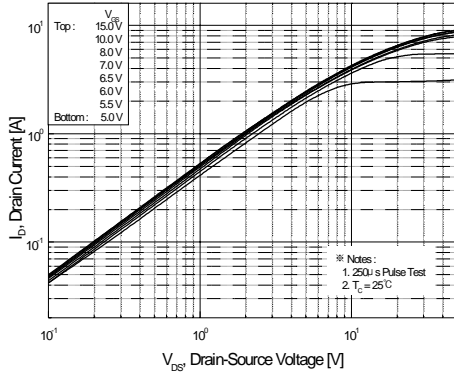


Figure 1. On-Region Characteristics

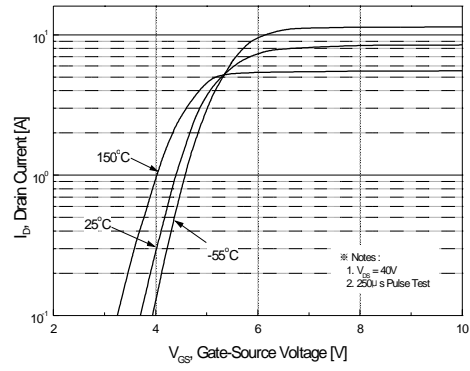


Figure 2. Transfer Characteristics

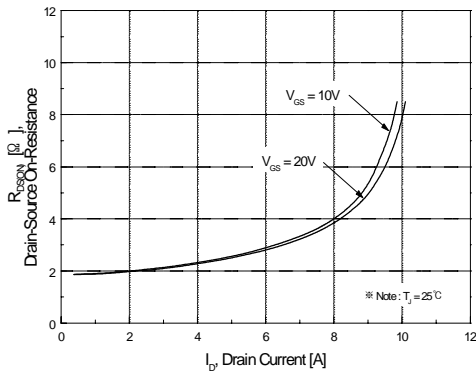


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

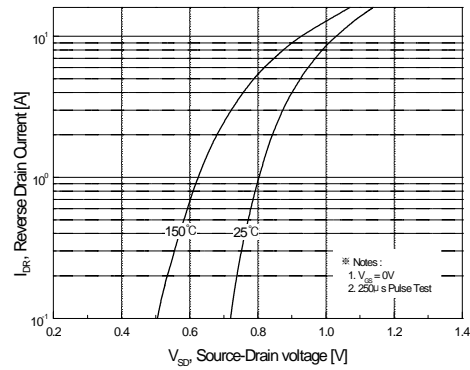


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

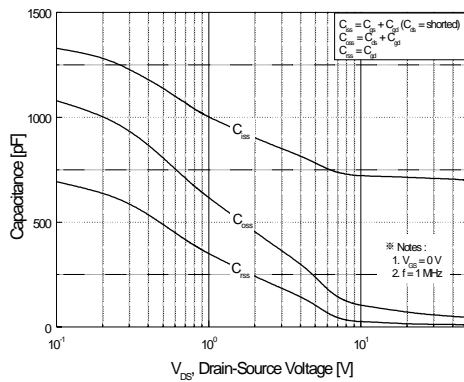


Figure 5. Capacitance Characteristics

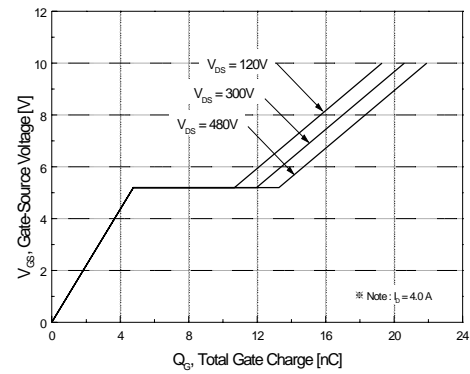


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

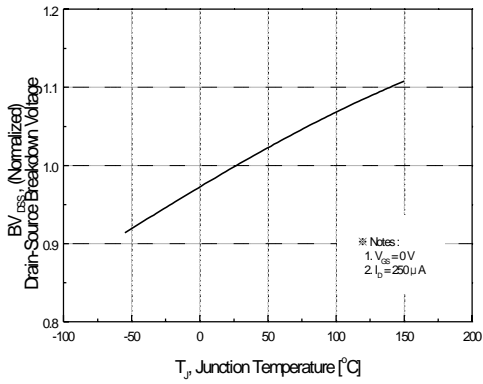


Figure 7. Breakdown Voltage Variation vs Temperature

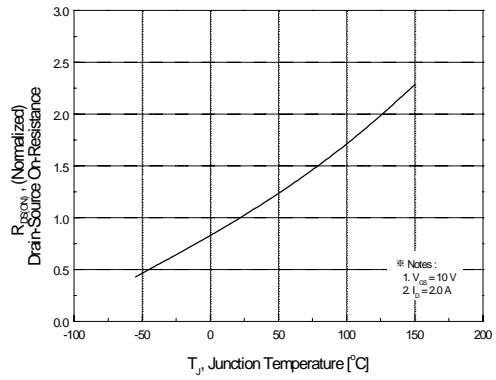


Figure 8. On-Resistance Variation

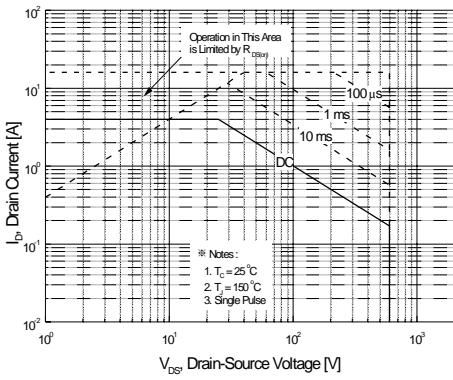


Figure 9-1. Maximum Safe Operating Area for SSP4N60B

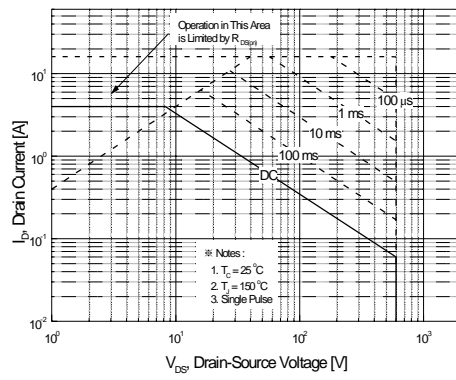


Figure 9-2. Maximum Safe Operating Area for SSS4N60B

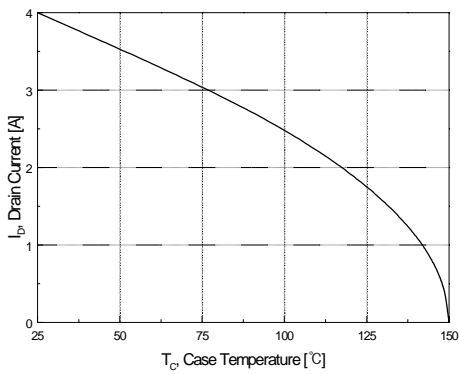


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

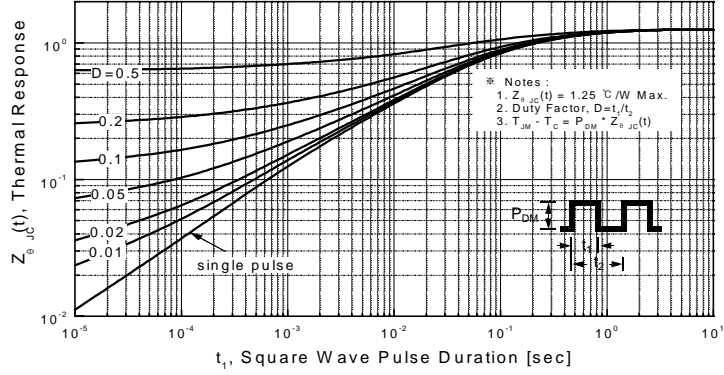


Figure 11-1. Transient Thermal Response Curve for SSP4N60B

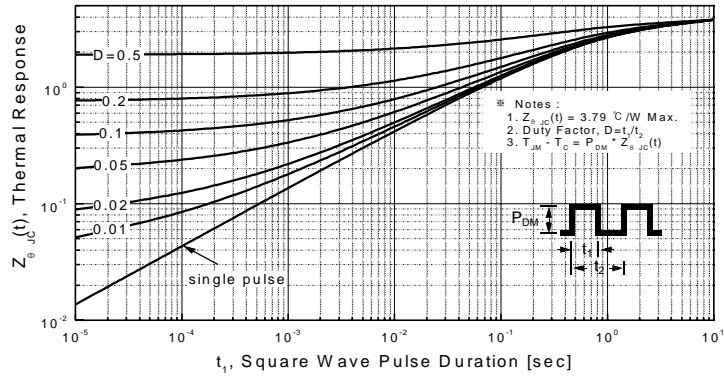
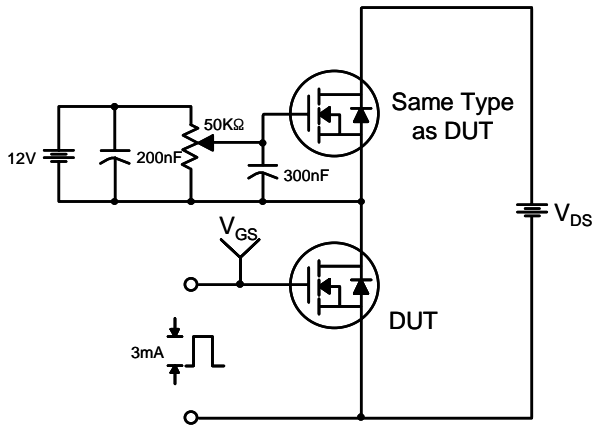


Figure 11-2. Transient Thermal Response Curve for SSS4N60B

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



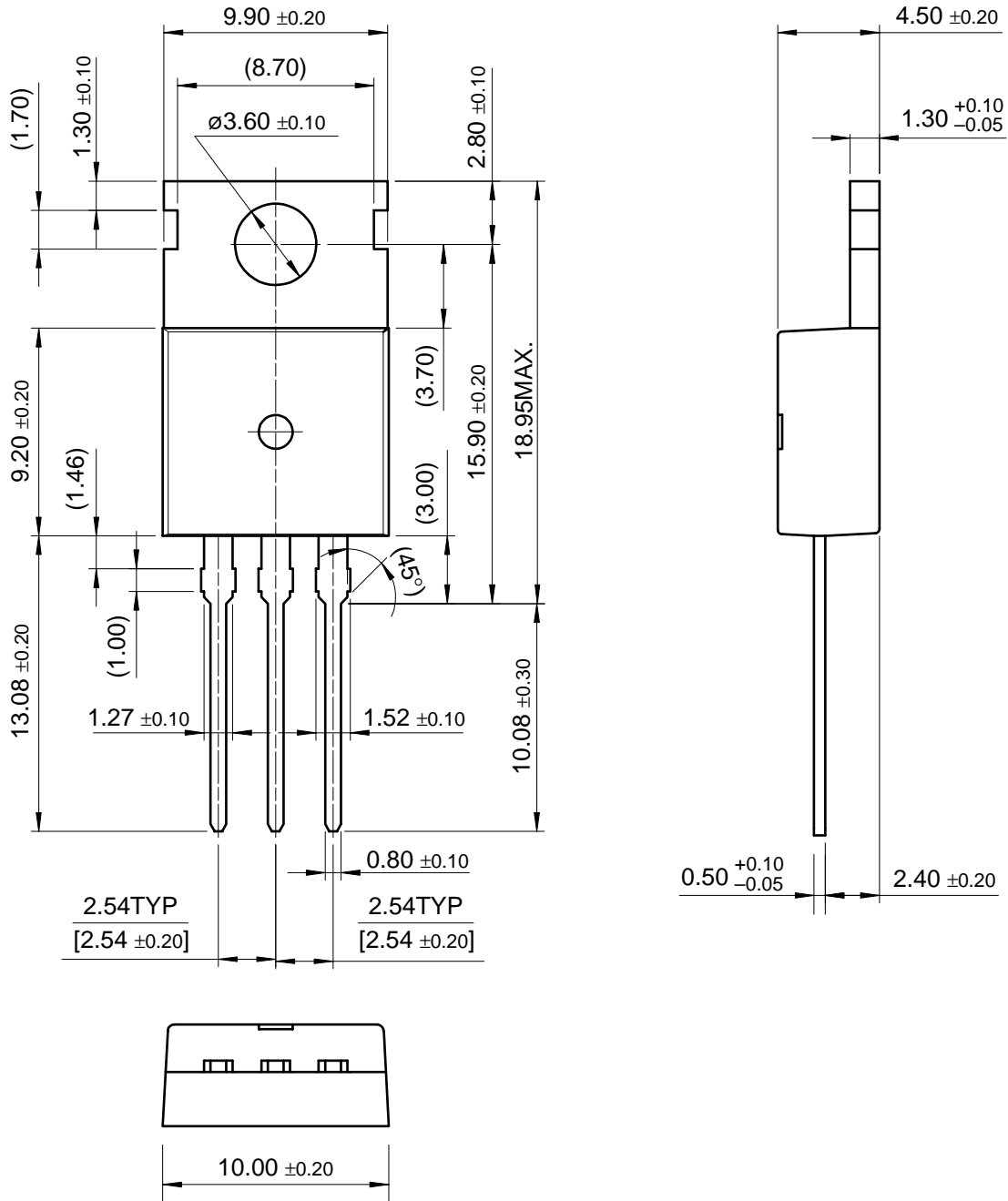
Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimensions

TO-220

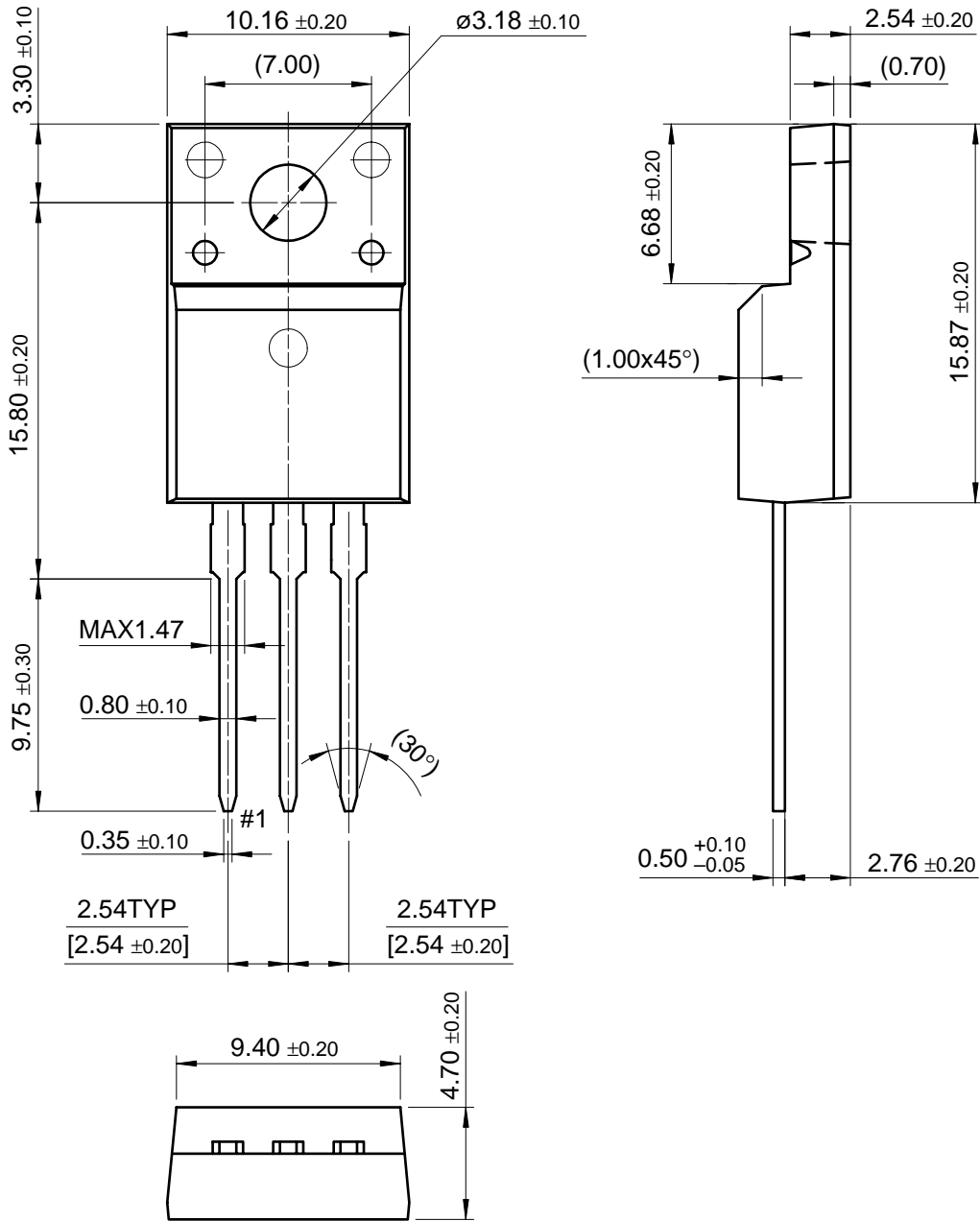
SSP4N60B/SSS4N60B



Dimensions in Millimeters

Package Dimensions (Continued)

TO-220F



SSP4N60B/SSS4N60B

Dimensions in Millimeters

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