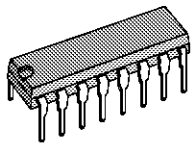
SGS-THOMSON MICROELECTRONICS

ST7162

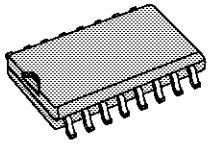
UNIVERSAL PROGRAMMABLE DUAL PLL

PRODUCT PREVIEW

- TWO INDEPENDENT PLL WITH 16 BITS PROGRAMMABLE DIVIDERS FROM 13 TO 65535 FOR TRANSMIT AND RECEIVE LOOPS
- ON CHIP REFERENCE OSCILLATOR COMMON FOR THE TWO LOOPS UP TO 16MHz WITH EXTERNAL CRYSTAL
- TWO INDEPENDENT PROGRAMMABLE REFERENCE COUNTERS:
  - 12 bits programmable counter from 13 to 4095 followed by selectable dividers by 1, 4 and 25
  - 14 bits auxiliary programmable counter from 13 to 16383
- A MCU CLOCK DERIVED FROM REFERENCE OSCILLATOR WITH A SELECTABLE DIVISION FACTOR OF 3 OR 4
- TWO INDEPENDENT PFD (PHASE FREQUENCY DISCRIMINATOR) WITH 3 STATE OUTPUTS
- LOCK DETECT SIGNAL OUTPUT FOR THE TRANSMIT LOOP
- 3 & 4 WIRES SELECTABLE MCU SERIAL INTERFACE, FOR SIMULTANEOUS PROGRAMMING OF 2 COUNTERS
- STAND-BY MODE



DIP16
ORDERING NUMBER: ST7162N



SO16
ORDERING NUMBER: ST7162D

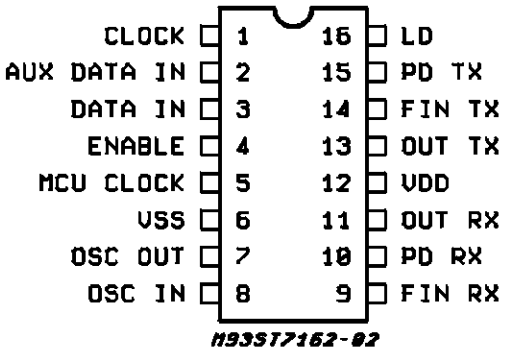
MAIN CHARACTERISTICS

- High input sensitivity:
  200mVpkpk @ 60MHz
- Low consumption:
  3.5mA @ 3V for the two loops
- Power supply voltage:
  3V to 5V
- Operating temperature range:
  –25°C to +70°C

DESCRIPTION

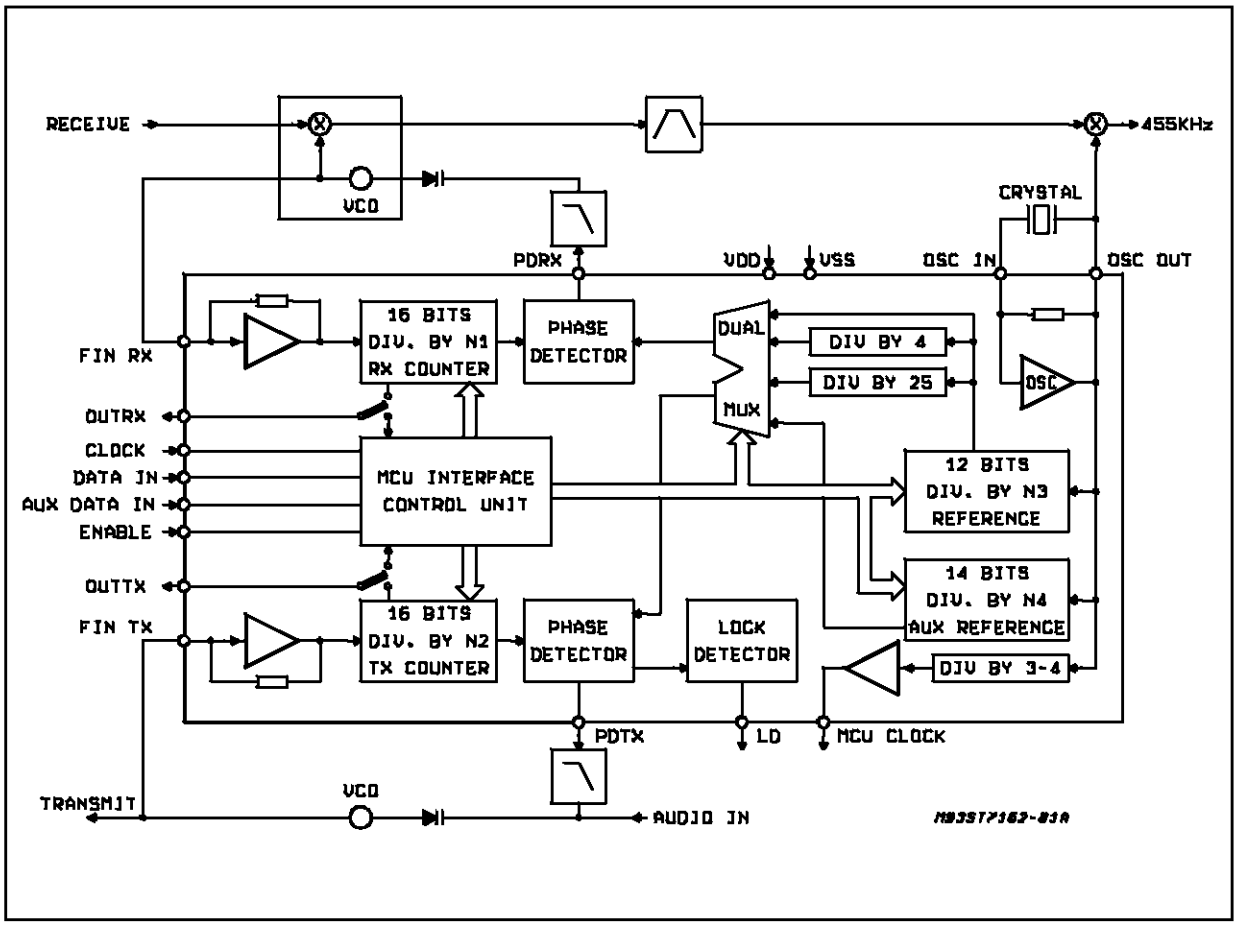
The ST7162 is a dual frequency synthesizer in High Speed CMOS technology for radio applications with a frequency up to 60MHz. The low power consumption and high flexibility make it well suitable for cordless CT0 applications in various countries.

PIN CONNECTION (Top view)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD} - V_{SS}	Supply Voltage	– 0.5 to +6	V
V_{IN}	Input Voltage	V_{SS} –0.5 to V_{DD} +0.5	V
V_{OUT}	Output Voltage	V_{SS} –0.5 to V_{DD} +0.5	V
I_{IN}, I_{OUT}	DC Current per pin	– 10 to 10	mA
I_{DD}, I_{SS}	DC Current for pin V_{DD} or V_{SS}	– 30 to 30	mA
T_{stg}	Storage Temperature	– 55 to +125	°C

PIN FUNCTIONS

N.	Name	Function
1	CLOCK	MCU Interface
2	AUX DATA IN	MCU Interface
3	DATA IN	MCU Interface
4	ENABLE	MCU Interface
5	MCU CLOCK	Scaled down reference frequency for clocking the MCU
6	V_{SS}	Negative Power Supply
7	OSC OUT	Oscillator Output
8	OSC IN	Oscillator Input
9	FIN R_X	Input to the 16 bits Receive Counter
10	PD R_X	Phase detector output of the Receive loop
11	Out R_X	Power saving output bit for the RX loop and FIN R_X divided by N1 for testing the R_X input sensitivity.
12	V_{DD}	Positive power supply
13	OUT T_X	Power saving output bit for the T_X loop and FIN T_X divided by N2 for testing the T_X input sensitivity.
14	FIN T_X	Input to the 16 bits Transmit counter.
15	PD T_X	Phase detector output of the transmit loop
16	LD	Lock detect output of the transmit loop.

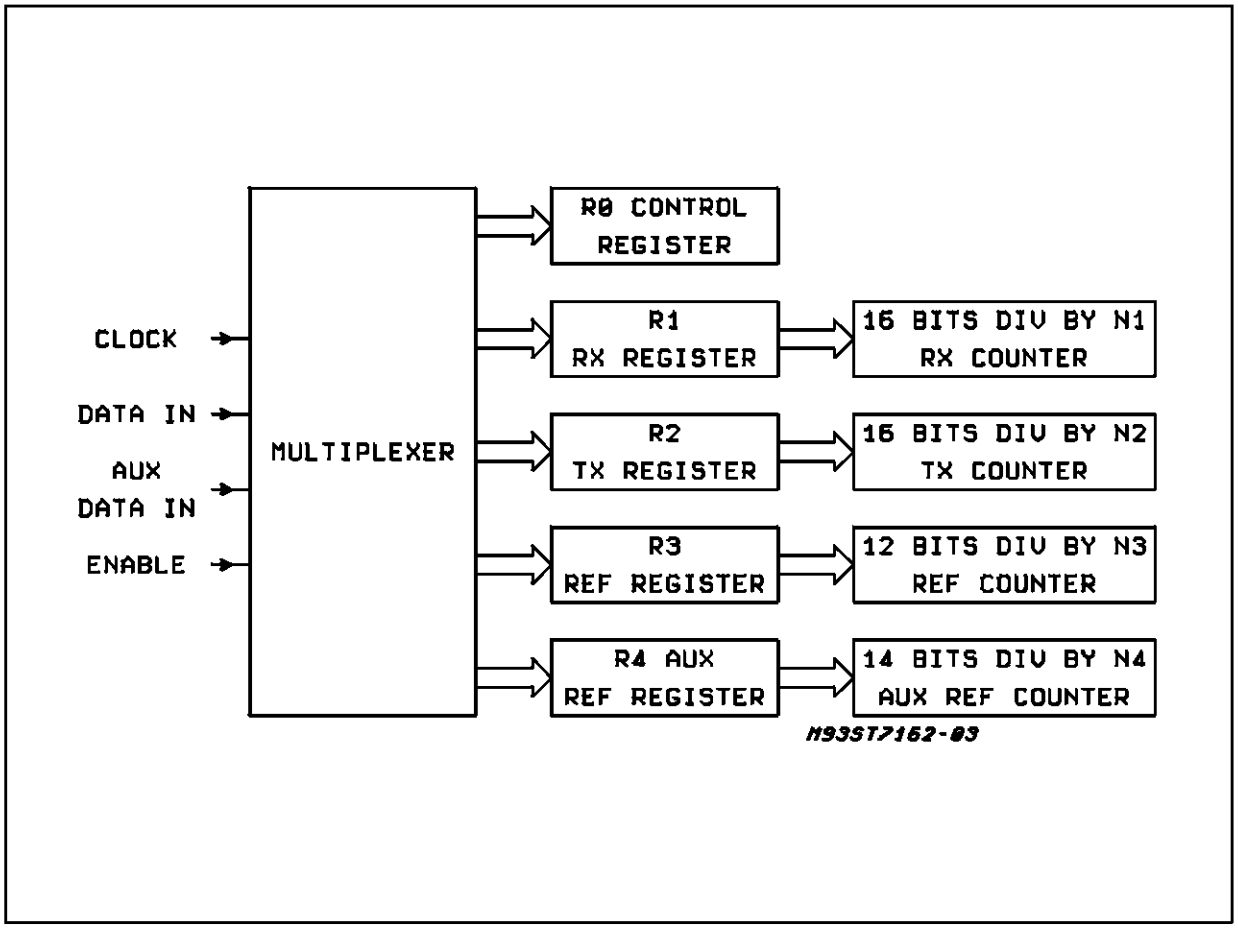
ELECTRICAL CHARACTERISTICS (Tamb = 25°C, voltage reference = V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	Min.	Typ.	Max.	Unit
SUPPLY							
V_{DD}	Supply Voltage			3		5.5	V
I_{DD} up	Supply Current	200mVpkpk sinus at input; FIN RX = 36MHz, FIN TX =49MHz; loop in lock condition; f_{osc} = 10.24MHz; no output load	3V 5V			3.7 7.7	mA mA
I_{DDRX}	Supply Current	200mVpkpk sinus at input; FIN RX = 36MHz; TX Loop in Power down; f_{osc} = 10.24MHz; no output load	3V 5V			2.5 5.3	mA mA
I_{DD} down	Supply Current	Stand-by mode for all counters; OSCIN pin Grounded; MCU interface disabled	3V 5V			150 300	µA µA
T_X and R_X INPUTS							
C_{IN}	Input Capacitance					8	pF
I_{IN} up	Input Current	$0 < V_{IN} < V_{DD}$	3V 5V	– 60 – 100		60 100	µA µA
Fmax	Input Frequency	Input = sinus 200mVpkpk AC coupled	3-5V			60	MHz
OSCILLATOR							
C_{IN}	Input Capacitance					8	pF
C_{OUT}	Output Capacitance					8	pF
I_{IN} up	Input Current	$0 < V_{IN} < V_{DD}$ DC measured	3V 5V	– 60 – 100		60 100	µA µA
Fmax	Input Frequency		3-5V			16	MHz

ELECTRICAL CHARACTERISTICS (Tamb = 25°C, voltage reference = V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	Min.	Typ.	Max.	Unit
PHASE FREQUENCY DISCRIMINATOR							
C_{OUT}	Output Capacitance					8	pF
$I_{OUT\ HI}$	Output Current	Source V_{OUT} = 2.7V V_{OUT} = 4.5V	 3V 5V	 – 200 – 500			 µA µA
$I_{OUT\ LO}$	Output Current	Sink VOUT = 0.3V V_{OUT} = 0.5V	 3V 5V	 200 500			 µA µA
I_{LEAK}	Leakage Current	Three state output $VPDT_X$, $VPDR_X$ = 0 or 5V	5V	– 50		50	nA
MCU INTERFACE INPUTS							
C_{IN}	Input Capacitance					8	pF
I_{IN}	Input Current	DC measured V_{IN} = V_{DD} or V_{SS}	3-5V	– 10		10	µA
V_{IH}	Input Voltage	High level ”1”	3V 5V	2.3 3.8			V V
V_{IL}	Input Voltage	Low level ”0”	3V 5V			0.7 1.2	V V
Fmax	Input Frequency	Maximum frequency at clock input	3-5V			500	KHz
T_W	Pulse width	Clock and Enable inputs	3V 5V	80 60			ns ns
T_{SU}	Set-up Time	Data to clock Enable to clock	3-5V 3-5V	100 200			ns ns
T_{HOLD}	Hold Time	Clock to data	3V 5V	80 40			ns ns
T_{REC}	Recovery Time	Enable to Clock	3V 5V	80 40			ns ns
DIGITAL OUTPUTS: $OUTT_X$, $OUTR_X$, MCU_{CLOCK}, LD							
C_{LOAD}	Output Load Capacitance					25	pF
$V_{OUT\ IH}$	Output Voltage	I_{OUT} = 0, High level ”1”	3V 5V	2.95 4.95			V V
$V_{OUT\ LO}$	Output Voltage	I_{OUT} = 0, Low level ”0”	3V 5V			0.05 0.05	V V
I_{OUTHI}	Output Current	Source V_{OUT} = 2.7V V_{OUT} = 4.5V	 3V 5V	 – 200 – 500			 µA µA
I_{OUTLO}	Output Current	Sink V_{OUT} = 0.3V V_{OUT} = 0.5V	 3V 5V	 200 500			 µA µA
THI	Output rise Time	C_{LOAD} = 25pF	3V 5V			200 100	ns ns
TLO	Output Fall Time	C_{LOAD} = 25pF	3V 5V			200 100	ns ns

Figure 1: Control Unit Block Diagram



Sumary of Internal Registers

Register	Adress			Number of Data Bits	Function
	A2	A1	A0		
R0	0	0	0	13	CIRCUIT CONTROL
R1	0	0	1	16	BINARY VALUE OF N1 = RX RATIO
R2	0	1	0	16	BINARY VALUE OF N2 = TX RATIO
R3	0	1	1	12	BINARY VALUE OF N3 = REF RATIO
R4	1	0	0	14	BINARY VALUE OF N4 = AUX REF RATIO

Description of Control Register

Bit	Name	Function
D12	TEST 1	Test Mode: See Table 1.
D11	TEST 2	
D10	TEST 3	
D9	AUXILIARY DATA SELECT	Set to 0 to select 3 wires serial data bus mode at the next pattern Set to 1 to select 4 wires serial data bus mode at the next pattern
D8	REFOUT/3	Set to 0, MCUCLOCK frequency = OSC.OUT frequency / 4 Set to 1, MCUCLOCK frequency = OSC.OUT frequency / 3
D7	TXCE	TX Counter Enable bit: if set to 0, TX amplifier, counter and PFD will be in power down mode and OUTTX pin will be set to 1.
D6	RXCE	RX Counter Enable bit: if set to 0, RX amplifier, counter and PFD will be in power down mode and OUTRX pin will be set to 1.
D5	RCE	Reference Counter Enable bit: if set to 0, ref counter will be in power down mode.
D4	ARCE	Auxiliary Reference Counter Enable bit: if set to 0, AUX Ref counter will be in power down mode
D3	MUX SELECT 1	Used to connect internally PFD inputs REFTX and REFRX to the chosen Ref frequency output: see Table 2.
D2	MUX SELECT 2	
D1	MUX SELECT 3	
D0	MUX SELECT 4	

Table 1.

TEST1	TEST2	TEST3	Status of output pin OUTTX	Status of output pin OUTRX	Status of TX and RX PFD
0	0	0	CONTROL BIT $\overline{TXCE}$	CONTROL BIT $\overline{RXCE}$	NORMAL OPERATION
0	0	1	INTERNAL POINT REFTX	INTERNAL POINT REFRX	TEST MODE NORMAL IUP
0	1	0	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE NORMAL IDOWN
0	1	1	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE I LEAKAGE
1	0	0	CONTROL BIT $\overline{TXCE}$	CONTROL BIT $\overline{RXCE}$	OPERATION WITH INCREASED IUP AND IDOWN
1	0	1	INTERNAL POINT REFTX	INTERNAL POINT REFRX	TEST MODE INCREASED IUP
1	1	0	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE INCREASED IDOWN
1	1	1	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE I LEAKAGE

Figure 2: Reference Frequency Diagram.

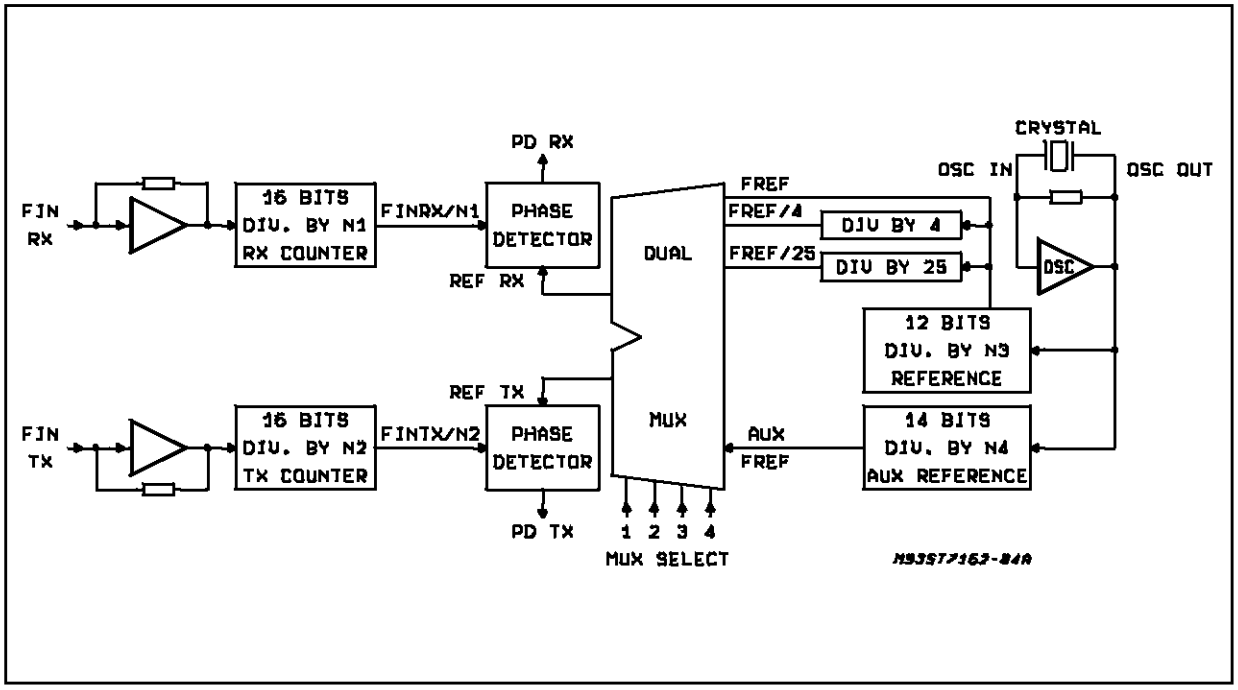


Table 2.

MUX SELECT 1	MUX SELECT 2	MUX SELECT 3	MUX SELECT 4	INPUT OF TX PFD REFTX CONNECTED TO INTERNAL POINT (see Note 1)	INPUT OF RX PFD REFRX CONNECTED TO INTERNAL POINT (see Note 2)
0	0	0	0	FREF	FREF
0	0	0	1	FREF	FREF/4
0	0	1	0	FREF	FREF/25
0	0	1	1	FREF	AUXFREF
0	1	0	0	FREF/4	FREF
0	1	0	1	FREF/4	FREF/4
0	1	1	0	FREF/4	FREF/25
0	1	1	1	FREF/4	AUXFREF
1	0	0	0	FREF/25	FREF
1	0	0	1	FREF/25	FREF/4
1	0	1	0	FREF/25	FREF/25
1	0	1	1	FREF/25	AUXFREF
1	1	0	0	AUXFREF	FREF
1	1	0	1	AUXFREF	FREF/4
1	1	1	0	AUXFREF	FREF/25
1	1	1	1	AUXFREF	AUXFREF

Note (1):
If the 12 bits REF. counter is disabled (R_{CE} control bit = 0) then the inputs of RX and TX PFD (REF TX and REF RX) are connected to internal point AUX REF.

Note (2):
If the 14 bits auxiliary reference counter is disabled (ARCE control bit = 0) then the internal point AUXFREF is replaced by FREF/ 25.

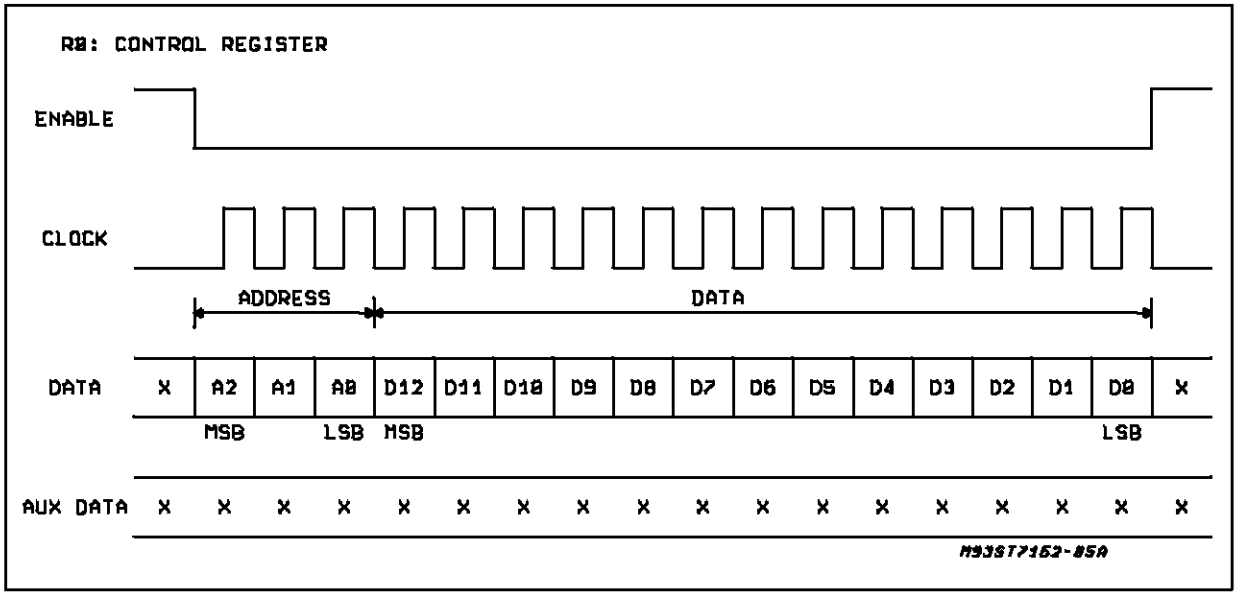
PROGRAMMING THE REGISTER (Figs 3 to 8)

When a Low level is present on the ENABLE input, information on the DATA and AUX DATA inputs are used to program the internal registers. Data are shifted at the rising edge of the clock input. First the 3 address bits of a register are sent, followed by 12 to 16 data bits, depending on the lenght of the register. The address is latched at the 3rd clock impulse following a falling edge at ENABLE input. This configuration allows to send various lenght patterns. Moreover, fixed patterns of 24 or 32 bits can be sent if dummy bits are inserted between the address bits and the first data bit. After the last data bit, a rising edge of the ENABLE input latches the information. When the V_{DD} supply is switched on, an internal circuit provides a reset of the control register bits. When the serial bus is not used, a Low level at clock input and a HIGH level at ENABLE inputs are applied.

PROGRAMMING THE 3/4 WIRES MODE

When the Auxiliary Data select bit of the control register is set to 1, the serial bus is switched in 4 wires mode at the next pattern. Then one or other of the 5 registers may be serially loaded by one or other of the DATA or AUX DATA inputs. When loading simultaneously 2 registers with different lenght, dummy bits are inserted between the address bits and the data bits of the shorter register (see fig. 8).

Figure 3: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

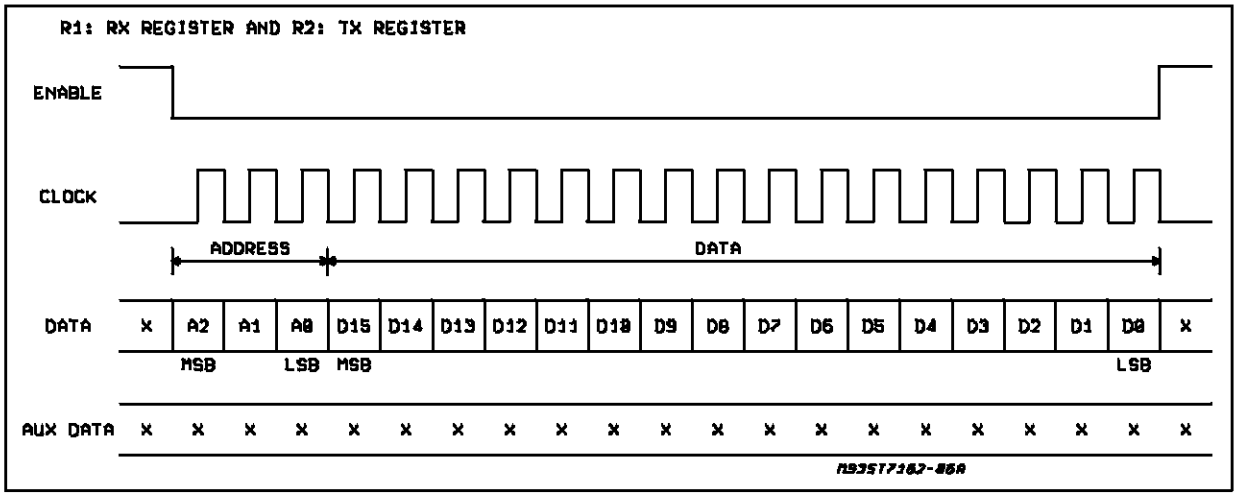
ADDRESS

A2	A1	A0
0	0	0

DATA

D12	TEST 1
D11	TEST 2
D10	TEST 3
D9	AUX. DATA SELECT
D8	REF OUT/3
D7	TX COUNTER ENABLE
D6	RX COUNTER ENABLE
D5	REF. COUNTER ENABLE
D4	AUX. REF. COUNTER ENABLE
D3	MUX SELECT 1
D2	MUX SELECT 2
D1	MUX SELECT 3
D0	MUX SELECT 4

Figure 4: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

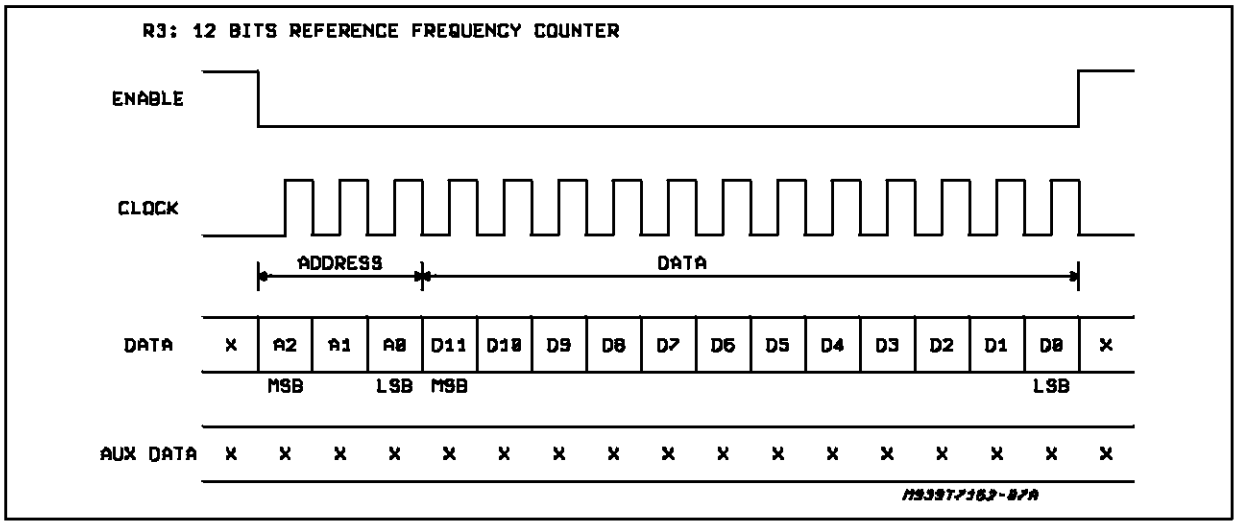
ADDRESS

A2	A1	A0	REGISTER
0	0	1	R1 : RX COUNTER
0	1	0	R2 : TX COUNTER

DATA

D15	MSB = 32768
⋮	
D0	LSB = 1

Figure 5: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

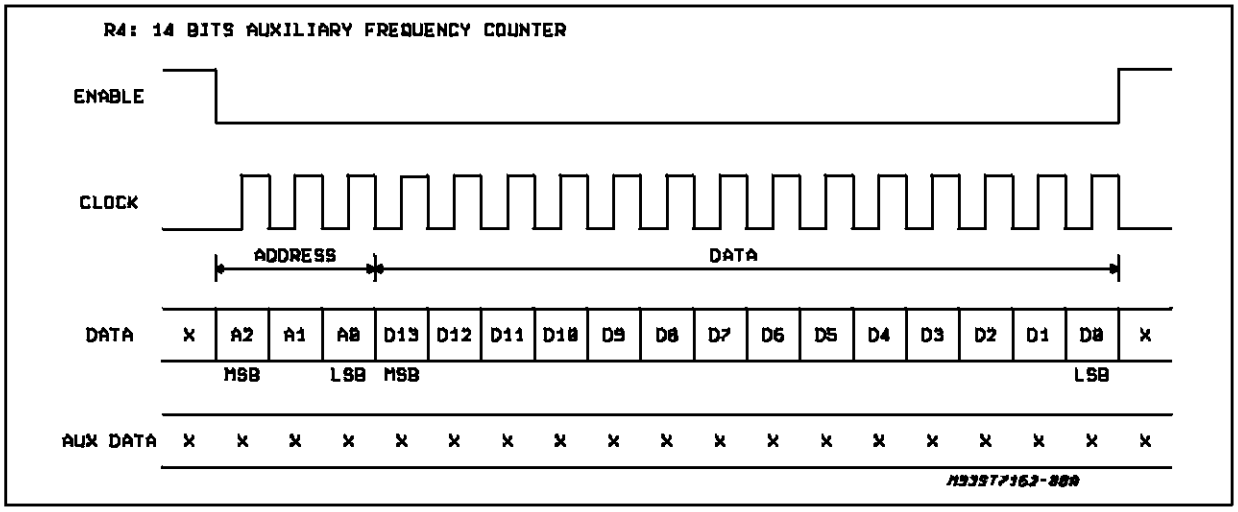
ADDRESS

A2	A1	A0	REGISTER
0	1	1	R3 : REF. COUNTER

DATA

D11	MSB = 2048
⋮	
D0	LSB = 1

Figure 6: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

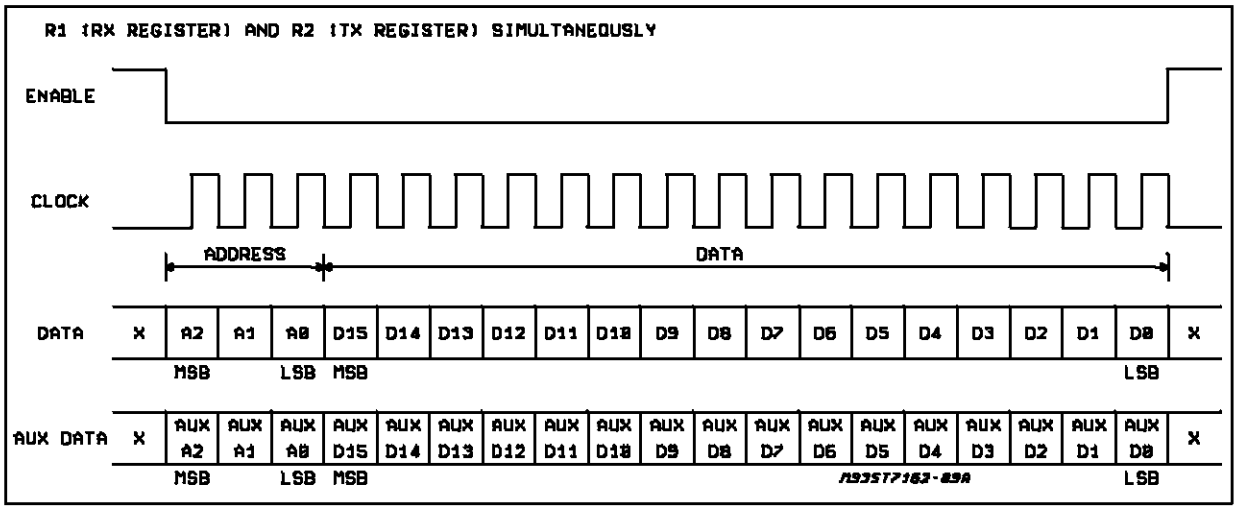
ADDRESS

A2	A1	A0	REGISTER
1	0	0	R4 : AUX REF. COUNTER

DATA

D13 : : : D0	MSB = 8192 LSB = 1

Figure 7: 4 Wires Serial Data Transmission Timing



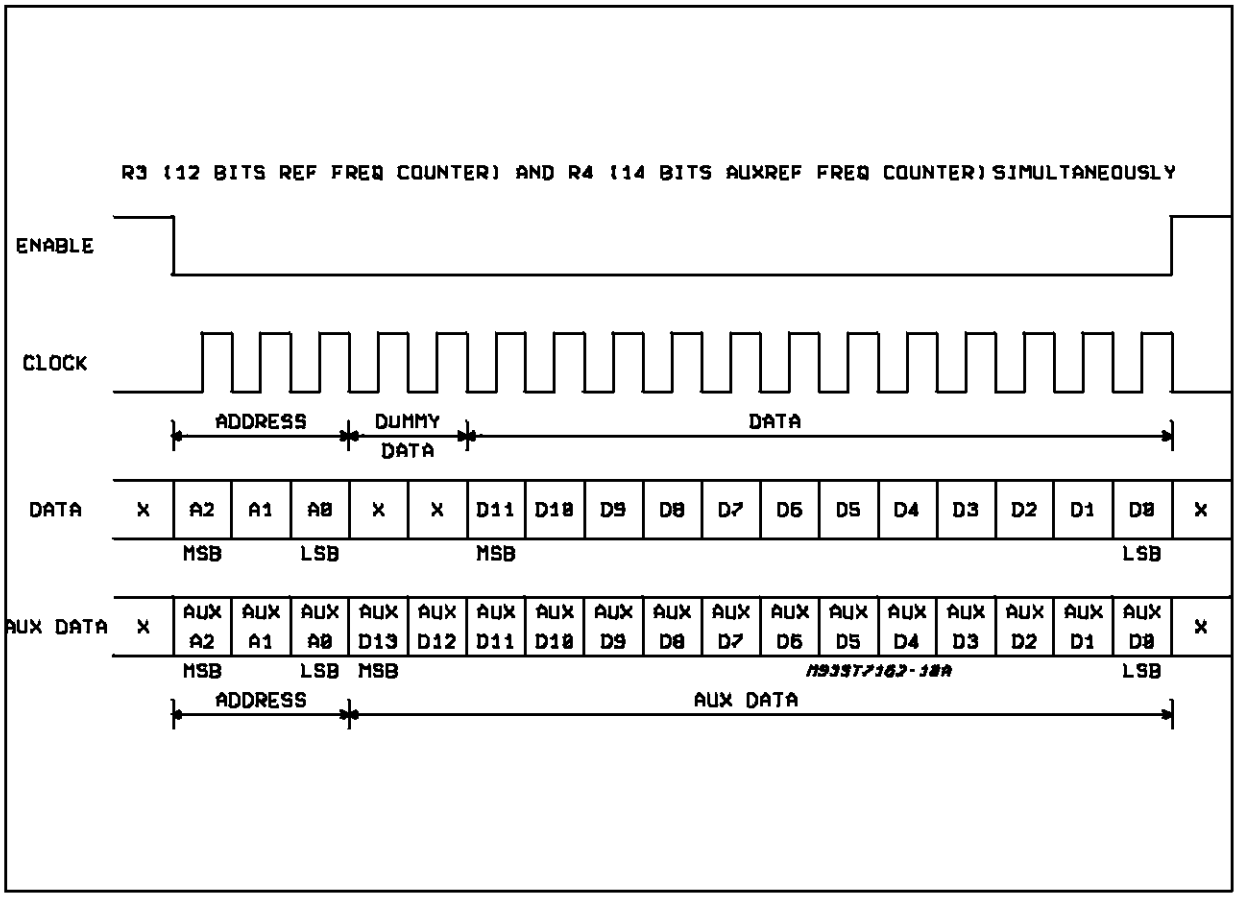
ADDRESS

A2 AUX A2	A1 AUX A1	A0 AUX A0	REGISTER
0	0	1	R1 : RX COUNTER
0	1	0	R2 : TX COUNTER

DATA

D15, AUX D15 : : : D0, AUX D0	MSB = 32768 LSB = 1

Figure 8: 4 Wires Serial Data Transmission Timing



X = DON'T CARE

ADDRESS

A2 AUX A2	A1 AUX A1	A0 AUX A0	REGISTER
0	1	1	R3 : REF COUNTER
1	0	0	R4 : AUX REF. COUNTER

DATA		AUX DATA	
D11	MSB = 2048	AUX D13	MSB = 8192
: : :		: : :	
D0	LSB = 1	AUX D0	LSB = 1

PFD DESCRIPTION (pin 10 & 15)

Outputs PDTX or PDRX produce an output pulse current, sourcing or sinking, whose width depends on the delay between falling edges of reference frequency and RF frequency divided. Simplified schematic of both PFD is described in figure 10. When the current output is off, PFD is in high impedance state. The voltage at PFD outputs pins depends on the loop filter and V_{CO} characteristics (Fig. 9)

Figure 9: PD Output Current vs. FIN / REF. Frequencies.

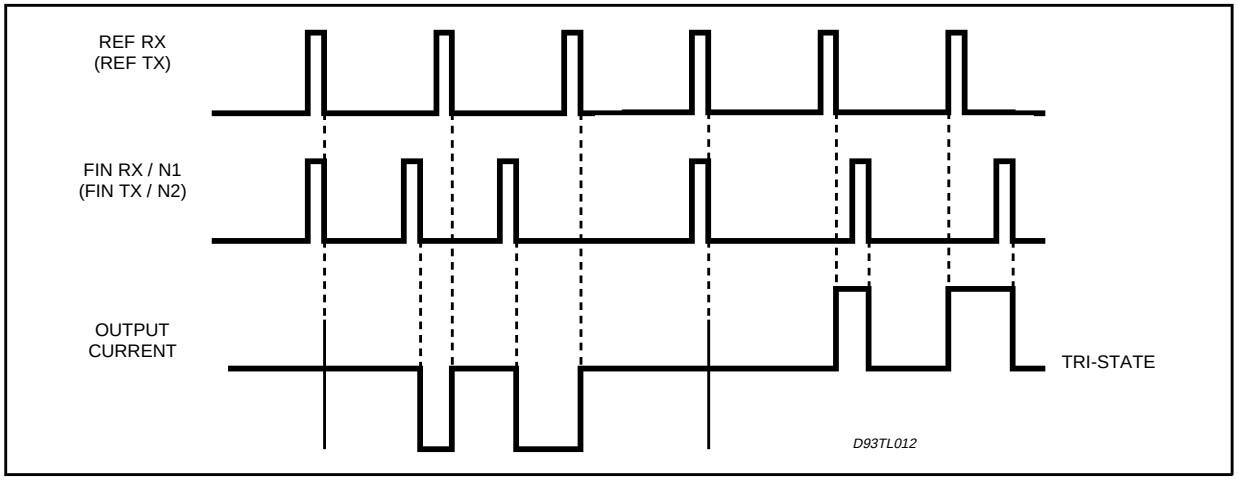
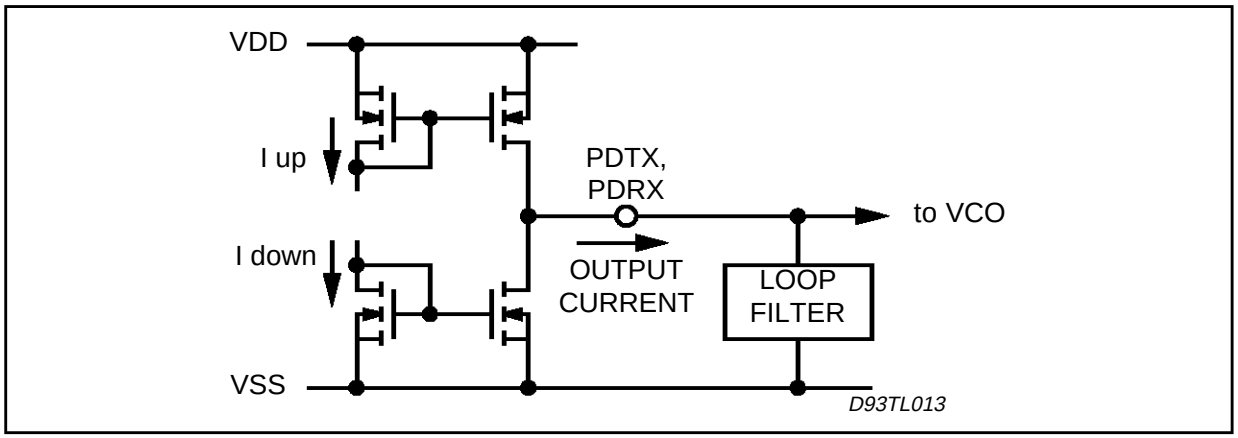


Figure 10: Simplified schematic of PFD outputs.



When the loop is locked, to prevent a dead area in the PFD gain due to switching delays, a very short phase offset is introduced in the loop, so the PFD output current show the following waveform Fig. 11.

Figure 11: PD output current in locked condition.

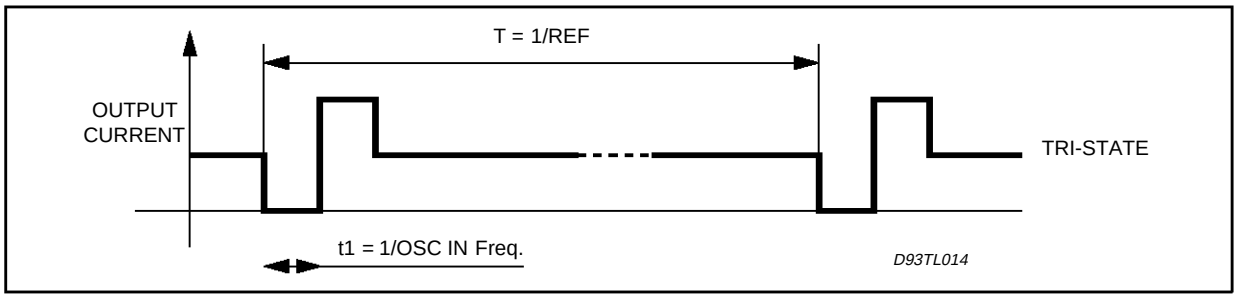


Figure 12: Switching diagrams.

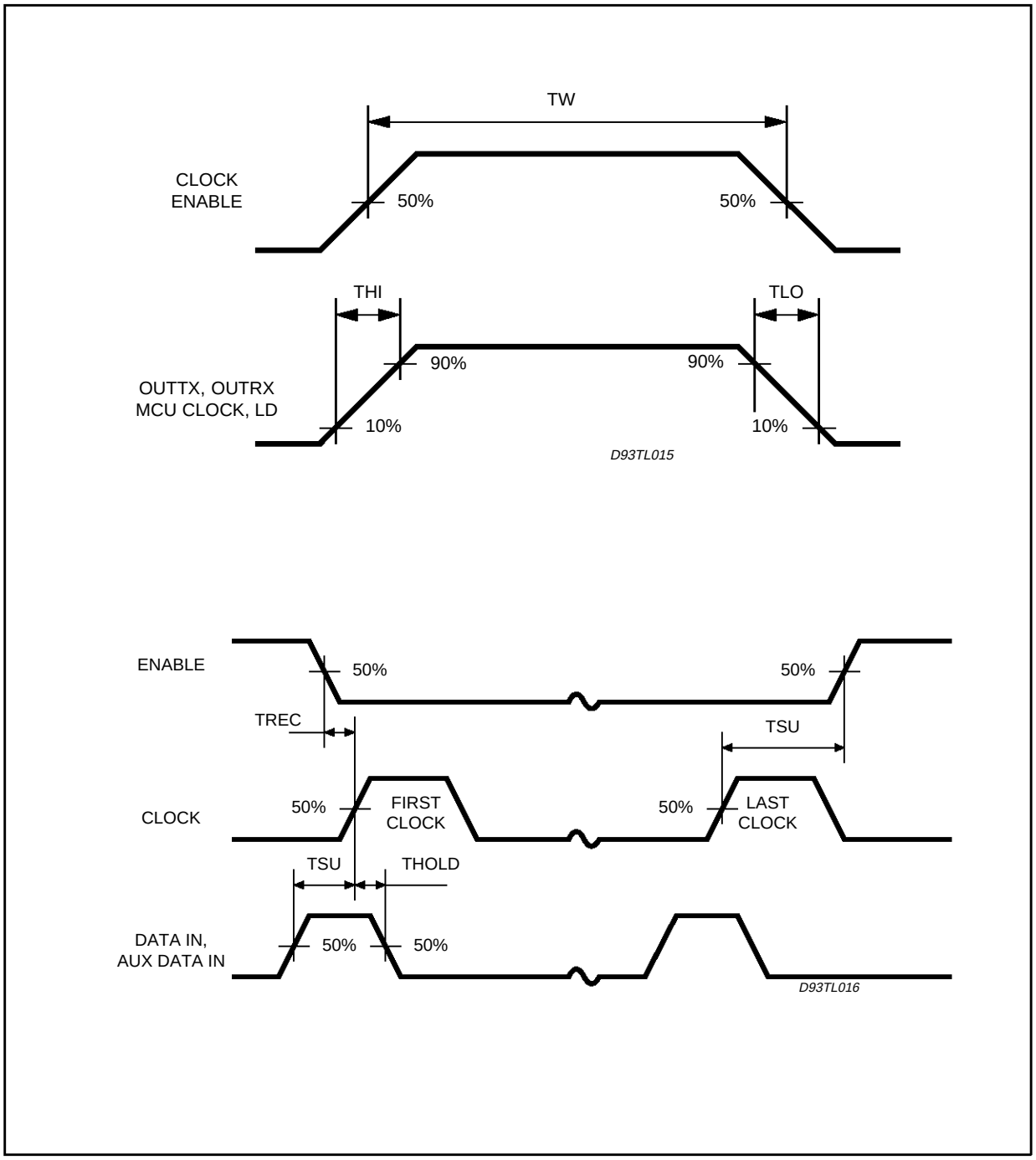
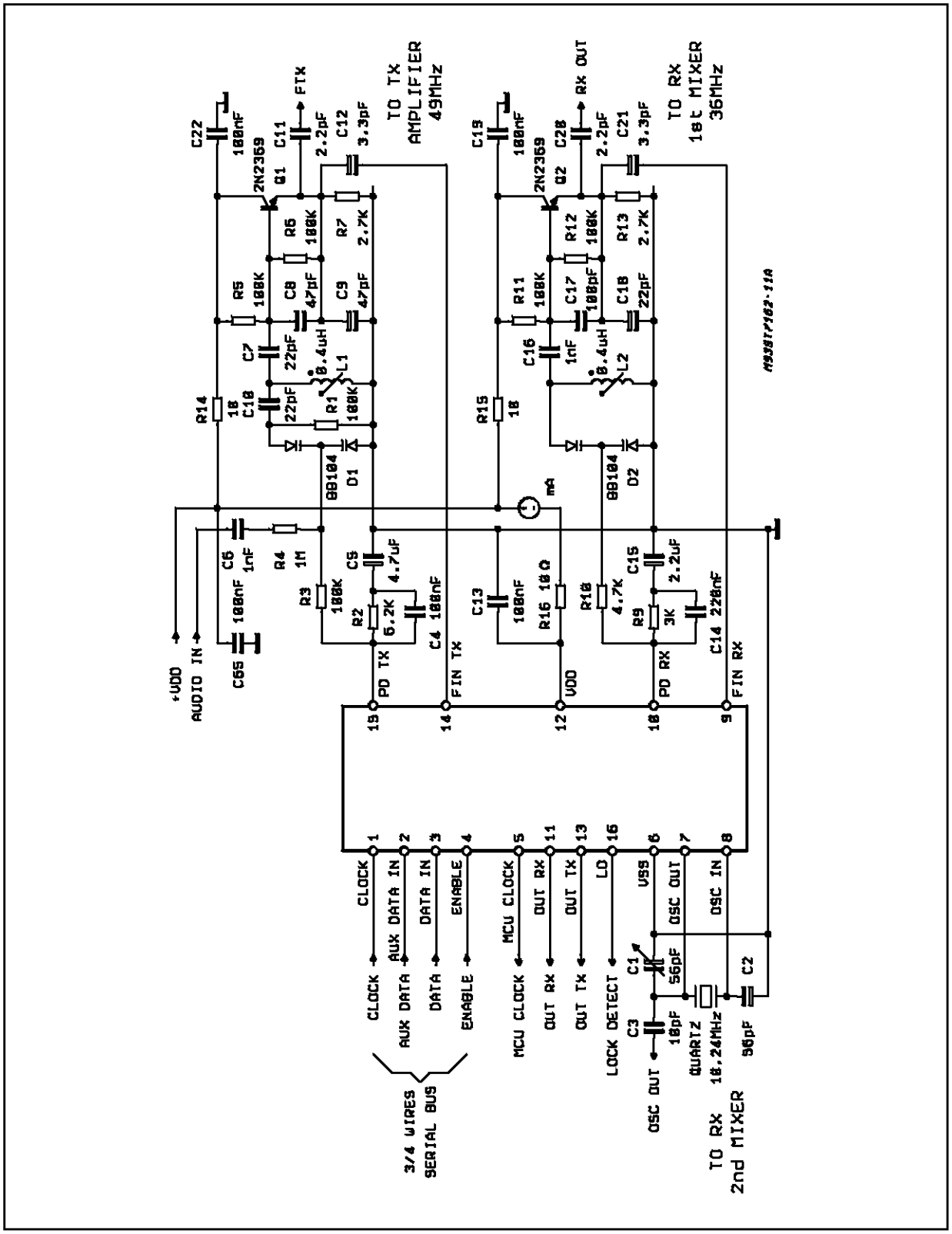
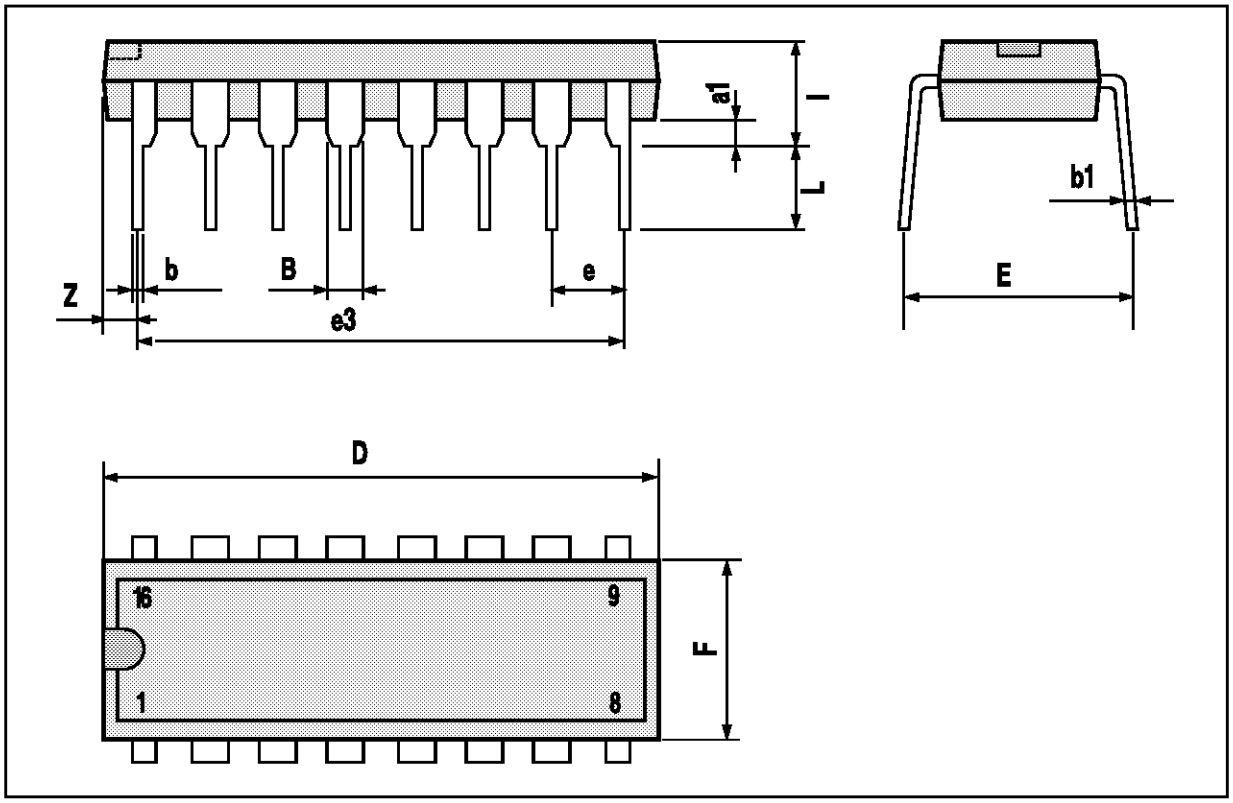


Figure 13: Test Circuit.



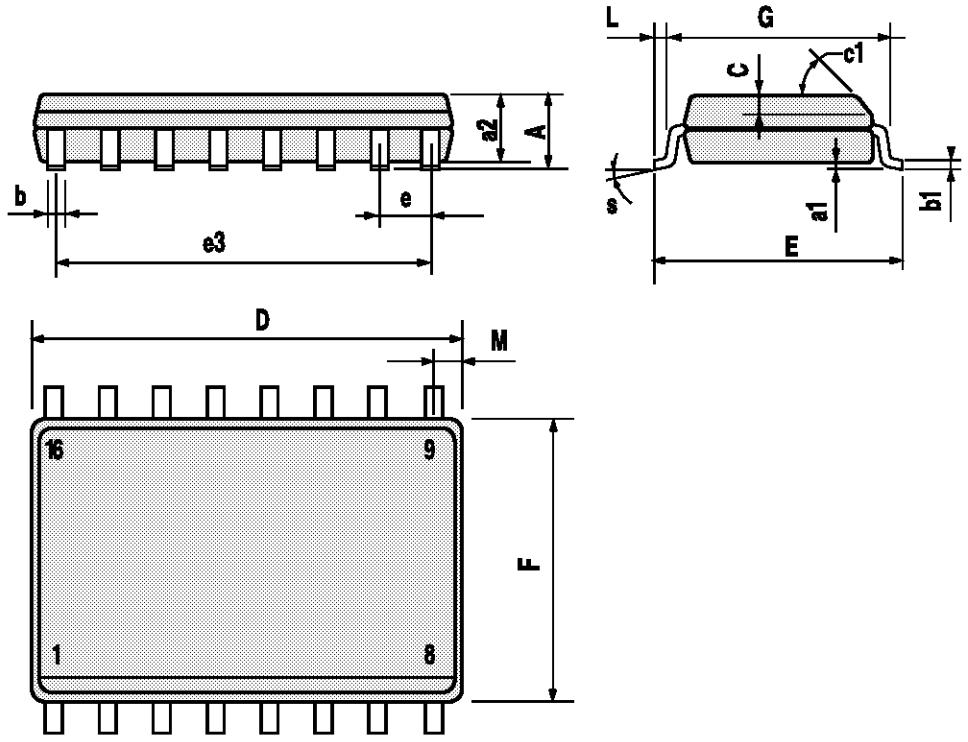
DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



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