SGS-THOMSON MICROELECTRONICS

ST7543

UNIVERSAL MODEM ANALOG FRONT-END (UMAFE)

- FULL ECHO CANCELLING CAPABILITY
- 16-BIT OVERSAMPLING A/D AND D/A CONVERTERS
  - Programmable down-sampling frequency : from 7200 to 16000Hz
  - Typical dynamic range : 89dB
  - Typical total harmonic distorsion : -90dB.
- ON CHIP REFERENCE VOLTAGE
- THREE PROGRAMMABLE DIGITAL FILTERS SECTIONS :
  - Tx interpolation filter
  - Rx decimation filter
  - Rx reconstruction filter (up to 14th order each coefficient loaded into RAM)
- ANCILLARY CONVERTERS FOR EYE-DIAGRAM MONITORING
- CLOCK SYSTEM BASED ON DIGITAL PHASE LOCKED LOOPS
  - Separate Tx DPLL and Rx DPLL
  - Terminal clock input for Tx synchronization
  - Bit, baud, sampling clock outputs
  - Clock rate up to 37MHz
- SINGLE OR DUAL SYNCHRONOUS SERIAL INTERFACE TO DSP
- SINGLE POWER SUPPLY VOLTAGE : +5V
- LOW POWER CONSUMPTION : OPERATING 180mW (for the nominal crystal frequency) low-power reset mode 5mW
- 1.2µm CMOS process
- 44-PIN PLCC or PQFP

GENERAL DESCRIPTION

The ST7543 is a single chip Analog Front-End (AFE) designed to implement high speed voice-grade Modems up to 19200 bps with echo cancelling capability.

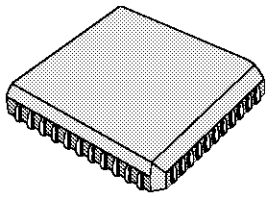
Associated with one or several Digital Signal Processors (DSP), such as the ST189XX family, it provides a powerful solution for the implementation of multi-mode Modems meeting CCITT (V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29, V.32, V.32 bis, V.33) and BELL (103, 202, 212 A...) recommendations. It is also well suited to new emerging applications involving bit rates up to 19200 bps.

The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and one for reconstruction). Oversampling and decimation ratios are equal to 128. Two additional 8-bit D/A converters allow eyediagram monitoring on a scope for modem performance adjustment (available in dual serial interface mode only).

Two independant clock generator systems are provided, one synchronized on the Tx rate and the other on the Rx rate.

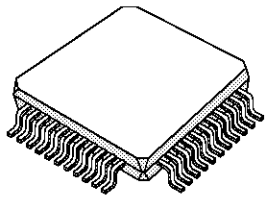
Two independant synchronous serial interfaces (SSI) allow several versatile ways of communication with standard DSPs.

To save power, e.g. in lap-top modem applications, the reset mode can be used to reduce the power consumption to 5mW.



PLCC44
(Plastic Package)

ORDER CODE : ST7543CFN



PQFP44
(Plastic Package)

ORDER CODE : ST7543CQFP

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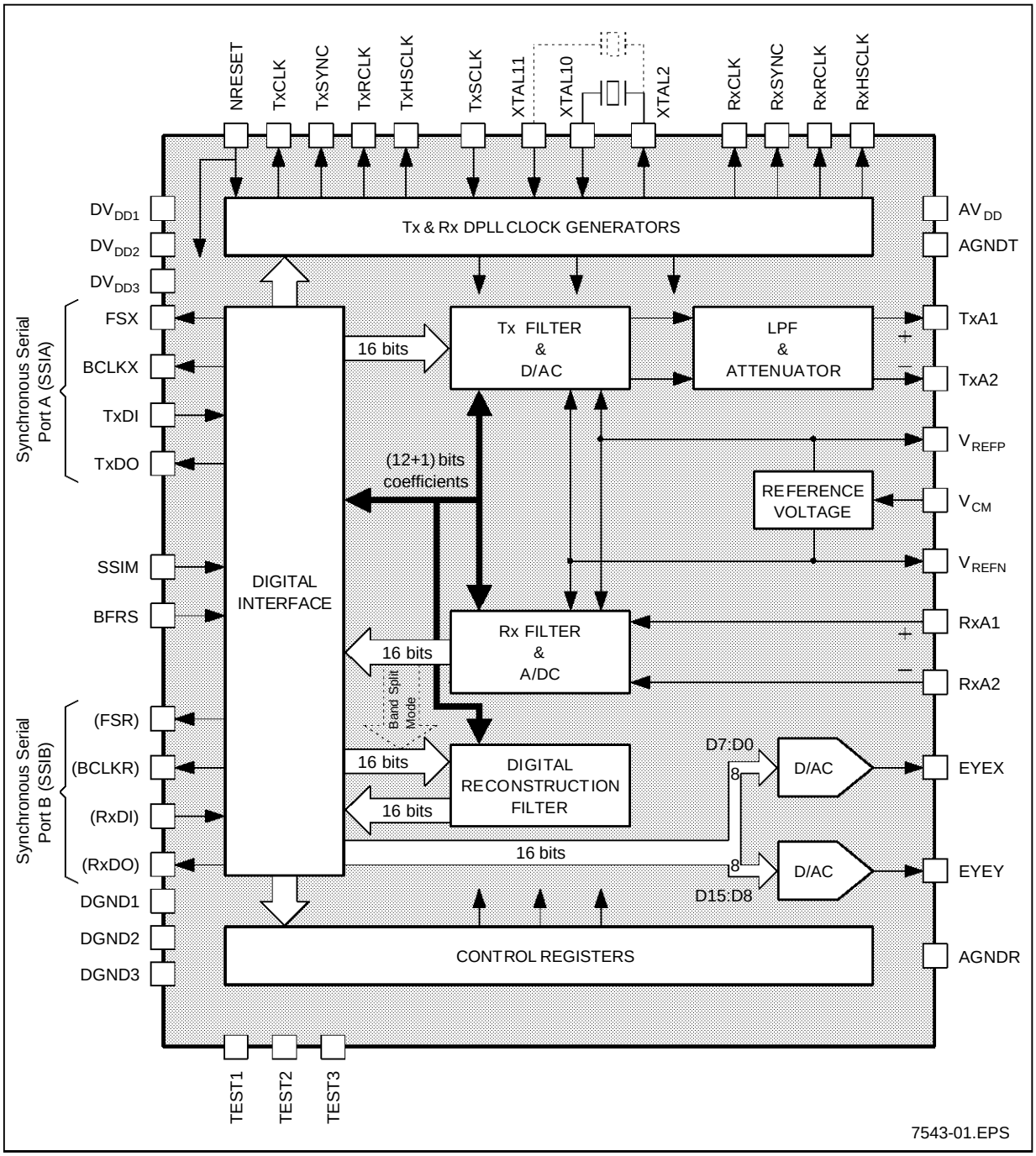
III. BLOCK DIAGRAM

Figure 1



IV. PIN CONNECTIONS (Top View)

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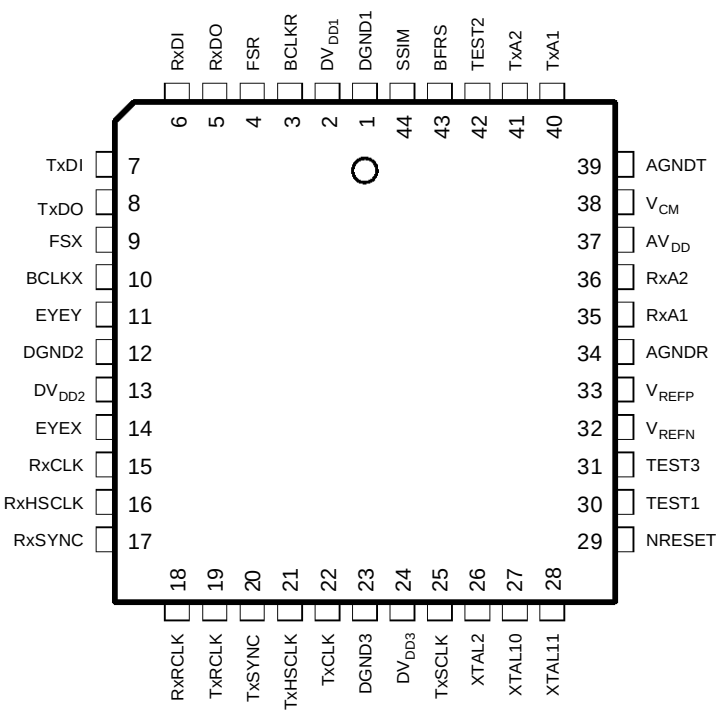

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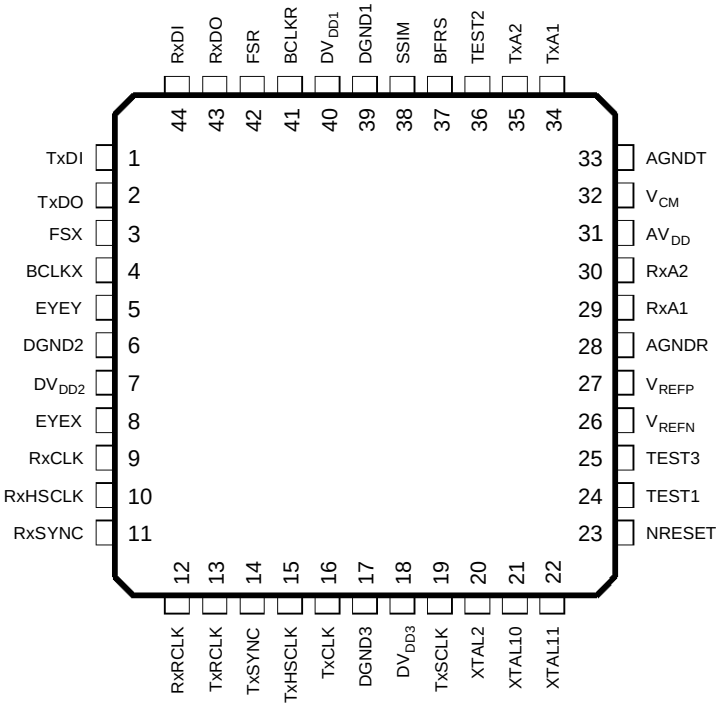

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V. PIN/OUT SUMMARY

PQFP	PLCC	Name	Description
39	1	DGND1	Digital Ground (0V).
40	2	DV_{DD1}	Positive Digital Power Supply. (+5V, ±5%).
41	3	BCLKR	Bit Clock Receive Output.
42	4	FSR	Frame Synchronization Receive Output.
43	5	RxDO	Serial Data Receive Output.
44	6	RxDI	Serial Data Receive Input.
1	7	TxDI	Serial Data Transmit Input.
2	8	TxDO	Serial Data Transmit Output.
3	9	FSX	Frame Synchronization Transmit Output.
4	10	BCLKX	Bit Clock Transmit Output.
5	11	EYEY	8 bit Y-D/AC Output for Eye Pattern display.
6	12	DGND2	Digital Ground (0V).
7	13	DV_{DD2}	Positive Digital Power Supply. (+5V, ±5%).
8	14	EYEX	8bit X-D/AC Output for Eye Pattern display.
9	15	RxCLK	Receive Bit Rate Clock Output.
10	16	RxHSCLK	Receive Highest Clock Output.
11	17	RxSYNC	Receive Synchronization Pulse Output.
12	18	RxRCLK	Receive Baud Rate Clock Output.
13	19	TxRCLK	Transmit Baud Rate Clock Output.
14	20	TxSYNC	Transmit Synchronous Pulse Output.
15	21	TxHSCLK	Transmit Highest Clock Output.
16	22	TxCLK	Transmit Bit Rate Clock Output.
17	23	DGND3	Digital Ground (0V).
18	24	DV_{DD3}	Positive Digital Power Supply. (+5V, ±5%).
19	25	TxSCLK	Transmit Synchronization Clock Input.
20	26	XTAL2	Crystal Output .
21	27	XTAL10	External Clock/Crystal Input 1.
22	28	XTAL11	External Clock/Crystal Input 2.
23	29	NRESET	Reset Input.
24	30	TEST1	Test Input. Must be tied to DGND.
25	31	TEST3	Test Input/output. Must be tied to DGND.
26	32	V_{REFN}	16 bit D/AC and A/DC Negative Reference Voltage.
27	33	V_{REFP}	16 bit D/AC and A/DC Positive Reference Voltage.
28	34	AGNDR	Analog Ground (0V).
29	35	RxA1	Receive Positive Analog Input.
30	36	RxA2	Receive Negative Analog Input.
31	37	AV_{DD}	Positive Analog Power Supply (+5V, ±5%).
32	38	VCM	Common Mode Voltage Input (2.5V, ±10%).
33	39	AGNDT	Analog ground (0V).
34	40	TxA1	Smoothing filter positive Output.
35	41	TxA2	Smoothing filter negative Output.
36	42	TEST2	Test Input/output. Must be tied to DGND.
37	43	BFRS	Bit Frame Rate Select Input.
38	44	SSIM	Serial Synchronous Interface Mode Input.

7543-01.TBL

VI. PIN DESCRIPTION.

VI.1. POWER SUPPLY (9 pins)

Analog V_{DD} Supply (AV_{DD})
This pin is the positive analog power supply (+5V ±5%) for the Transmit and the Receive sections.

Digital V_{DD} Supply (DV_{DD1},DV_{DD2},DV_{DD3})
These pins are the positive digital power supply (+5V, ±5%) for Transmit and Receive digital internal circuitry.

Analog Ground (AGNDT,AGNDR)
These pins, which are the analog ground return of the analog Transmit (Receive) section, are internally not connected to digital ground (DGND13).

Digital Ground (DGND1,DGND2,DGND3)
These pins are the ground connections for Transmit and Receive internal digital circuitry.

Note 1 : To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to AGND and DGND, respectively. The decoupling is intended to isolate digital noise from the analog section; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

Note 2 : All the ground pins must be tied together. Do the same for the supply pins (+5V). In the following section they are simply named GND and V_{DD}, respectively.

VI.2. CLOCK AND CONTROL SIGNALS (13 pins)

External Clock/crystal Inputs (XTAL10,XTAL11)
XTAL10 and XTAL11 inputs must be tied to external crystal(s) or external clock(s). These inputs are selected from the TxCtrl register. The maximum clock rate is 37.0MHz. XTAL10 is the default External Clock/Crystal input. It is mandatory to shortcircuit XTAL10 and XTAL11 when a single external crystal or clock generator is used (see Fig.16). The nominal master clock frequency is 18.432MHz.

Crystal Outputs (XTAL2)
This output is to be tied to one or two external crystals (see Fig.1). If an external clock is used, XTAL2 should be left open circuit.

Reset Input (NRESET)
This pin, when low completely resets the ST7543 clock system. NRESET must be tied to V_{DD} during normal operation. Access to the chip is disabled during power-on reset until the clock oscillator starts. The reset time duration can be increased by connecting the NRESET input to an external RC time-constant (see Fig.8). The Low-Power Reset Mode is actived when this pin is tied to GND (Operation of all clocks and the analog section is stopped).

Transmit Synchronization Clock Input (TxSCLK)
This pin can be connected to an external terminal clock to phase-lock the internal transmit clocks. It can be disabled under software control to allow the Tx DPLL to free run or phase lock on the RX clock system.

Transmit Bit Rate Clock Output (TxCLK)
This pin outputs the synchronous transmit bit clock selected for the MODEM.

Transmit Baud Rate Clock Output (TxRCLK)
This pin outputs the synchronous transmit baud Rate clock.

Transmit Synchronization Pulse Output (TxSYNC)
This pin outputs the synchronization transmit reset pulse. Combined with TxHSCLK clock it can be used to externally provide any synchronous transmit clock.

Transmit Highest Clock Output (TxHSCLK)
This pin outputs the highest synchronous transmit clock to provide any multiplexing clock.

Receive Bit Rate Clock Output (RxCLK)
This pin outputs the synchronous receive bit clock selected for the MODEM.

Receive Baud Rate Clock Output (RxRCLK)
This pin outputs the synchronous Receive baud rate clock.

Receive Synchronization Pulse Output (RxSYNC)
This pin outputs the synchronization receive reset pulse. Combined with RxHSCLK clock it can be used to externally provide any synchronous receive clock.

Receive Highest Clock Output (RxHSCLK)
This pin outputs the highest synchronous receive clock to give any multiplexing clock.

VI.3 SYNCHRONOUS SERIAL INTERFACES (SSIA,SSIB) (10 pins)

Serial Synchronous Interface Mode Input (SSIM)
This input activates one or both serial interfaces. When SSIM is tied to V_{DD}, both A and B ports are functional : port A (SSIA) is dedicated to the Transmit channel and port B (SSIB) is dedicated to the Receive channel.
When SSIM is tied to GND only port A (SSIA) is selected. In this case SSIA carries both Tx and Rx Signals.

Bit Frame Rate Select Input (BFRS)
This input selects one of the two possible bit frequencies for the BCLKX and BCLKR clocks. When BFRS is tied to V_{DD} the BCLKX (BCLKR) frequencies are 128 times the FSX (FSR) frequencies. When BFRS is tied to GND, BCLKX (BCLKR) frequencies are 64 times the FSX (FSR) frequencies.

Frame Synchronization Transmit Output (FSX)
This output clock is the Transmit Frame synchronization pulse signal of the SSIA port which has nominal frequency equal to the transmit sampling frequency. This pulse indicates the beginning of the 16-bit serial words on the serial data input/output port A.

Bit Clock Transmit Output (BCLKX)
This output pin provides the serial bit clock for the SSI port A. The BCLKX frequency equals 128 or 64 times the Transmit sampling frequency, depending on the Bit Frame Select Input (**BFRS**).

Serial Data Transmit Input (TxDI)
This input receives word-oriented serial data. Data is loaded from TxDI into the Transmit Shift Register (TSRIN) on the falling edge of BCLKX and transfered to the Transmit Buffer Register (TBRIN) when a complete 16-bit word has been received. Data is assumed to be received MSB first.

Serial Data Transmit Output (TxDO)
This output sends word-oriented serial data. The 16-bit Data Word loaded in the Transmit Buffer Register (TBROUT) is transfered to the Transmit Shift Register (TSROUT) and clocked out of TSROUT on the rising edge of BCLKX. Serial words are transmitted MSB first.

Frame Synchronization Receive Output (FSR)
This output clock is the Receive Frame synchronization pulse signal of SSI port B which has frequency equal to the receive sampling frequency. This pulse is used to indicate the beginning of serial words on the serial data input/output port B.

Bit Clock Receive Output (BCLKR)
This output pin provides the serial bit clock for the SSI port B. The BCLKR frequency is 128 times (or 64 times, selected by **BFRS**) the receive sampling frequency.

Serial Data Receive Input (RxDI)
This input receives word-oriented serial data. Data is clocked from RxDI into the Receive Shift Register (RSRIN) on the falling edge of BCLKR and transfered to the Receive Buffer Register (RBRIN) when a complete 16-bit word has been received. Data is assumed to be received MSB first.

Serial Data Receive Output (RxDO)
This output sends word-oriented serial data. The 16-bit Data Word loaded in the Receive Buffer Register (RBROUT) is transfered to the Receive Shift Register (RSROUT) and clocked out of RSROUT on the rising edge of BCLKR. Serial words are transmitted MSB first.

VI.4. ANALOG INTERFACE (9 pins).

D/AC and A/DC Positive Reference Voltage Output (V_{REFP})
This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 2.5V. V_{REFP} should be externally decoupled with respect to V_{CM} (see Fig. 15).

D/AC and A/DC Negative Reference Voltage (V_{REFN})
This pin provides the Negative Reference Voltage and should be externally decoupled with respect to V_{CM}.

Common Mode Voltage Input (V_{CM})
This input pin is the common mode Voltage (AV_{DD} - AGND)/2 and should be externally provided. This input must be decoupled with respect to GND.

Smoothing Filter Positive Output (TxA1)
This pin is the positive output of the fully differential analog smoothing filter.

Smoothing Filter Negative Output (TxA2)
This pin is the negative output of the fully differential analog smoothing filter.
Outputs TxA1 and TxA2 provide analog signals with maximum peak to peak amplitude $2*V_{REF}$, and must be followed by an external continuous time two pole smoothing filter (see Fig. 14). The external filter follows the internal single pole switch capacitor filter (see section VII2.2). The cut-off frequency of the external filter must be greater then 2.0 + Fsx, so that the combined frequency response of both the internal and external filters is flat in the pass band.

Receive Positive Analog Input (RxA1)
This pin is the differential positive A/DC Input.

Receive Negative Analog Input (RxA2)
This pin is the differential negative A/DC Input.
These analog inputs (RxA1,RxA2) are presented to the Sigma-Delta modulator, the analog input peak to peak signal range must be less than $2*V_{REF}$, and must be preceded by an external continuous-time single pole anti-aliasing filter (see Fig.14). The cut-off frequency of the filter must be lower than one half the transmit over-sampling frequency (TxOSCK).

D/AC Output for Eye Pattern (EYEX,EYEY)
These pins are the outputs of two 8-bit digital to analog converters used to monitor, on a CRT, the X and Y quadrature signals of the eye pattern of the demodulated signal. EYE D/ACs are only accessible from Rx port B.

VI.5. TEST PURPOSE (3 pins)

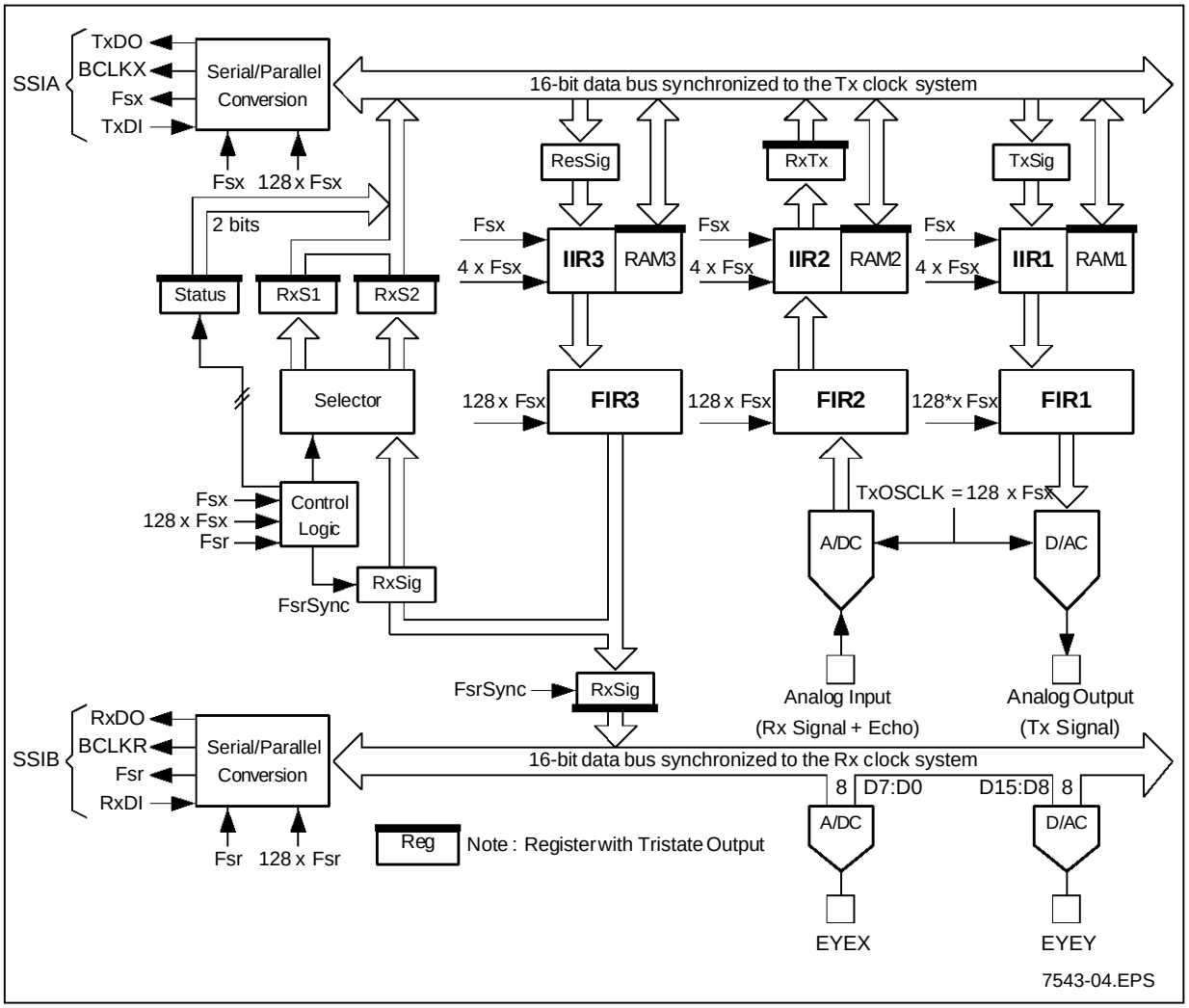
Test Input/output (TEST1,TEST2,TEST3)
These pins are used for test purpose and should be tied to GND during normal operation.

VII. FUNCTIONAL DESCRIPTION

VII.1. SIGNAL TRANSFER BLOCK DIAGRAM

The ST7543 Block Diagram (see Figure 2) illustrates three paths as follows : The **Transmit D/A Section**, the **Receive A/D section** and the **Receive Reconstruction section**.

Figure 2



VII.2. TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter.

VII.2.1. Interpolation Filters

The 128 fold oversampling is performed by two cascaded digital interpolating filters : IIR1 and FIR1. They are sampled at 4 x Fsx (four times the transmit sampling clock) and 128 x Fsx, respectively.

VII.2.1.1. PROGRAMMABLE INTERPOLATION FILTER (IIR1)

IIR1 is an infinite impulse response interpolating filter.

The purpose of this digital filter is to interpolate 4-times the digital signal coming from the DSP (TxSig). This filter is sampled at 4-times the basic sampling frequency, e.g. 7200 x 4Hz, and must exhibit, as a minimum, a low-pass section which is mandatory to remove replicas above half the sam-

pling frequency (e.g. 3600Hz) (see Fig.12).
The digital samples are encoded in 16-bit two's complement format.
The IIR1 filter is a cascade of seven biquads (see Fig. A1). The filter coefficient are loaded into the associated RAM (38 x 16). Each coefficient is coded into 12bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function (see Annexe A). This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. high pass section or equalization, matched to a particular application.

VII.2.1.2. FIR FILTER (FIR1)
FIR1 is a finite impulse response interpolating filter. Its input sampling frequency is 4*Fsx and its interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(Z) = \left(\frac{1 - Z^{-32}}{32\left(1 - Z^{-1} \right)} \right)^3$$

with $Z = \exp(j2\pi F/128 \times Fsx)$

VII.2.2. D/A Converter
The 128-times oversampled D/A converter includes a second order digital noise shaper,a one bit D/A converter and a single pole analog low-pass filter. The gain of the last output stage can be programmed to 0dB,-6dB or infinite attenuation. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc_{-3dB} = 128 \times Fsx/(2 \times \pi \times 10) \cong 2.04\ Fsx$$

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components (see Fig.14).
At least 84dB dynamic range can be obtained for a signal in the frequency band 300 → 3400Hz.

VII.3. RECEIVE A/D SECTION
The different functions included in the Rx A/D section are detailed hereafter. The format used at the digital interfaces of the Rx channel is two's complement encoded 16-bit.

VII.3.1. A/D Converter
The 128-times oversampled A/D converter is based on a second order sigma-delta modulator. The dynamic range obtained for a signal spectrum limited to the 300-3400Hz telephone band, is typically 84dB.

VII.3.2. Decimation Filters
The 128 ratio decimation is performed by two interpolating digital filters : FIR2 and IIR2, which are sampled at 128 x Fsx and 4 x Fsx, respectively .

VII.3.2.1. Fir Filter (FIR2)
FIR2 is a finite impulse response decimating filter. Its sampling frequency is 128*Fsx and its decimation ratio is 32. The Z transfer function of this FIR is :

$$H(Z) = \left(\frac{1 - Z^{-32}}{32\left(1 - Z^{-1} \right)} \right)^3$$

with $Z = \exp(j2\pi F/128 \times Fsx)$

VII.3.2.2. PROGRAMMABLE DECIMATION FILTER (IIR2)
IIR2 is an infinite impulse response filter. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency (e.g. 3600Hz) (see Fig.12bis). The output of the IIR2, RxTx, will be processed by the DSP. In band split mode (see Table 19), RxTx becomes the input signal to IIR3. The RxTx will always be available on serial interface A (SSIA in Fig.2)
The IIR2 filter is a cascade of seven biquads. The filter coefficients are loaded into the associated RAM (38 x 16).
The filter transfer function has been made programmable in order to meet specific requirements. The sampling frequency is 4-times the down-sampling frequency selected for the Tx section (e.g. 7200 x 4 Hz).
To support echo cancelling applications, the clocks used for the A/D converter and the decimation filters are synchronized on the Tx system clock, i.e. on the Tx rate. It must be pointed out that using a single clock system in A/D and D/A conversions is important for reducing induced noise.
The 12+1 bit filter coefficients are loaded in the internal RAM2 and must be loaded from the serial bus. All 38 coefficients have to be loaded to implement an IIR transfer function.

VII.3.3. Eye-diagram Display
Two 8-bit digital to analog converters are provided to monitor, on a CRT, the X and Y quadrature signals of the eye pattern related to the demodulated signal. The format of the data input is MSB first, 8-bit two's complement, and most significant byte for EYEY sample and least significant byte for the EYEX sample. The reference voltage of these two converters is the power supply voltage V_{DD}.

VII.4. RECEIVE RECONSTRUCTION SECTION

As the Rx channel sampling is synchronized to the Tx system clock, it is necessary to reconstruct the Rx signal in order to get samples synchronized to the Rx symbol rate recovered in the demodulator.
The function of the reconstruction filter (IIR3 and FIR3) is to over sample, by 128 x Fsx, the receive signal after echo cancellation (ResSig) coming from the DSP. The over sampled signal is then down sampled at Fsr rate to make it available to DSP as RxSig at SSIB or RxS1/RxS2 at SSIA (see sections VIII.1 and VIII.2). The down sampling process does not introduce significant error.
The transfer function of the first section of the reconstruction filter is programmable in the same way as the Tx and Rx IIR filters previously described.

VII.4.1. Programmable Interpolation Filter (IIR3)

IIR3 is an infinite impulse response interpolating filter.
The purpose of this digital filter is to interpolate 4-times the digital signal coming from the DSP. This filter is sampled at 4-times the basic sampling frequency, e.g. 7200 x 4 Hz (see Fig.12).
The digital samples are encoded in 16-bit two's complement format.
The IIR3 filter is a cascade of seven biquads. the filter coefficients are loaded into the associated RAM (38 x 16). Each coefficient is coded into 12bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function.
This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. highpass section or equalization, matched to a particular application. For example, in a band-split MODEM application, the first section can be a wide channel band-pass filter (allowing the DSP to supervise boundary audio tones) and the second section can be dedicated to high band and low band splitting.

VII.4.2. Fir Filter (FIR3)

FIR3 is a finite impulse response interpolating filter. Its input sampling frequency is 4 x Fsx and the interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(Z) = \left(\frac{1 - Z^{-32}}{32\left(1 - Z^{-1}\right)} \right)^3$$

with $Z = \exp(j2\pi F/128 * Fsx)$

VII.5. CLOCK GENERATION

Master clock is obtained from either a crystal tied between pins XTAL10 (or XTAL11) and XTAL2 or from an external signal connected to the XTAL10 (or XTAL11) pin; in the latter case, the XTAL2 pin should be left open circuit.
Two external crystals (or two external master clock signals), selected one at a time, can be used to cope with complex applications. It is mandatory to short-circuit XTAL10 and XTAL11 when a single external crystal or clock generator is used
To insure the start-up of the ST7543, the XTAL10 input must always be tied to a crystal or an external clock signal, as that pin is automatically selected when powering-on the device.
The different transmit (Tx) and Receive (Rx) clocks are obtained by master clock frequency division in several programmable counters. Tx and Rx clocks can be synchronized on external signals by performing phase shifts in the frequency division process (equivalent to adding or suppressing master clock transitions at the counter inputs). Two independant digital phase locked loops (DPLL) are implemented using this principle , one for Tx and one for Rx.
Several values can be chosen for the master clock frequency. The three frequencies given in table 1 are of particular interest, as they are compatible with standard Modem frequencies.
Note : In the remainder of the datasheet unless otherwise indicated, 18.432MHz will be considered as the nominal master clock frequency. The maximum master clock frequency is 32MHz.

Table 1.

Crystal Frequency	Symbol Rate Frequency	Bit Rate (bps)		Sampling Frequency
F_Q (MHz)	Fbaud (baud)	All up to 14400	others	Fsx, Fsr (Hz)
18.432	2400	Yes	16800/19200 24000	3 or 4 times Fbaud
29.4912	2400 2743 3200	Yes	16800/19200 21600/24000 19200 16000/19200 22400/25600	3 or 4 times Fbaud
25.8048	2400 2800	Yes	19200 16800/19600 22400	3 or 4 times Fbaud

VII.5.1. Transmit DPLL

Frequency control of the Tx clock system (fig. 9) is obtained by performing additional up or down counting steps in the three input dividers M, N and P. These elementary phase shifts of one master clock period are repeated at either the rate of the Fsx clock, or half that rate, depending on the required capture and tracking ranges (see table 24). The average updated frequency then varies between the following limits :

$$f_Q - f_{SHIFT} \leq f_{average} \leq f_Q + f_{SHIFT}$$

Where fQ is the master clock frequency and f_{SHIFT} equals Fsx or Fsx/2 (see table 24).

The TxDPLL phase comparison which determines lead or lag decisions, is simply obtained by sampling the synchronization clock, TxSCLK or RxCLK, on the falling edges of an internal clock taken from the division chain, f_{COMP} (see table 23). f_{COMP} frequency must be an integer submultiple of the synchronization clock. This frequency determines the Tx jitter magnitude. It is usually chosen to be equal to the baud rate frequency. Only phase shifts of the same sense (lead or lag) are performed during each f_{COMP} period. The actual phase shifts during f_{COMP} period are given by the ratio f_{SHIFT}/f_{COMP}. These phase shifts are performed at the inputs of the M, N, and P dividers to lock the DPLL to the synchronization signal (see Table 20). The Tx clock system may also run freely without any phase shift. In this case, the TxSCLK input is no longer active.

The DPLL capture and tracking range equal $\pm f_{SHIFT}/f_Q$. They have to be greater than ±200ppm to comply with the CCITT recommendations. f_{SHIFT} = Fsx/2 minimizes the jitter. Because of this, there is a trade-off between higher capture and tracking ranges and lower jitter.

Ex : f_Q = 18.432MHz and f_{SHIFT} = Fsx = 7200Hz.

Capture and tracking ranges =

$\pm f_{SHIFT}/f_Q = \pm$ 7200Hz/18.432MHz = ± 390.6ppm

VII.5.2. Transmit Clocks

The ST7543 provides three synchronous programmable Tx modem clocks :

- transmit bit rate clock TxCLK
- transmit baud rate clock TxRCLK
- transmit highest synchronous clock TxHSCLK, useful to implement external clocks (e.g. extra divisors) if needed.

The outputs of the latter two clocks, can be disabled when not used, but a correct baud rate frequency must be programmed as the f_{COMP} clock frequency depends on it.

The Tx clock system provides the sampling and oversampling clocks as well as the bit and synchro clocks (BCLKX and FSX) used by the serial interface A (SSI-A) described in section VIII.

The counters of the Tx clock system (fig. 9) are automatically reset when powering-on the ST7543 and when the NRESET input level is low. They can also be reset, under software control (see Tables 20-21), during the following conditions :

- on the next falling edge of the TxSCLK terminal clock or of the RxCLK receive bit rate clock (SST bit table 20).
- on the next falling edge of the TxRCLK transmit baud rate clock (SYT bit table 21).

The former gives the capability to speed-up the Tx DPLL synchronization; the latter is useful to fix the phase of the bit rate clock with respect to the baud rate clock, in particular after each modification of the bit rate value.

The internally generated pulse resetting of the Tx counters is output at the TxSYNC pin in order to synchronize external functions using the TxHSCLK clock.

VII.5.3. Receive DPLL

The synchronization of the Rx counters delivering the Rx clocks (fig. 10) is performed by addition or suppression of master clock periods under DSP control. In this case, the phase comparison function of the RxDPLL is implemented in the associated DSP recovering the received symbols.

Two types of phase shift control are provided in the ST7543 :

- a coarse phase lag of programmable magnitude, obtained from the suppression of 64 to 4096 successive master clock transitions (see Table 35). This control is to be used to reduce the RxDPLL locking time.
- a fine phase lead or lag of programmable magnitude (i.e. 8 to 32 master clock periods or one Tx oversampling clock period) continuously used to implement the phase control loop (see Table 34). Each elementary phase shift, corresponding to an addition or a subtraction of one master clock transition, is synchronized on to internal clock with frequency 128 times the Rx sampling frequency Fsr. A phase shift is ,therefore, always completed in less than one Fsr period.

Even after both the coarse and fine phase shift programming, the bit and baud clocks my not be synchronized. To ensure synchronization, the receive clock (Rxclk) needs a soft reset (bit D2 in RxCR3 should be set) (see Table 36).

VII.5.4. Receive Clocks

The ST7543 provides three synchronous Rx Modem clocks :

- receive bit rate clock RxCLK
- receive baud-rate clock RxRCLK
- receive highest synchronous clock, RxHSCLK useful to generate external clocks if needed.

The RxRCLK and RxHSCLK outputs can be disabled when not used.

The bit rate clock frequency of the Rx modem can be chosen to be different from its Tx counterpart, provided Rx to Tx loopback is not required.

The Rx clock system also provides the sampling and oversampling clocks as well as the bit and synchro clocks (BCLKR and FSR) used by the serial interface B (SSI-B) described in section VIII.

The digital reconstruction filter implemented in the ST7543 makes possible the choice of a receive nominal sampling frequency to be different from the transmit nominal sampling frequency.

The counters of the Rx clock system (fig. 10) are reset when either powering-on the ST7543 or the NRESET input is low. They can also be reset, under software control, on the next falling edge of the RxRCLK receive baud rate clock (SYR bit Table 36) : this feature is used to fix the phase of the bit rate clock with respect to the baud rate clock, e.g. after each modification of the bit rate value.

The internally generated pulse resetting the Rx counters is output at the RxSYNC pin in order to be used with the RxHSCLK clock.

VII.6. SERIAL INPUT/OUTPUT SYNCHRONOUS INTERFACES

The MAFE has two synchronous serial interface ports, SSIA and SSIB. They allow independent transmit and receive paths. Through the two serial ports, the MAFE can talk to various digital signal processors. The various serial interface signals and internal registers are given below :

SSI Port A (SSIA)

- Transmit Frame Synchronization output (Fsx)
- Transmit Bit clock output (BCLKX)
- Transmit Serial Data input (TxDI)
- Transmit input Shift Register (TSRIN)
- Transmit input Buffer Register (TBRIN)
- Transmit output Shift Register (TSROUT)
- Transmit Buffer Register output (TxDO)

SSI Port B (SSIB)

- Receive Frame Synchronization output (Fsr)
- Receive Bit clock output (BCLKR)
- Receive Serial Data input (RxDI)
- Receive input Shift Register (RSRIN)
- Receive input Buffer Register (RBRIN)
- Receive output Shift Register (RSROUT)
- Receive Buffer Register output (RxDO)

Mode Inputs :

- Serial Synchronous Interface Mode (SSIM)
- Bit Frame Rate Select (BFRS)

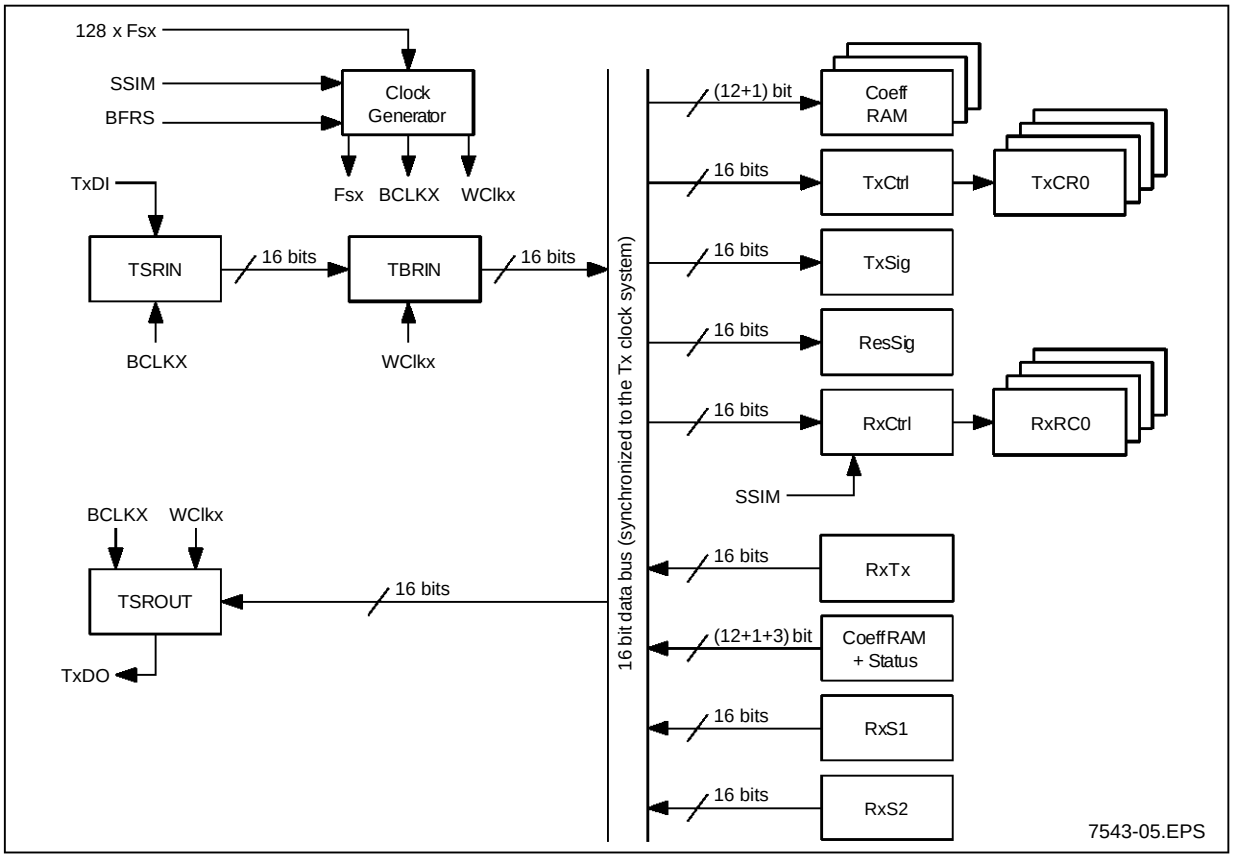
With SSIM input, the user can choose either single interface mode or dual interface mode. In single interface mode (section VIII.2), only port SSIA is operational. Where as in dual interface mode (section VIII.1), both SSIA and SSIB ports are operational.

These two ports carry data inside a synchronous frame consisting of four or eight sixteen bit time slots. SSIA port is synchronous to the Tx system clock and SSIB port is synchronous to Rx system clock. The format of the signal samples carried on these port is two's complement with MSB sent or received first.

As explained hereafter it is also possible to use the port A only to transfer the data between the ST7543 and the associated DSP.

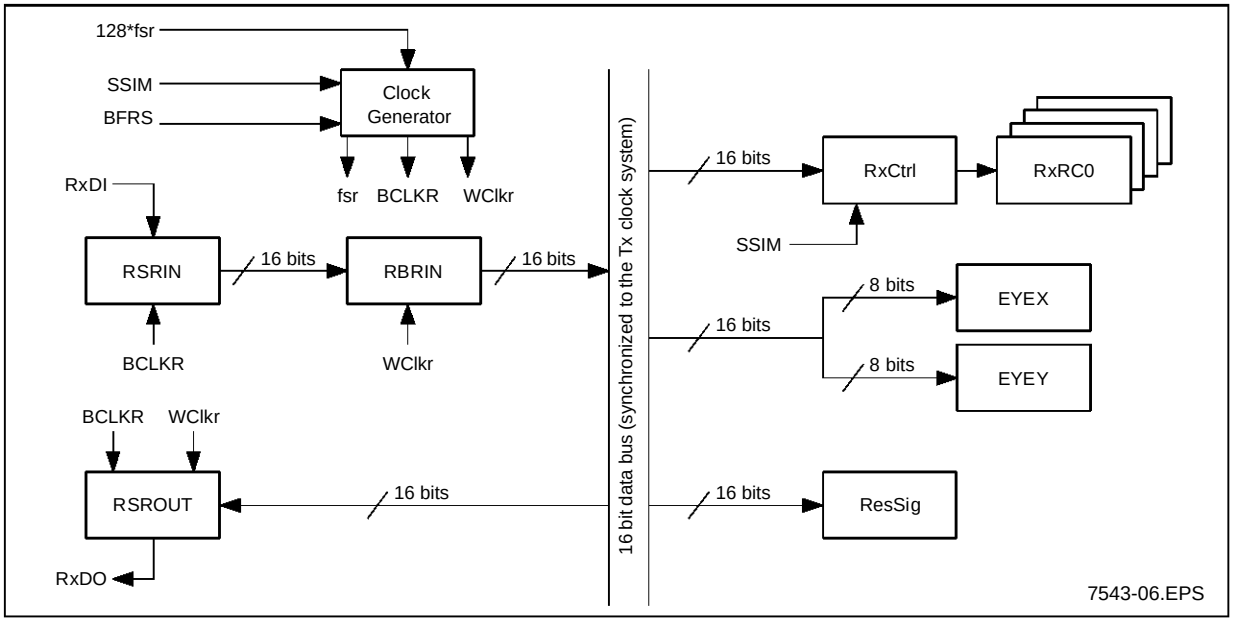
VII.6.1. Tx Clock Related Registers

Figure 3



VII.6.2. Rx Clock Related Registers

Figure 4

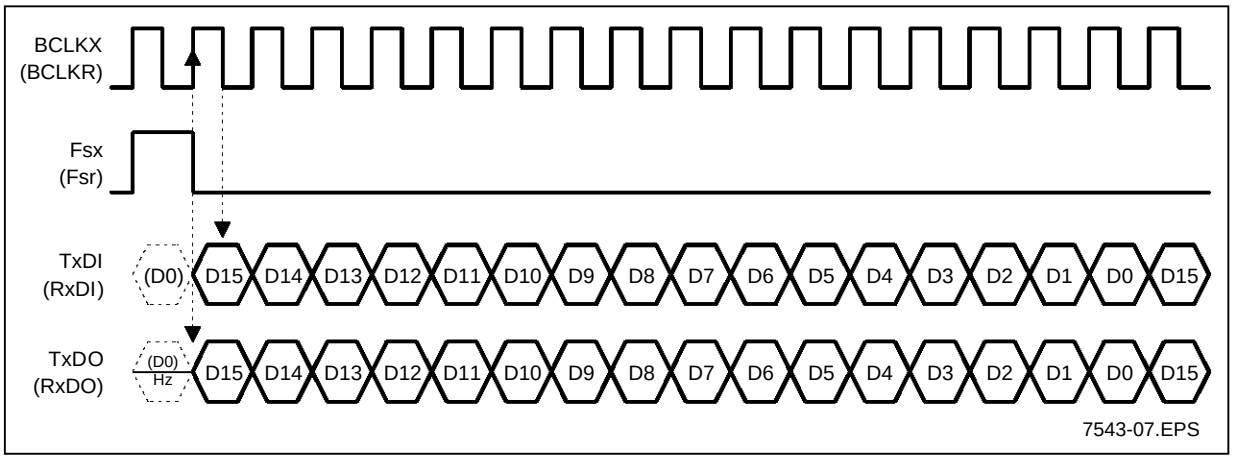


VIII. SERIAL INTERFACE OPERATION

Serial data transmission (reception) is initiated by a frame synchro signal Fsx (Fsr). The Data is clocked from TxDI (RxDI) into TSRIN (RSRIN) on the falling edge of BCLKX (BCLKR) and transfered to the TBRIN (RBRIN) register when a complete 16 bit word has been received. Data is assumed to be received MSB first.

Serial data transmission (reception) output is initiated by a frame synchro signal Fsx (Fsr). The 16 bit Data word is loaded into TSROUT (RSROUT) and serially clocked out of TSROUT (RSROUT) to TxDO (RxDO) on the rising edge of BCLKX (BCLKR).
BCLKX (BCLKR) frequency can be programmed to be either 64 or 128 times Fsx (Fsr) using the Bit Frame Rate Select (BFRS) input pin.

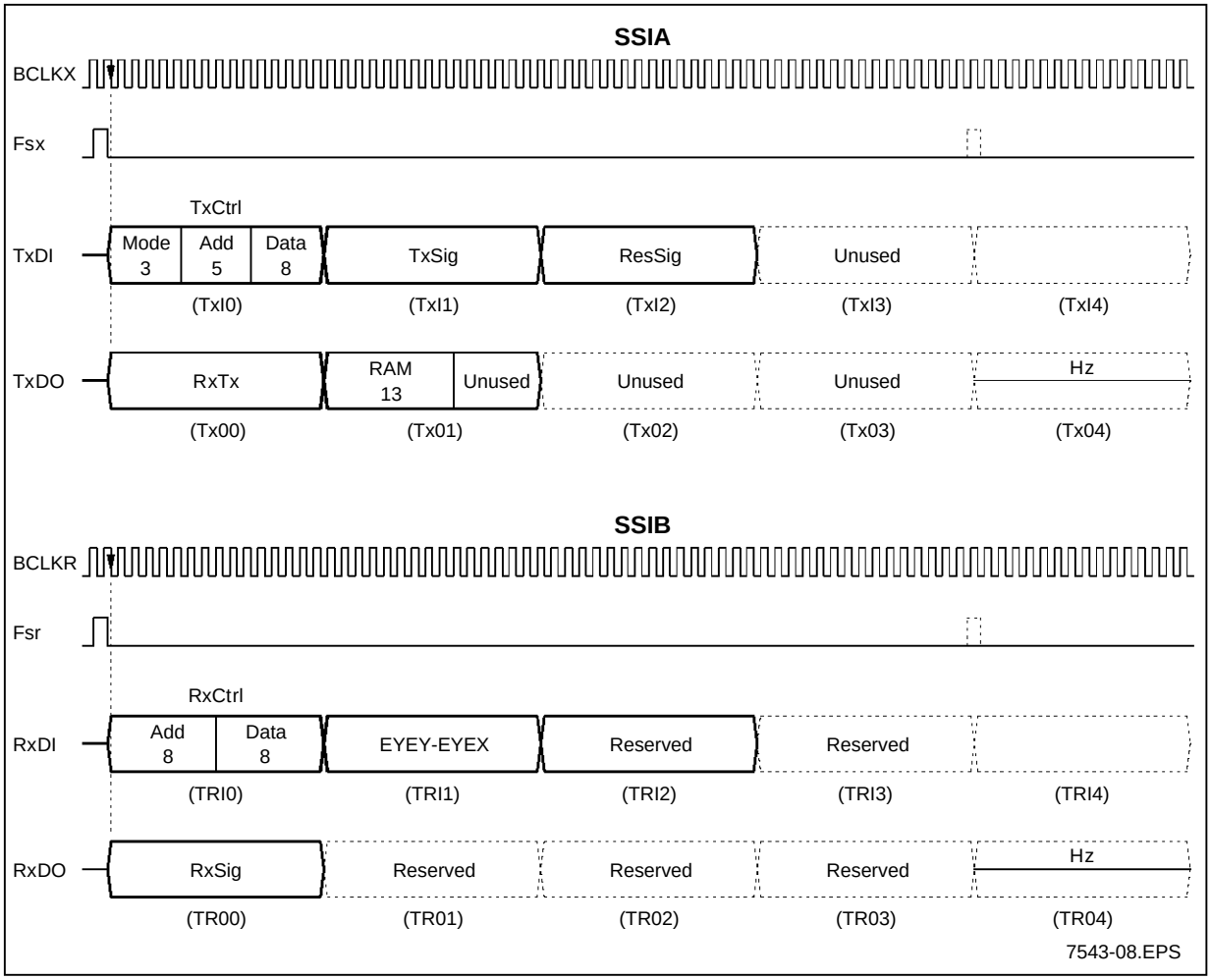
Figure 5 : Serial Channel Timing



VIII.1. DUAL SERIAL INTERFACE MODE (SSIA, SSIB)

When SSIM is tied to V_{DD}, both A and B ports are functional. The port A (SSIA) is dedicated to the Tx channel and the port B (SSIB) to the Rx channel. The timing diagram showing the data format is given in fig 5. and 5bis.
The time-slot TXO1 is dedicated to the RAM coefficient reading. The RAM coefficient is selected by the address bits RA0 to RA1 in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of the start bit Stb (bit D14in Table 3) in the TxCtrl word.

Figure 5 bis : Serial Channel Timing - Dual Port Mode



VIII.2. SINGLE SERIAL INTERFACE MODE

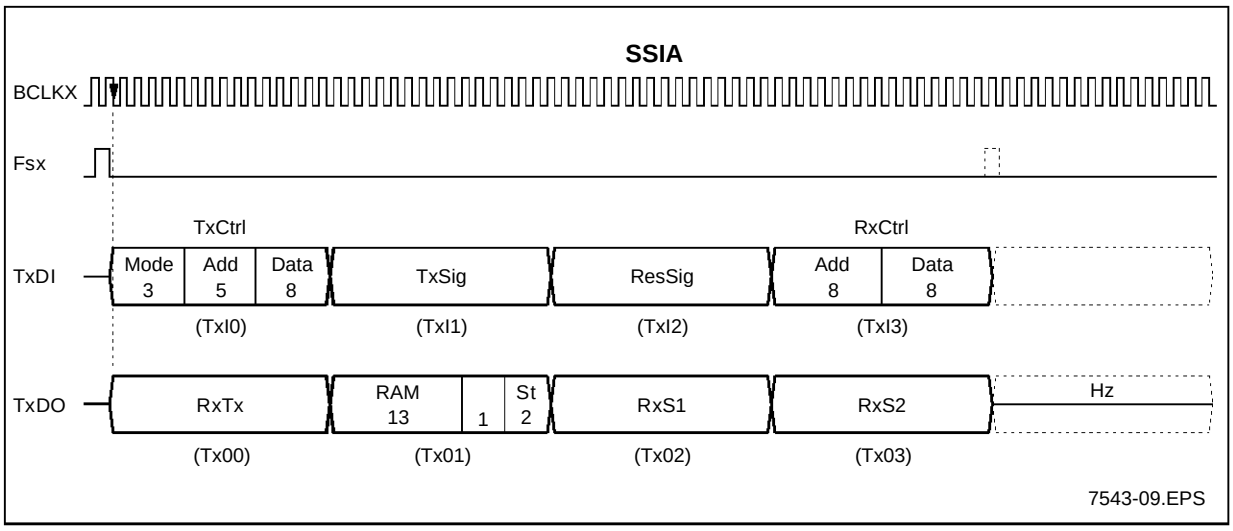
When SSIM is tied to GND, only port A (SSIA) is selected. In this case, port A carries both Tx and Rx signal samples and control words at the Tx sampling rate (Fsx). The RxDI input should be tied to V_{DD}. Since port B is not functional in this mode, the RxSig (synchronized to Fsr) will be available in the two time slots, RxS1 and RxS2, synchronized to Fsx. The reason for the two time slots is that the Fsr could be different in magnitude and phase from the Fsx. The status bits St0 and St1 are used to indicate which of the RxS1 and RxS2 are valid. Please see the table below. For example, if Fsx = 7200Hz and Fsr = 14400Hz both RxS1 and RxS2 could carry valid data. Figure 6 shows the timing diagram.

The time-slot TXO1 is dedicated to RAM coefficient reading. The RAM coefficient is selected by address bits (RA0 to RA1) in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of Start bit, Stb (bit D14 in Table 3) in the TxCtrl word.

Table 2.

STATUS WORD IN TxO1 TIME SLOT		
D1	D0	Valid Data
St1	St0	
0	0	None
0	1	None
1	0	RxS2
1	1	RxS1 and RxS2

Figure 6 : Serial Channel Timing - Single Port Mode

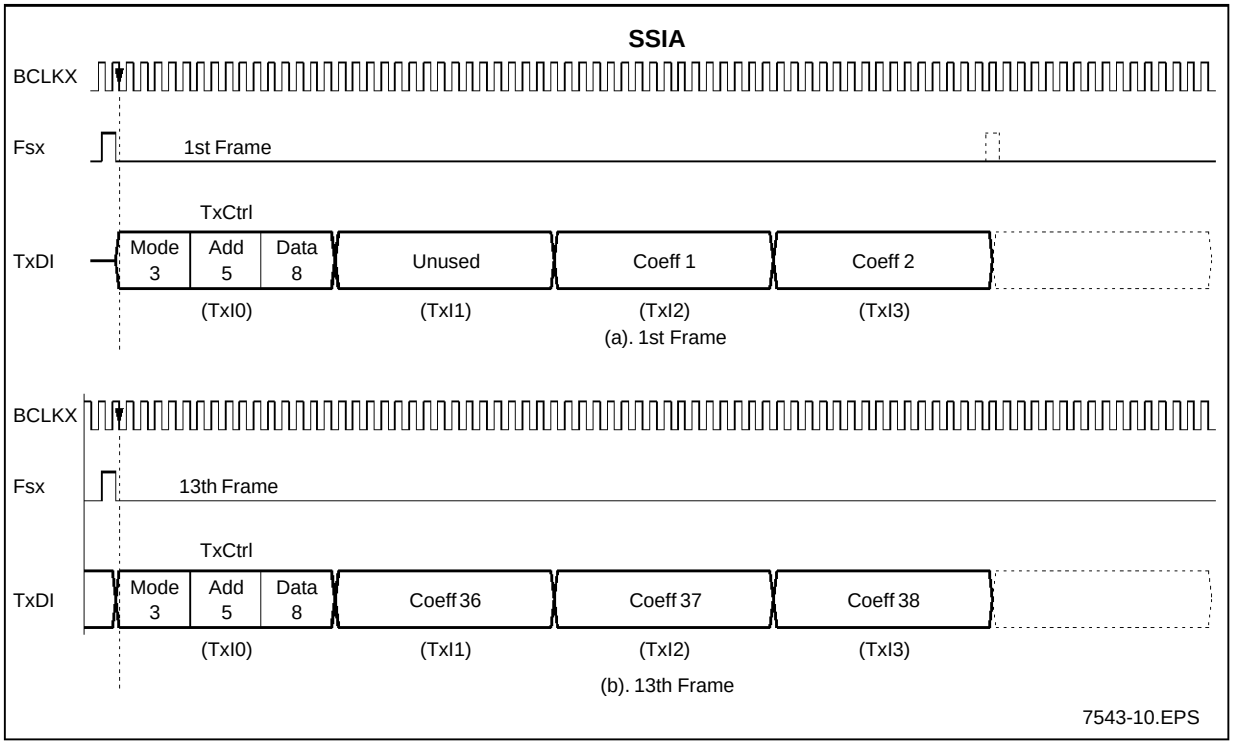


VIII.3. COEFFICIENT LOADING MODE

The Coefficient Loading Mode is selected by the Mode Select bit (MS) in the TxCtrl Word (Table 3). When the MS bit is a logic "1" the loading mode is selected. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). Each coefficient RAM stores 38 coefficients with 13 bits. Therefore the size of the coefficient RAM is 38 x 16 bits. The first frame transfers 2 coefficients and the 12 following frames each transfers 3 coefficients into the selected RAM, as shown in the following figure. The transfer is initiated by the rising edge of the Start bit coefficient Stb which is loaded into the TxCtrl word.

Note : Coefficient loading is the same for both dual and single serial interface modes.

Figure 7 : Coefficient Loading Mode



VIII.4. COEFFICIENT READING

Coefficient reading is selected in DATA mode only, i.e. when the Mode Select bit (MS) in the TxCtrl word is tied to logical 0. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). The 38 coefficients of 13 bits per coefficient are available, one per frame, in the timeslot TxO1 on the output Tx port A (see Fig.6). The reading is initiated by the rising edge of the Start bit Stb loaded into the TxCtrl word. The first coefficient is available at the output with one frame of delay on TxO1.

VIII.5. CRYSTAL SELECTION (XTAL10, XTAL11)

For applications needing different or higher symbol rates, the user can software select different master clock frequencies for the ST7543. Two XTAL inputs are provided for this purpose. The active XTAL input is selected in the TxCR1 register word with the Quartz Select bit (QS). It is mandatory to shortcircuit the XTAL10 and XTAL11 inputs when a single external crystal or clock generator is used.

VIII.6. FRAME FREQUENCY PROGRAMMING

When using the nominal master clock frequency, the frame frequency can be chosen between 7200Hz, 8000 and 9600Hz (see Tables 14 and 29). Whenever the frame frequency Fsx (Fsr) is modified, the data to the ST7543 during that frame should be high in the time-slots TxI1 (TrI1), TxI2 (TrI2) and TxI3 (TrI3). This is because the BCLKX (BCLKR) during that frame may not be correct. Therefore, whenever the Fsx (Fsr) is changed the user has to send information to the ST7543 after one frame delay.

VIII.7. INITIALIZATION AND LOW-POWER RESET MODE

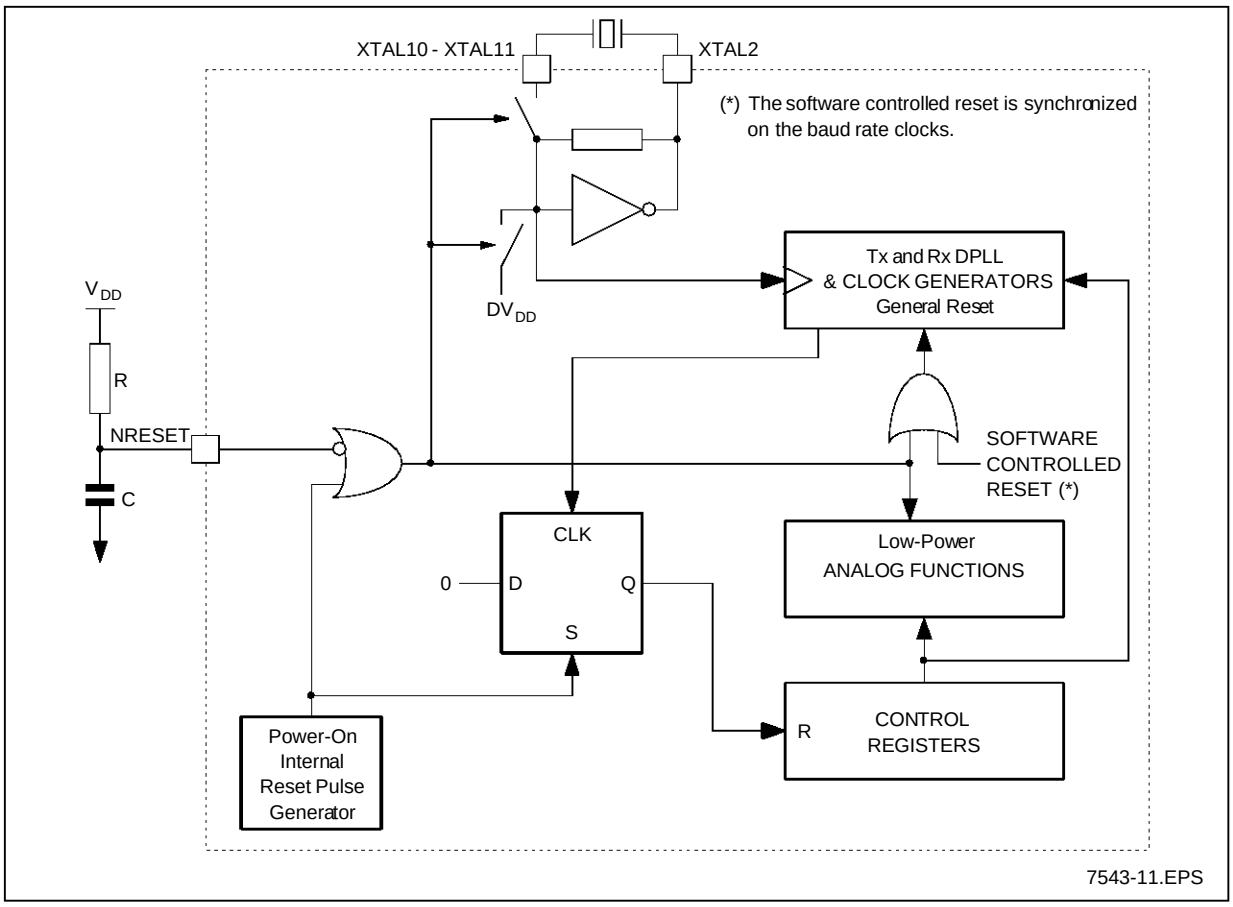
Internal power-on circuitry automatically resets the DPLL, the clock generator counters, and initializes the internal control registers. The initial status of these registers is given in the PROGRAMMABLE FUNCTIONS section.

During hardware reset (NRESET pin is tied to GND), the input to the inverter (across the crystal) will be high (DV_{DD}), the DPLL and the clock generator counters are initialized, all the analog circuitry is placed in low-power mode and the XTAL oscillator is stopped. The transmit attenuator is initialized in an infinite attenuation mode (see Table 22) in order to avoid the transmission of undesirable signals on the phone line.

Access to the circuit is disabled during reset until the clock oscillator starts. The duration of the reset time can be increased by connecting the NRESET input to an external RC timeconstant as indicated in fig 8.

In normal operation the NRESET input is used to control the LowPower mode. When NRESET is not used, it must be tied to V_{DD}. The ST7543 also allows software reset (see Table 21). For example, for Tx clock reset the bits D2 and D3 should be set.

Figure 8 : Power-on Initilization Circuitry



IX. CIRCUIT PROGRAMMING

This section defines the control and status words required to program the ST7543.
The circuit configuration is managed by the control words TxCtrl and RxCtrl and the SSIM, BFRS inputs.
The control words contain three fields :

- **Mode Field** 3 bits (D15-D13) mode control bit
- **Address Field** 5 bits (D12-D8) 2 bits for Coeff RAM address
  3 bits for Control Registers address
- **Data Field** 8 bits (D7-D0) Control Registers content

IX.1. MODE FIELD

Table 3

TxCtrl Word			
D15	D14	D13	Select mode
MS	Stb	QS	
0	-		Data Mode, Control Register Access Mode and Coefficient Reading Mode
1 (INI)	-		Coefficient Loading Mode and Filter Data Memory Reset (INI)
-	↑		Start bit for Coefficient Loading or Reading. The loading is initiated by a rising edge, i.e. a logical one programmed after a logical zero.
-	-	1	XTAL10 Selected (INI)
-	-	0	XTAL11 Selected

INI : initial value

IX.2. ADDRESS FIELD

IX.2.1. Ram Address Field
Table 4

TxCtrl Word								
D15	D14	D13	D12	D11	D10	D9	D8	RAM Address
MS	Stb	QS	RA0	RA1	AD2	AD1	AD0	
-	↑	-	0	0	-	-	-	RAM 1 (INI)
-	↑	-	0	1	-	-	-	RAM 2
-	↑	-	1	0	-	-	-	RAM 3
-	-	-	1	1	-	-	-	Not any RAM accessed

INI : initial value

IX.2.2. Transmit Control Register Address Field
Table 5

Register Name	TxCtrl Word							
	D15	D14	D13	D12	D11	D10	D9	D8
	MS	Stb	QS	RA0	RA1	AD2	AD1	AD0
TxCR0	-	-	-	-	-	0	0	0
TxCR1	-	-	-	-	-	0	0	1
TxCR2	-	-	-	-	-	0	1	0
TxCR3	-	-	-	-	-	0	1	1
None	-					1	1	1

IX.2.3. Receive Control Register Address Field
Table 6

Register Name	RxCtrl Word							
Note 1	D15	D14	D13	D12	D11	D10	D9	D8
-	-	-	-	-	-	AD2	AD1	AD0
RxCR0	-	-	-	-	-	0	0	0
RxCR1	-	-	-	-	-	0	0	1
RxCR2	-	-	-	-	-	0	1	0
RxCR3	-	-	-	-	-	0	1	1
None	-	-	-	-	-	1	1	1

Note 1 : In single interface mode, the RxCtrl registers cannot be programmed during the coefficient loading mode (see Fig.6 and 7).

IX.3. CONTROL REGISTER DATA FIELD

IX.3.1. Transmit Control Register Programming
Table 7

REGISTER	DATA								PROGRAMMED FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
TxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Tx Bit rate clock generator
TxCR1	M0	Q1	Q0	U2	U1	U0	P0	BS	Tx Sampling, Baud and HS clock generators; Band Split configuration.
TxCR2	AT1	AT0	LTX	LC	SST	SYT	Ts4	Ts3	Tx Attenuator; TxClock Synchronization and Reset
TxCR3	V2	V1	V0	W	Ts2	Ts1	Ts0	DL	Tx Phase Comp and Lead or Lag Clock generator; Test configuration

IX.3.2. Receive Control Register Programming

Table 8

REGISTER	DATA								PROGRAMMED FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
RxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Rx Bit rate clock generator
RxCR1	M0	Q1	Q0	U2	U1	U0	P0	ECK	Rx Sampling, Baud and HS clock generators; Baud and HS clock Enable
RxCR2	LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	Rx Fine and Coarse Phase Shift Control
RxCR3	-	-	-	-	Ts2	SYR	Ts1	Ts0	Rx Clock generator Reset; Test configuration

IX.3.3. Control Bit Function Summary

IX.3.3.1. TxCTRL WORD

Table 9

Table	Bit	PROGRAMMED FUNCTION
11,12,13	N0	N Divisor rank : 3, 4.
"	R1,R0	R Divisor rank : 8/7, 6/5, 4/3, 1.
"	S1,S0	S Divisor rank : 1, 3, 5, 7.
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512.
14,15,16	M0	M Divisor rank : 3, 4.
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8.
17	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 , 8, 12, 16.
18	P0	P Divisor rank : 3, 4.
19	BS	Band Splitting or Echo cancelling mode. In this mode, the IIR2 filter output is internally connected to the IIR3 filter input. The RxTx signal will still be available at the port A.
20	LTX	Synchronization signal : TxSCLK or RxCLK.
20	LC	Synchronization enabling : Lock or Free DPLL.
20	SST	TxDPLL reset on the next falling edge of the synchronization signal. SST is automatically reset after its action is completed.
21	SYT	Tx Clock generator reset. This reset is synchronized to the next baud rate clock falling edge . SYT bit is reset after action completion.
22	AT1,AT0	Tx Attenuation: 0dB, 6dB or infinite.
23	V2,V1,V0	V Divisor rank : 1, 2, 4
24	W	f_{SHIFT} frequency : Fsx or Fsx / 2 (Related to frequency capture range of the TxDPLL as $f_Q - f_{SHIFT} < f_{AVERAGE} < f_Q + f_{SHIFT}$
25	Ts0,Ts1,Ts2	Test Functions. Must be set to logical 0 for normal operation
25	DL	Normal Mode or Digital Loop Mode

IX.3.3.2. RxCTRL WORD

Table 10

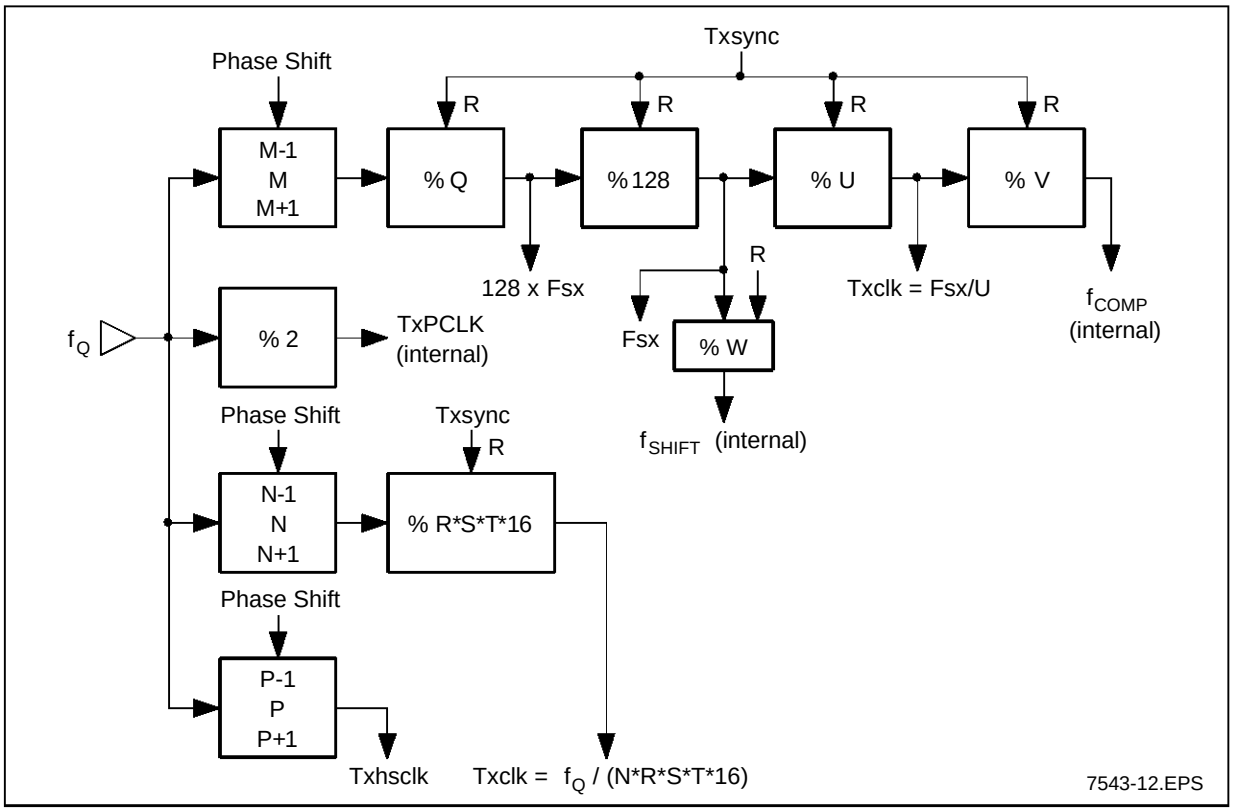
Table	Bit	PROGRAMMED FUNCTION
26,27,28	N0	N Divisor rank : 3, 4.
"	R1,R0	R Divisor rank : 8/7, 6/5, 4/3, 1.
"	S1,S0	S Divisor rank : 1, 3, 5, 7.
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512.
29,30,31	M0	M Divisor rank : 3, 4.
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8.
32	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 , 8, 12, 16.
33	P0	P Divisor rank : 3, 4.
33	ECK	Tx/RxRCLK and Tx/RxHSCLK output enabling.
34	LL	Rx DPLL Lead/Lag control.
34	PS1,PS0 PS2	Rx DPLL Phase Shift magnitude : 0, 8, 12, 16, 20, 24, 28, or 32 master clock periods. These bits are reset after phase shift completion.
34	PS3	Rx DPLL Phase Shift magnitude : One 128*Fsx period. This bit is reset after phase shift completion.
35	AP2,AP1 AP0	Rx DPLL Coarse Phase Lag : 0, 64, 128, 256 512, 1024, 2048, or 4096 master clock period. These bits are reset after phase lag completion.
36	SYR	Rx Clock generator reset. This reset is synchronized to the next RxRCLK clock falling edge. SYR bit is reset after action is completed.
36	Ts0,Ts1,Ts2	Test Functions. Must be set to logical 0 for normal operation.

X. PROGRAMMABLE FUNCTIONS

X.1. TRANSMIT SECTION

The different transmit clocks are obtained by frequency division process in several counters (see Fig.9).

Figure 9 : Transmit Clock Generator



Note 1 : TxPCLK is an internal Processing Clock used by the three IIR filters

Note 2 : The phase of internal clock f_{COMP} will be compared to the synchronization signal (Table 20) in order to control TxDPLL (see Tables 20, 23 and 24). V divisor must be chosen such that the f_{COMP} frequency is an integral sub-multiple of the synchronization frequency. The most typical frequency for f_{COMP} is the baud rate frequency.

Note 3 : During each period of f_{COMP} the average input frequency of the transmit clock generator can be :
f_Q , $f_Q + f_{SHIFT}$ or $f_Q - f_{SHIFT}$ with f_{SHIFT} = Fsx or Fsx/2

Note 4 : The bit rate frequency should always be an integer multiple of the baud rate frequency for the transmit DPLL to lock on to the synchronization signal.

X.1.1. Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency f_Q=18.432MHz
Table 11

TxCRO Register									Bit Rate Clock Frequency(Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank	(f_Q = 18.432MHz) Txclk=f_Q/(N*R*S*T*16)
N0	R1	R0	S1	S0	T2	T1	T0		
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960*8/7	16800
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600

INI : initial value

X.1.2. Transmit Bit Rate Clock Frequency Programming with Master Clock FrequencY f_Q=29.4912MHz.
Table 12.

TxCRO Register									Bit Rate Clock Frequency(Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank	(f_Q = 29.4912MHz) Txclk=f_Q/(N*R*S*T*16)
N0	R1	R0	S1	S0	T2	T1	T0		
1	1	1	0	0	0	1	0	1024	28800
0	1	1	0	1	0	0	1	1152	25600
1	0	1	0	0	0	1	0	1024*6/5	24000
0	0	0	0	1	0	0	1	1152*8/7	22400
1	1	0	0	0	0	1	0	1024*4/3	21600
1	1	1	0	1	0	0	1	1536	19200
1	0	0	0	1	0	0	1	1536*8/7	16800
1	0	1	0	1	0	0	1	1536*6/5	16000
1	1	1	0	0	0	1	1	2048	14400
0	1	1	0	1	0	1	0	2304	12800
1	0	1	0	0	0	1	1	2048*6/5	12000
1	1	1	0	1	0	1	0	3072	9600
1	1	1	0	0	1	0	0	4096	7200
1	1	1	0	1	0	1	1	6144	4800
1	1	1	0	1	1	0	0	12288	2400
1	1	1	0	1	1	0	1	24576	1200
1	1	1	0	1	1	1	0	49152	600

X.1.3. Transmit Bit Clock Frequency Programming. Divisor Rank
Table 13

TxCR0 Register								Bit rate clock Frequency(Hz) Txclk=f_Q/(N*R*S*T*16)			
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
0	-	-	-	-	-	-	-	3(INI)			
1	-	-	-	-	-	-	-	4			
-	0	0	-	-	-	-	-		8/7		
-	0	1	-	-	-	-	-		6/5		
-	1	0	-	-	-	-	-		4/3		
-	1	1	-	-	-	-	-		1(INI)		
-	-	-	0	0	-	-	-			1	
-	-	-	0	1	-	-	-			3	
-	-	-	1	0	-	-	-			5(INI)	
	-	-	1	1	-	-	-			7	
	-	-	-	-	0	0	0				4
-	-	-	-	-	0	0	1				8(INI)
-	-	-	-	-	0	1	0				16
-	-	-	-	-	0	1	1				32
-	-	-	-	-	1	0	0				64
-	-	-	-	-	1	0	1				128
-	-	-	-	-	1	1	0				256
-	-	-	-	-	1	1	1				512

INI : initial value

X.1.4. Transmit Sampling Clock Frequency Programming with Master Clock Frequency f_Q=18.432MHz
Table 14

TxCR1 Register								Sampling Clock Frequency fsx (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Quartz frequency f_Q = 18.432MHz Fsx=f_Q/(M*Q*128)
M0	Q1	Q0	U2	U1	U0	P0	BS	
0	0	0	-	-	-	-	-	9600
0	0	1	-	-	-	-		8000
1	0	0	-	-	-	-	-	7200 (INI)

INI : initial value

X.1.5. Transmit Sampling Clock Frequency Programming with Master Clock Frequency f_Q=29.4912MHz.
Table 15

TxCR1 Register								Sampling Clock Frequency fsx (Hz)	
D7	D6	D5	D4	D3	D2	D1	D0	Quartz frequency f_Q = 29.4912MHz Fsx=f_Q/(M*Q*128)	
M0	Q1	Q0	U2	U1	U0	P0	BS		
0	0	1	-	-	-	-	-	12800	(4*3200)
0	1	0	-	-	-	-		10971	(4*2743)
0	1	1	-	-	-	-	-	9600	(4*2400) (3*3200)
1	1	0	-	-	-	-		8229	(3*2743)
1	1	1	-	-	-	-	-	7200	(3*2400)

X.1.6. Transmit Sampling Clock Frequency Programming. Divisor Rank
Table 16

TxCR1 Register								Sampling Clock frequency $Fsx = f_Q/(M*Q*128)$	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	BS	M	Q
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI)
-	0	1	-	-	-	-	-		6
-	1	0	-	-	-	-	-		7
-	1	1	-	-	-	-	-		8

INI : initial value

X.1.7. Transmit Baud Rate Frequency Programming. Divisor Rank.
Table 17

TxCR1 Register								Baud rate frequency Txrclk = Fsx / U
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	U
-	-	-	0	0	0	-	-	3 (INI)
-	-	-	0	0	1	-		4
-	-	-	0	1	0	-	-	5
-	-	-	0	1	1	-	-	6
-	-	-	1	0	0	-	-	8
-	-	-	1	0	1	-	-	12
-	-	-	1	1	0	-	-	16
-	-	-	1	1	1	-	-	16

INI : initial value

X.1.8. Transmit Highest Synchronous Bit Frequency Programming. Divisor Rank
Table 18

TxCR1 Register								Transmit Highest Synchronous Frequency $Txhsclk=f_Q/P$
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	P
-	-	-	-	-	-	0	-	3 (INI)
-	-	-	-	-	-	1		4

INI : initial value

X.1.9. Band Split Mode
Table 19

TxCR1 Register								Band Split Mode
D7	D6	D5	D4	D3	D2	D1	D0	
M0	Q1	Q0	U2	U1	U0	P0	BS	
-	-	-	-	-	-	-	0	Inactive (INI)
-	-	-	-	-	-	-	1	Active : Rx Filter Output connected to reconstruction filter input (see Table 9)

INI : initial value

X.1.10. Transmit Synchronization Signal Programming
Table 20

TxCR2 Register								Tx DPLL Clock
D7	D6	D5	D4	D3	D2	D1	D0	Synchronization
AT1	AT0	LTX	LC	SST	SYT	Ts4	Ts3	
-	-	0	1	-	-	-	-	TxSCLK
-	-	1	1	-	-	-	-	RxCLK
-	-	-	1	1	-	-	-	Reset on Next falling edge of Synchronization Signal (Note 1)
-	-	-	0	-	-	-	-	No Synchronization (INI)

INI : initial value
Note 1: The SST bit is automaticaly reset after its action is completed
Note 2 : If D4 = 1, the Tx DPLL will be locked to the synchronization signal. Otherwise, the Tx DPLL will be free-running.

X.1.11. Clock Reset Programming
Table 21

TxCR2								RegisterReset Mode
D7	D6	D5	D4	D3	D2	D1	D0	
AT1	AT0	LTX	LC	SST	SYT	Ts4	Ts3	
-	-	-	-	-	0	0	0	Normal Mode (INI)
-	-	-	-	-	1	-	-	Tx Clock Reset (Note 1) on next falling edge of TxRCLK
-	-	-	-	-	-	1	-	Test purpose
-	-	-	-	-	-	-	1	Test purpose

INI : initial value
Note 1: The SYT bit is automaticaly reset after its action is completed

X.1.12. Transmit Attenuator Programming
Table 22

TxCR2 Register								Transmit Attenuator
D7	D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
AT1	AT0	LTX	LC	SST	SYT	Ts4	Ts3	
0	0	-	-	-	-	-	-	Infinite (INI)
1	0	-	-	-	-	-	-	-6
1	1	-	-	-	-	-	-	0

INI : initial value

X.1.13. Phase Comparator Frequency (f_{COMP})
Table 23

TxCR3 Register								Tx Phase Comparator Frequency f_{COMP} = Txrclk / V
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank
V2	V1	V0	W	Ts2	Ts1	Ts0	DL	V
0	0	0	-	-	-	-	-	1
0	0	1	-	-	-	-	-	2
1	0	0	-	-	-	-	-	4 (INI)

INI : initial value

X.1.14. Phase Shift Frequency (f_{SHIFT})

Table 24

TxCR3 Register								Phase Shift Frequency (*) f_{SHIFT} = Fsx / W
D7	D6	D5	D4	D3	D2	D1	D0	(Average updated master clock frequency)
V2	V1	V0	W	Ts2	Ts1	Ts0	DL	W
			0					Fsx/2 (INI) (f_Q +/- Fsx/2)
			1					Fsx (f_Q +/- Fsx)

INI : initial value
(*) The W bit selects the phase shift frequency of the TxDPLL, and hence the capture range (see Fig. 9)

X.1.15. Test Modes

Table 25

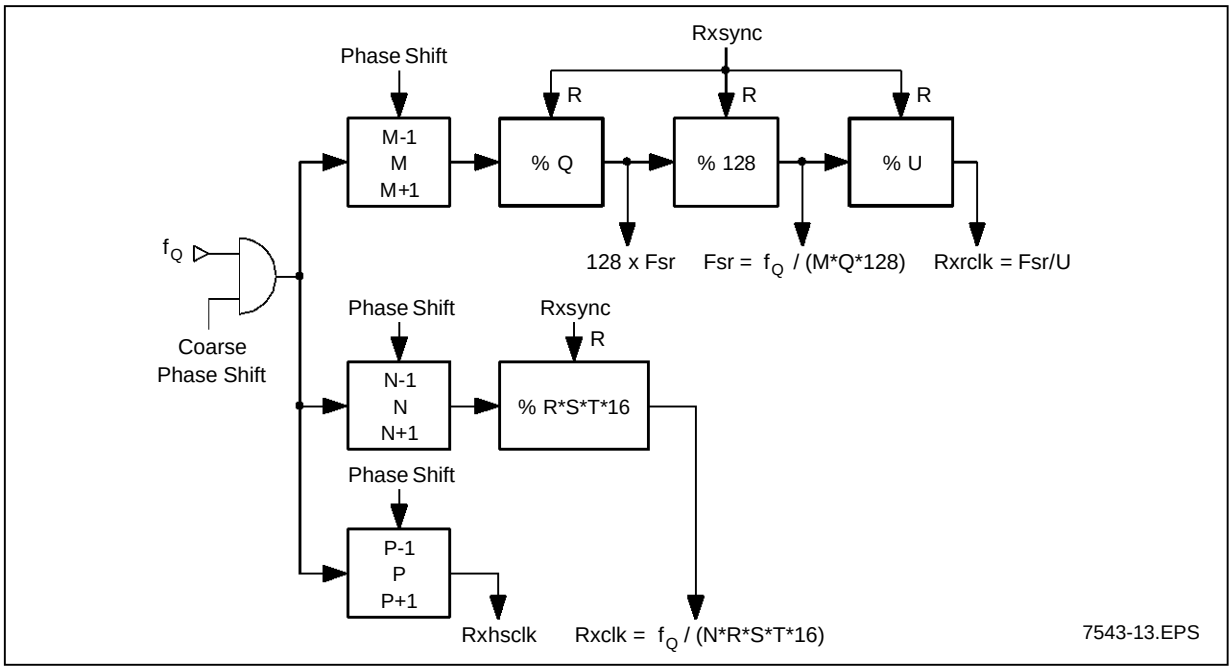
TxCR3 Register								Test Modes
D7	D6	D5	D4	D3	D2	D1	D0	
V2	V1	V0	W	Ts2	Ts1	Ts0	DL	
				0	0	0	0	Normal Mode (INI)
-	-	-	-	-	-	-	1	Digital Loop Test (1)
-	-	-	-	-	-	1	-	Test 0
-	-	-	-	-	1	-	-	Test 1
-	-	-	-	1	-	-	-	Test 2

INI : initial value
Note 1: When the digital loop test is performed, with the Rx sample clock equal to the Tx sample clock and the single serial interface mode the output of the interpollator RxSig is sent internally to the TxSig register, and if the band split mode is selected (TxCR1) and the output pins TxDO is connected to the RxD1 pin the input analog signal on A/DC is output on the D/AC. It's the easiest test to verify the right programming of the chip.

X.2. RECEIVE SECTION

The different Receive clocks are obtained by frequency division in several counters (see Fig.10)

Figure 10 : Receive Clock Generator



X.2.1. Receive Bit Rate Clock Frequency Programming with Master Clock Frequency f_Q=18.432MHz Table 26

RxCRO Register									Bit rate clock frequency(Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(f_Q = 18.432MHz) Rxclk=f_Q/(N*R*S*T*16)
N0	R1	R0	S1	S0	T2	T1	T0		
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960*8/7	16800
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600

INI : initial value

X.2.2. Receive Bit Rate Clock Frequency Programming with Master Clock Frequency f_Q=29.4912MHz Table 27

RxCRO Register									Bit rate clock frequency(Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(f_Q = 29.4912MHz) Rxclk=f_Q/(N*R*S*T*16)
N0	R1	R0	S1	S0	T2	T1	T0		
1	1	1	0	0	0	1	0	1024	28800
0	1	1	0	1	0	0	1	1152	25600
1	0	1	0	0	0	1	0	1024*6/5	24000
0	0	0	0	1	0	0	1	1152*8/7	22400
1	1	0	0	0	0	1	0	1024*4/3	21600
1	1	1	0	1	0	0	1	1536	19200
1	0	0	0	1	0	0	1	1536*8/7	16800
1	0	1	0	1	0	0	1	1536*6/5	16000
1	1	1	0	0	0	1	1	2048	14400
0	1	1	0	1	0	1	0	2304	12800
1	0	1	0	0	0	1	1	2048*6/5	12000
1	1	1	0	1	0	1	0	3072	9600
1	1	1	0	0	1	0	0	4096	7200
1	1	1	0	1	0	1	1	6144	4800
1	1	1	0	1	1	0	0	12288	2400
1	1	1	0	1	1	0	1	24576	1200
1	1	1	0	1	1	1	0	49152	600

INI : initial value

X.2.3. Receive Bit Rate Clock Frequency Programming. Divisor Rank
Table 28

RxCR0 Register								Bit rate clock frequency Rxclk=f_Q/(N*R*S*T*16)			
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
0	-	-	-	-	-	-	-	3 (INI)			
1	-	-	-	-	-	-	-	4			
-	0	0	-	-	-	-	-		8/7		
-	0	1	-	-	-	-	-		6/5		
-	1	0	-	-	-	-	-		4/3		
-	1	1	-	-	-	-	-		1(INI)		
-	-	-	0	0	-	-	-			1	
-	-	-	0	1	-	-	-			3	
-	-	-	1	0	-	-	-			5(INI)	
-	-	-	1	1	-	-	-			7	
-	-	-	-	-	0	0	0				4
-	-	-	-	-	0	0	1				8(INI)
-	-	-	-	-	0	1	0				16
-	-	-	-	-	0	1	1				32
-	-	-	-	-	1	0	0				64
-	-	-	-	-	1	0	1				128
-	-	-	-	-	1	1	0				256
-	-	-	-	-	1	1	1				512

INI : initial value

X.2.4. Receive Sampling Clock Frequency Programming with Master Clock Frequency f_Q=18.432MHz
Table 29

RxCR1 Register								Sampling Clock frequency Fsr (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Quartz frequency f_Q = 18.432MHz Fsr=f_Q/(M*Q*128)
M0	Q1	Q0	U2	U1	U0	P0	ECK	
0	0	0	-	-	-	-	-	9600
0	0	1	-	-	-	-		8000
1	0	0	-	-	-	-	-	7200 (INI)

INI : initial value

X.2.5. Receive Sampling Clock Frequency Programming with Master Clock Frequency f_Q=29.4912MHz
Table 30

RxCR1 Register								Sampling Clock frequency Fsr (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Quartz frequency f_Q = 29.4912MHz Fsr=f_Q/(M*Q*128)
M0	Q1	Q0	U2	U1	U0	P0	ECK	
0	0	1	-	-	-	-	-	12800 (4 x 3200)
0	1	0	-	-	-	-	-	10971 (4 x 2743)
0	1	1	-	-	-	-	-	9600 (4 x 2400) (3 x 3200)
1	1	0	-	-	-	-	-	8229 (3 x 2743)
1	1	1	-	-	-	-	-	7200 (3 x 2400)

X.2.6. Receive Sampling Clock Frequency Programming. Divisor Rank.
Table 31

RxCR1 Register								Sampling Clock frequency $Fsr=f_Q/(M*Q*128)$	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	ECK	M	Q
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI)
-	0	1	-	-	-	-	-		6
-	1	0	-	-	-	-	-		7
-	1	1	-	-	-	-	-		8

INI : initial value

X.2.7. Receive Baud Rate Frequency Programming. Divisor Rank.
Table 32

RxCR1 Register								Baud rate frequency(Hz) Rxrclk
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	ECK (*)	U
-	-	-	0	0	0	-	1	3 (INI)
-	-	-	0	0	1	-	1	4
-	-	-	0	1	0	-	1	5
-	-	-	0	1	1	-	1	6
-	-	-	1	0	0	-	1	8
-	-	-	1	0	1	-	1	12
-	-	-	1	1	0	-	1	16
-	-	-	1	1	1	-	1	16

INI : initial value

X.2.8. Receive Highest Synchronous Bit Frequency Programming. Divisor Rank.
Table 33

RxCR1 Register								Receive Highest Synchronous Frequency $Rxhsclk=f_Q/P$
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	ECK (*)	P
-	-	-	-	-	-	0	1	3 (INI)
-	-	-	-	-	-	1	1	4

INI : initial value
(*) ECK bit is used to enable the RxRCLK and RxHSCLK outputs (as well as TxRCLK and TxHSCLK clock outputs) when set at logical 1. The baud rate clock must be programmed to its correct value even though the corresponding output pin is disabled (ECK = 0).

X.2.9. Receive Fine Phase Shift Programming
Table 34

RxCR2 Register								Receive Phase Shift Programming
D7	D6	D5	D4	D3	D2	D1	D0	Action on RxDPLL Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No phase shift (INI)
0	0	0	0	1	0	0	0	8
0	0	0	1	0	0	0	0	12
0	0	0	1	1	0	0	0	16
0	0	1	0	0	0	0	0	20
0	0	1	0	1	0	0	0	24
0	0	1	1	0	0	0	0	28
0	0	1	1	1	0	0	0	32
0	1	0	0	0	0	0	0	One 128*fsx oversampling period
1	-	-	-	-	-	-	-	As above but lead instead of lag (i.e. addition of Master-Clock pulses)

INI : initial value

X.2.10. Receive Coarse Phase Shift Programming
Table 35

RxCR2 Register								Receive Phase Shift Amplitude Programming
D7	D6	D5	D4	D3	D2	D1	D0	Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No Phase Shift (INI)
0	0	0	0	0	0	0	1	64
0	0	0	0	0	0	1	0	128
0	0	0	0	0	0	1	1	256
0	0	0	0	0	1	0	0	512
0	0	0	0	0	1	0	1	1024
0	0	0	0	0	1	1	0	2048
0	0	0	0	0	1	1	1	4096

INI : initial value

X.2.11. RxCLOCK Reset Programming
Table 36

RxCR3 Register								Reset Mode
D7	D6	D5	D4	D3	D2	D1	D0	
				Ts2	SYR	Ts1	Ts0	
0	0	0	0	0	0	0	0	Normal Mode (INI)
0	0	0	0	0	1	0	0	Rx Clock Reset on next falling edge of the RxRclk clock (1).

INI : initial value
Note 1: SYR bit is automaticaly reset after its action is completed

XI. ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V_{DD} = +5V , T_{amb}=25°C and for nominal crystal frequency f_Q=18.432MHz, Fsx = 7.2kHz.

XI.1. ABSOLUTE MAXIMUM RATINGS (referenced to GND)

Table 37

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_I,V_{IN}	Digital or Analog Input Voltage	-0.3 to V_{DD} +0.3	V
I_I,I_{IN}	Digital or Analog Input Current	±1	mA
I_O	Digital Output Current	±20	mA
I_{OUT}	Analog Output Current	±10	mA
T_{oper}	Operating Temperature Range	0, +70	°C
T_{stg}	Storage Temperature Range (Plastic)	-40, +125	°C
P_D	Maximum Power Dissipation	500	mW

XI.2. DC CHARACTERISTICS

V_{DD} = 5.0 V ± 5%, GND = 0 V, T_A = 0 to +70°C (unless otherwise specified)

XI.2.1. Power Supply And Common Mode Voltage

Table 38

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	4.75	5	5.25	V
I_{DD}	Supply current		32	37	mA
I_{DDlp}	Supply current in low power mode		0.6	2	mA
V_{CM}	Input common mode voltage	V_{DD}/2 (-5%)	V_{DD}/2	V_{DD}/2 (+5%)	V

XI.2.2. Digital Interface

All digital pins except XTAL pins.

Table 39

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	-0.3		0.8	V
V_{IH}	High level input voltage	2.2			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	+/-1	+10	µA
V_{OH}	High level output voltage (I_{load} = -2mA)	2.4			V
V_{OL}	Low level output voltage (I_{load} = 2 mA)			0.4	V
C_{IN}	Input capacitance		5		pF

XI.2.3. Crystal Oscillator Interface (XTAL10,XTAL11)

Table 40

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage			1.5	V
V_{IH}	High level input voltage	3.5			V
I_L	Low level input current GND ≤ V_I ≤ V_{ILmax}		-15		µA
I_H	High level Input Current V_{IHmin} ≤ V_I ≤ V_{DD}		15		µA

XI.2.4. Analog Interface
Table 41

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Differential reference voltage output = V_{REFP}-V_{REFN}	2.40	2.50	2.60	V
Tempco (V_{REF})	V_{REF} temperature coefficient		200		ppm/C
V_{CMOin}	Input common mode offset voltage $= \frac{RxA1 + RxA2}{2} - V_{CM}$	-300		300	mV
V_{DIFin}	Differential input voltage : RxA1-RxA2 ≤ 2*V_{REF}		2 V_{REF}		Vpp
V_{OFFin}	Differential input DC offset voltage. RxA1 = RxA2 = V_{CM} (note 1)	-100		100	mV
V_{CMOout}	Output common mode voltage offset $= \frac{TxA1 + TxA2}{2} - V_{CM}$	200		200	mV
V_{DIFout}	Differential output voltage : TxA1-TxA2 = 2*V_{REF}		2 V_{REF}		Vpp
V_{OFFout}	Differential output DC offset voltage : (TxA1-TxA2)DC	-100		100	mV
V_{OUT}	Output voltage EYEX,EYEY	GND		V_{DD}	V
R_{IN}	Input resistance RxA1, RxA2	100			kΩ
R_{OUT}	Output resistance TxA1,TxA2 EYEX, EYEY			 10 50	 Ω kΩ
R_L	Load resistance TxA1,TxA2 EYEX, EYEY	 10 1			 kΩ MΩ
C_L	Load capacitance TxA1,TxA2 EYEX, EYEY			 50 30	 pF pF

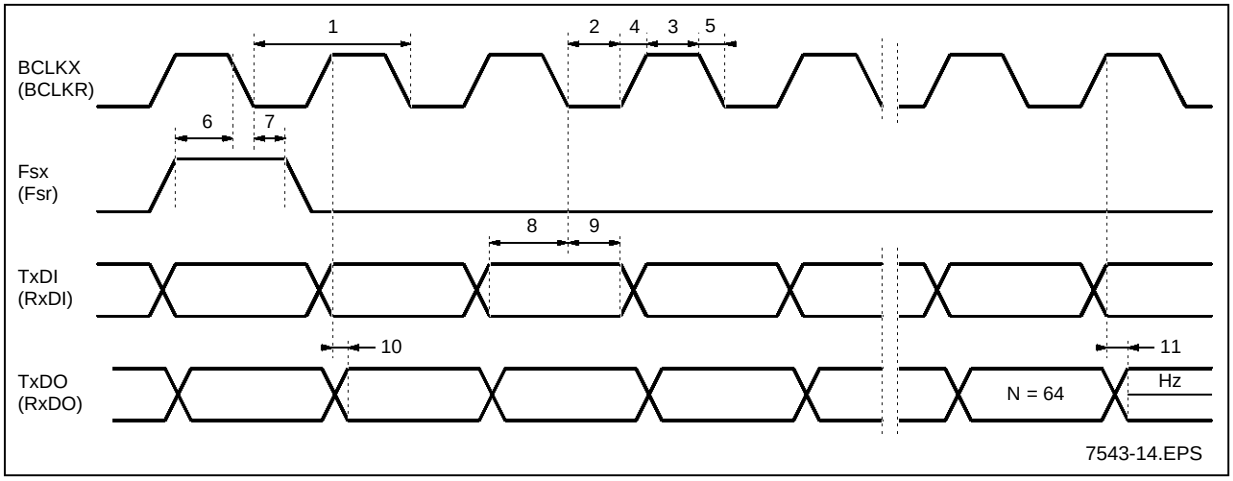
Note 1 : Input DC offset can be cancelled by high-pass filtering in IIR2 filter.

XI.3. AC ELECTRICAL SPECIFICATIONS
(V_{DD} = 5.0 V ± 5%, T_A = 0 to +70°C) - Output Load = 50 pF
Reference levels : V_{IL} = 0.8 V, V_{IH} = 2.2 V, V_{OL} = 0.4 V, V_{OH} = 2.4 V

XI.3.1. Serial Channel Timing (see Fig.11)
Table 42

Number	Parameter	Min.	Max.	Unit
1	BCLKX, BCLKR Period	450		ns
2	BCLKX, BCLKR Width Low	195		ns
3	BCLKX, BCLKR Width High	195		ns
4	BCLKX, BCLKR Rise Time		30	ns
5	BCLKX, BCLKR Fall Time		30	ns
6	FSX, FSR to BCLKX, BCLKR Setup	100		ns
7	FSX, FSR to BCLKX, BCLKR Hold	100		ns
8	TxDI, RxDI to BCLKX, BCLKR Setup	20		ns
9	TxDI, RxDI to BCLKX, BCLKR Hold	0		ns
10	BCLKX, BCLKR High to TxDO, RxDO Valid		50	ns
11	BCLKX, BCLKR to TxDO, RxDO Hiz		50	ns

Figure 11 : Serial Channel Timing



XII. TRANSMIT CHARACTERISTICS

XII.1. TEST CONDITIONS

The Tx characteristics depend on the transfer function of the transmit filter. The indicated performance is measured when IIR1 filter implements the 8th order low-pass transfer function (including sinx/x correction) shown in figure 12. This is achieved by loading the coefficients given in table 43.
The frequency response in Fig.12 includes the gain of 72.25dB in front of the biquad 1 (see Fig.A1).

Figure 12 : Filter Transfer Function
(Sampling frequency = 28800Hz, Fsx = 7200Hz, Sample of groups delay = $\frac{1}{(4 \times fsx)}$)

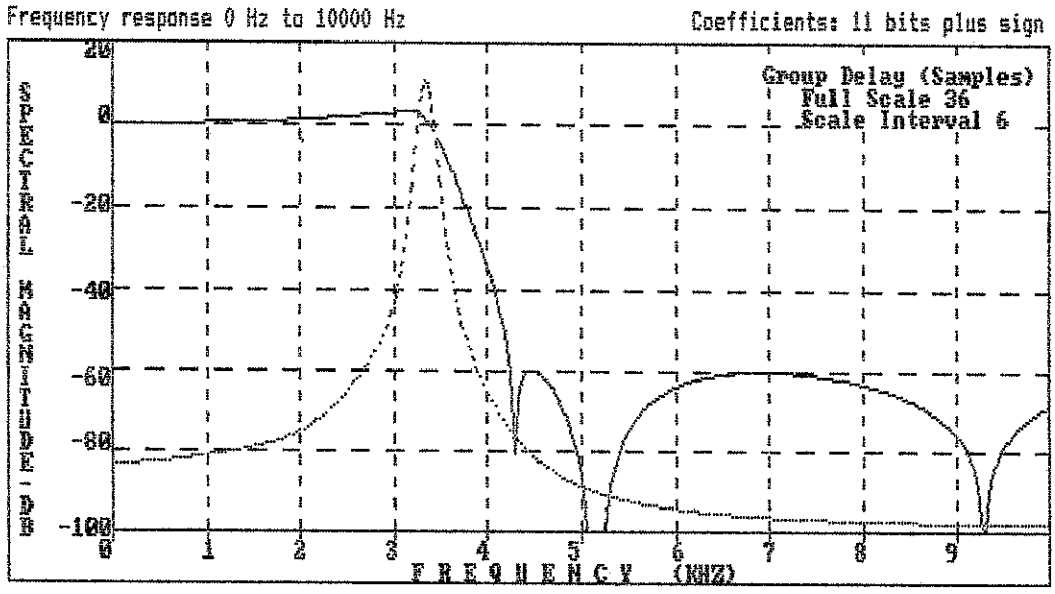


Table 43

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	11	0000,0000	21	abb8,b230	31	a660,ac98
2	0000,0000	12	0000,0000	22	5308,4ef0	32	50e8,4ed0
3	a000,a000	13	a000,a000	23	0950,08d8	33	1570,1e30
4	0000,0000	14	0000,0000	24	4a18,d678	34	4718,d4f0
5	0000,0000	15	0000,0000	25	a000,a000	35	a000,a000
6	0000,0000	16	aa70,afb0	26	adc0,b4e8	36	0000,0000
7	0000,0000	17	6180,5af0	27	4590,4440	37	0000,0000
8	a000,a000	18	01b0,0140	28	04b8,04b0	38	00b8,00a0
9	0000,0000	19	3838,1230	29	da00,cf20	-	
10	0000,0000	20	a000,a000	30	a000,a000	-	

- Filter coefficients (HEX FORMAT) for Fsx equal to 7200 AND 9600Hz respectively

XII.2. PERFORMANCE OF THE TX CHAIN

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V_{DD} = +5V , T_{amb}=25°C and for nominal crystal frequency f_Q=18.432MHz, Fsx = 7.2kHz. (from IIR1 filter input to (TxA1-TxA2) output)

- Measurement band = DC to 3.4kHz
- Tx DPLL free running.

Table 44

Symbol	Parameter	Min	Typ	Max	Unit
Gabs	Absolute gain at 1 kHz	-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Tx signal : V_{OUT} = 2.5 Vpp, f = 1 kHz) fsx = 7200 Hz fsx = 9600 Hz		 -90 -90		 dB dB
DR (1)	Dynamic Range fsx = 7200 Hz fsx = 9600 Hz	 86 87	 89 90		 dB dB
PSRR	Power supply rejection ratio f = 1 kHz, V_{AC} = 200 mVpp	40	50		dB
CTxRx	Crosstalk (transmit channel to receive channel	85	90		dB

Note 1 : Measurement made at -10dB and extrapolated to full scale.

XII.3.SMOOTHING FILTER TRANSFER CHARACTERISTICS

The cut-off frequency of the single pole switch-capacitor low-pass filter is :

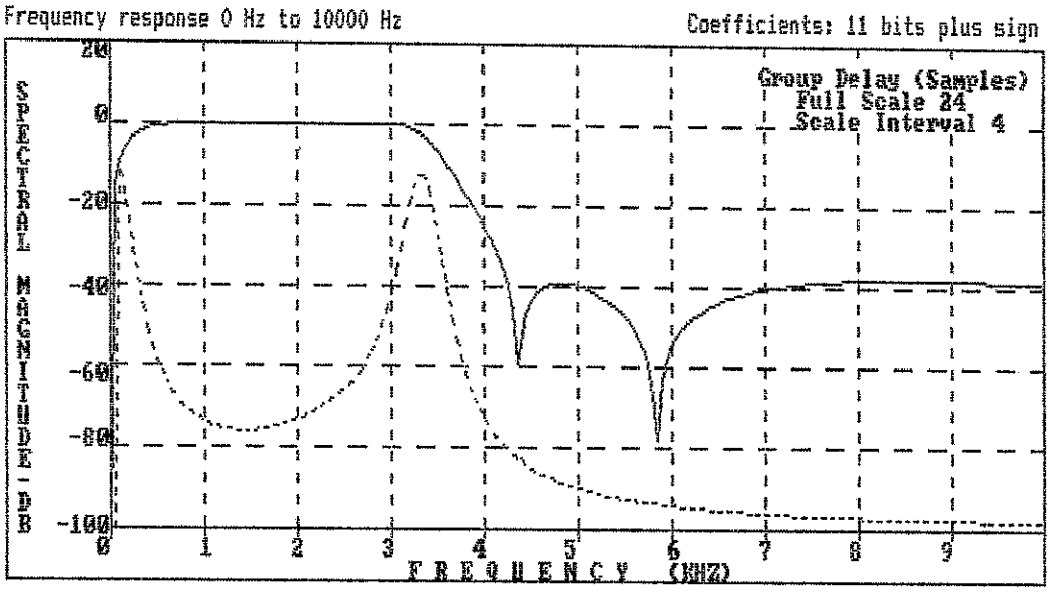
$fc\text{-}3dB = 128 \times Fsx/(2 \times \pi \times 10) \cong 2.04 \times Fsx$

XIII. RECEIVE CHARACTERISTICS

XIII.1. TEST CONDITIONS

The Rx characteristics depend on the transfer function of the receive filter. The indicated performance is measured when IIR2 filter implements the 6th order band-pass transfer function shown in figure 12.bis This is achieved by loading the coefficients given in table 45.

Figure 12bis : Filter Transfer Function
(Sampling frequency = 28800Hz, Fsx = 7200Hz, Sample of groups delay = $\frac{1}{(4 \times fsx)}$)



7543-16.IMG

Table 45

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	11	0000,0000	21	a840,aee0	31	aca0,b3c0
2	0000,0000	12	0000,0000	22	5b08,55f0	32	48c8,46a8
3	a000,a000	13	a000,a000	23	0380,0470	33	2278,1278
4	0000,0000	14	0000,0000	24	5a90,dce8	34	dae8,cfa8
5	0000,0000	15	0000,0000	25	a000,a000	35	a000,a000
6	0000,0000	16	0000,0000	26	b2c0,b600	36	0000,0000
7	0000,0000	17	0000,0000	27	5910,5348	37	0000,0000
8	a000,a000	18	a000,a000	28	0320,0120	38	0040,00c0
9	0000,0000	19	0000,0000	29	0000,0000	-	
10	0000,0000	20	0000,0000	30	e000,e000	-	

- Filter coefficients (HEX FORMAT) for Fsx equal to 7200 AND 9600Hz respectively

XIII.2. PERFORMANCE OF THE RX CHAIN

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V_{DD} = +5V , T_{amb}=25°C and for nominal crystal frequency f_Q=18.432MHz, Fsx = 7.2kHz. (from (RxA1-RxA2) input to IIR2 filter output)

- Measurement band = DC to 3.4kHz
- Tx DPLL free running.

Table 46

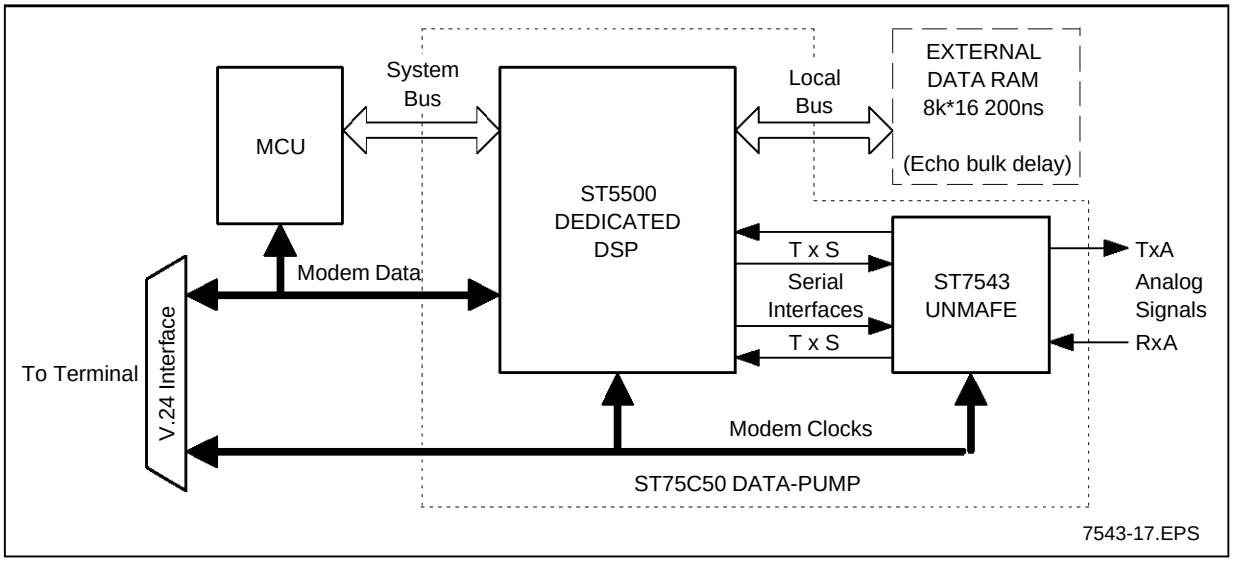
Symbol	Parameter		Min	Typ	Max	Unit
Gabs	Absolute gain at 1 kHz		-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Rx signal : V_{IN} = 2.5 Vpp, f = 1 kHz)					
		Fsx = 7200 Hz		-90		dB
		Fsx = 9600 Hz		-90		dB
DR (1)	Dynamic Range	Fsx = 7200 Hz	86	89		dB
		Fsx = 9600 Hz	87	90		dB
PSRR	Power supply rejection ratio f = 1 kHz, V_{AC} = 200 mVpp		40	50		dB
CRxTx	Crosstalk (receive channel to transmit channel		85	90		dB

Note 1 : Measurement made at -10dB and extrapolated to full scale.

XIV. TYPICAL APPLICATIONS

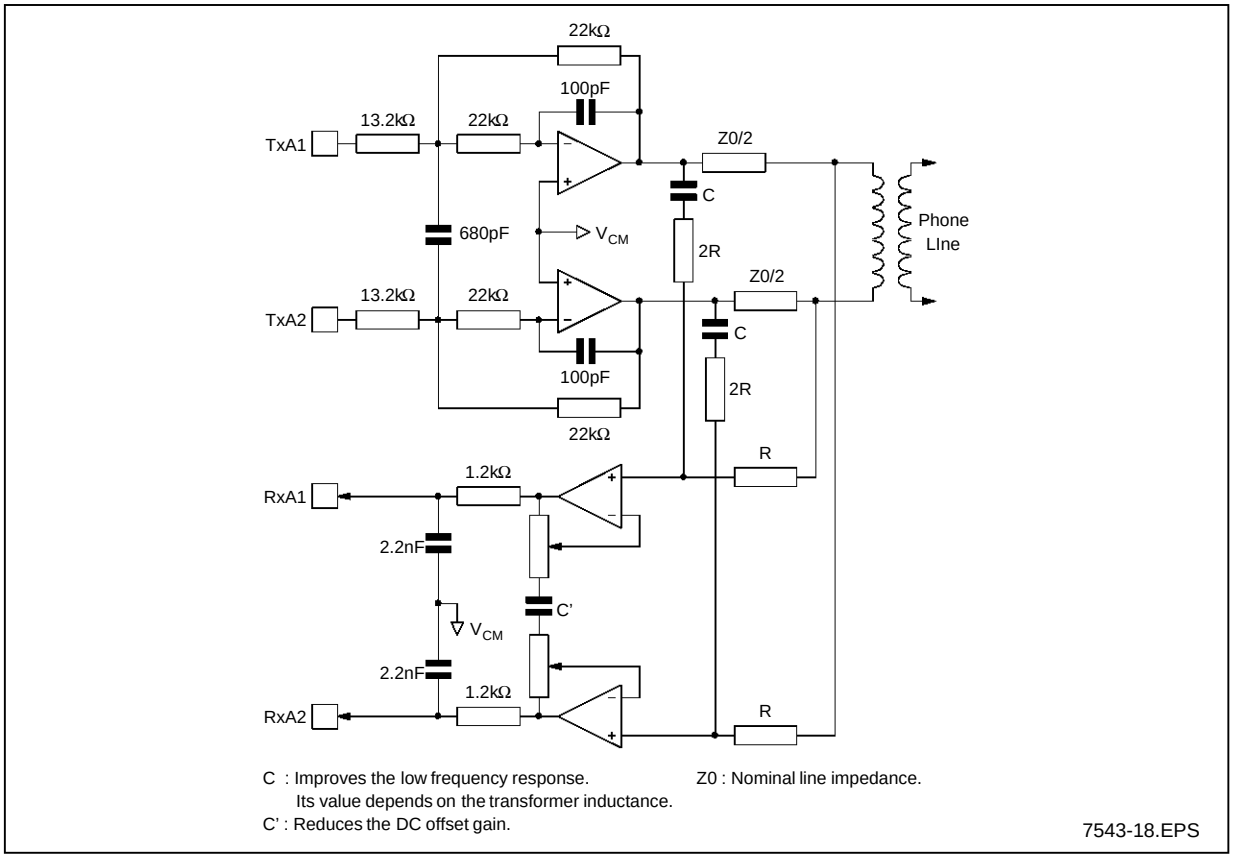
XIV.1. MULTI-STANDARD MODEM WITH ECHO CANCELLING

Figure 13 : Multistandard Modem with Echo Cancelling Capability



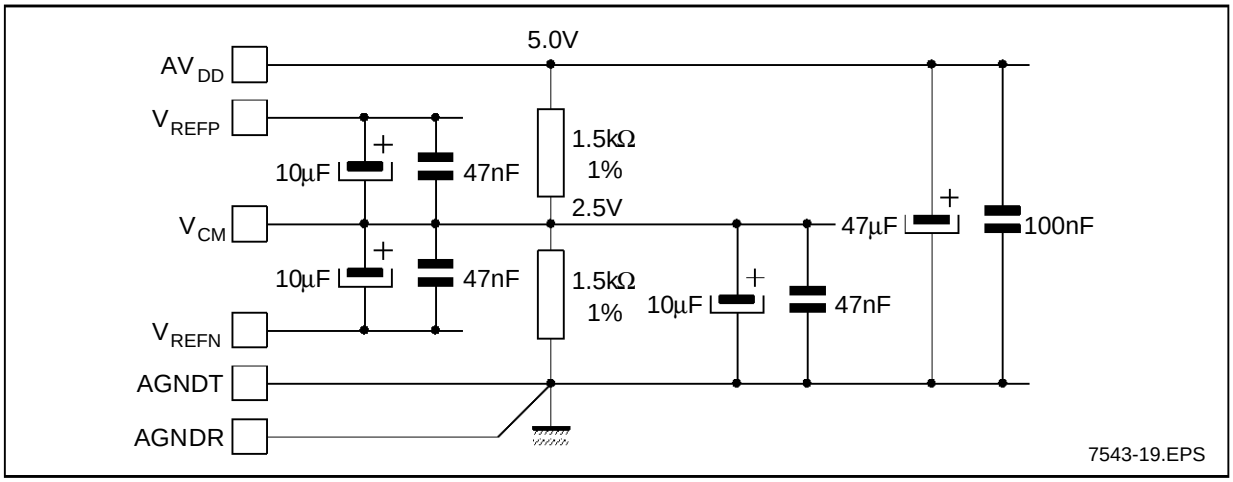
XIV.2. LINE INTERFACE

Figure 14 : Differential Duplexer



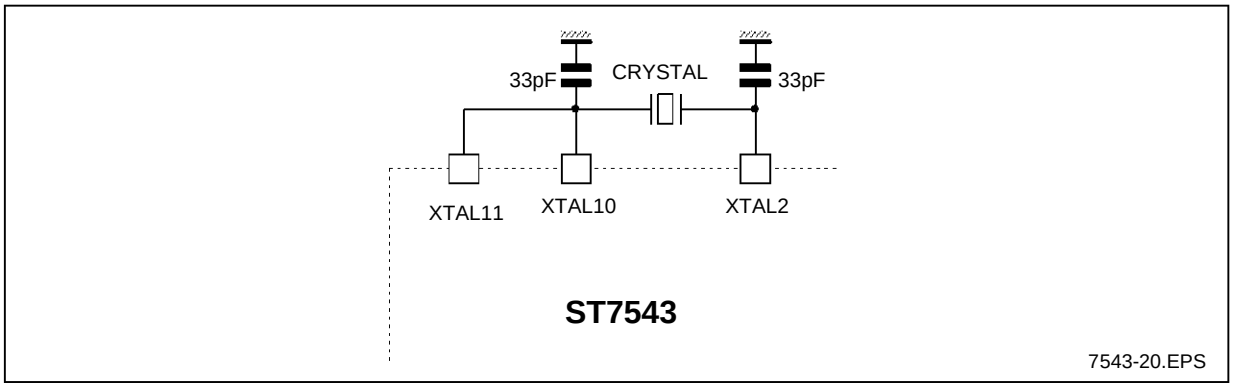
XIV.3. COMMON MODE VOLTAGE GENERATION AND DECOUPLING

Figure 15 : Voltage Decoupling



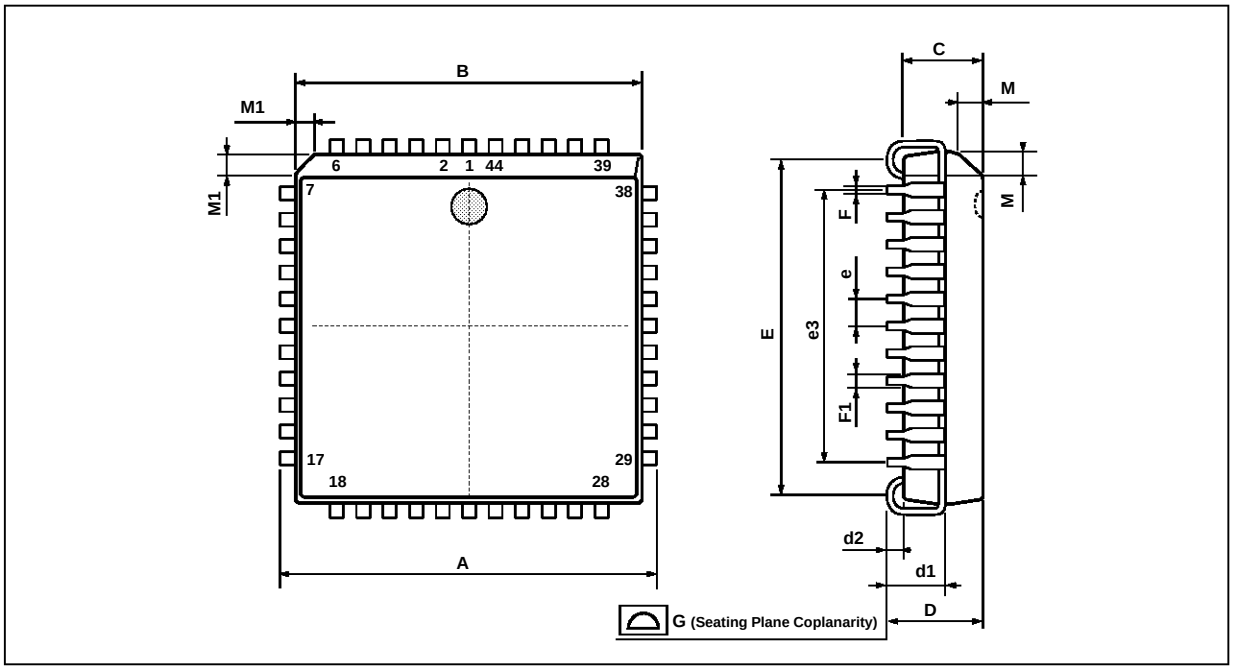
XIV.4. CRYSTAL OSCILLATOR

Figure 16 : External Components for Crystal Oscillator



XV. PACKAGE MECHANICAL DATA

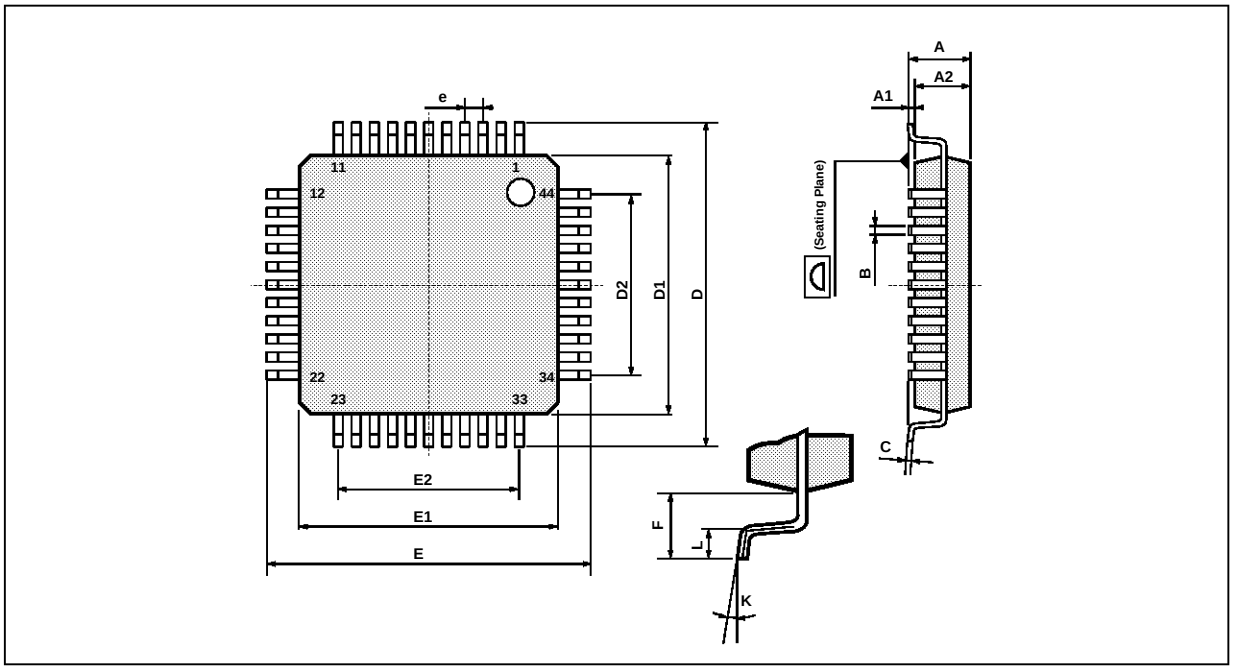
44 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

XV. PACKAGE MECHANICAL DATA

44 PINS - PLASTIC QUAD FLAT PACK



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1		0.25			0.01	
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.35		0.50	0.014		0.020
C			0.17			0.007
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.45	0.60	0.75	0.018	0.024	0.030

ANNEXE A

I. IIR FILTER OPERATION

Each IIR filtering section included in the ST7543 can perform up to seven biquadratic transfer functions in cascade, operating at four times the sampling frequency (figure A1).
Each biquad is defined by five coefficients, A, B, C, D and E (figure A2). An additional coefficient ,F, scales the IIR filter output.
Unused biquads are made transparent by programming A to one and the four remaining coefficients to zero. Such biquads should preferably be located in the first sections of the IIR filter in order to reduce the calculation noise.

I.1. COEFFICIENT ROUNDING

Initially, coefficients of the filter to be implemented must be exclusively between +2 and -2. To derive the actual usable 12+1 bit coefficients, the rounding process described in figure A3 must be performed. Each 13 bit coefficient K is split into its doubling factor K2, and its 12 bit basic value K1, as the IIR architecture works with 12 bit coefficients and uses an extra accumulation when coefficient doubling is needed.

$$K2\ [0,1] \text{ and } -2^{12} < K1 < 2^{12}$$

The coefficients are loaded into the different IIR filters through 16bit wide time slots. The format to be used is as follows :

MSB		LSB
K2	K1	0 0 0
(1 bit)	(12 bits)	(3 bits)

To programme one IIR filter it is necessary to send five words per biquad followed by two additional words set to zero and the F coefficient word :
B(1), C(1), A(1), D(1), E(1), B(2),..., E(7), 0000_H, 0000_H, F
The total number of words send is therefore 38.

I.2. DETAILED OPERATION

The architecture of the device supporting the IIR filter is based on 28 bit data path. The basic function is as follows: one coefficient K(N) is multipled by one sample X(N) followed by one accumulation with value clampling. It can be precisely described as follows :

```
FUNCTION PAC K(N), X(N), S
  LOCAL P
  P = TRUNC (K1(N)*X(N)/2^12)
  S = S + P
  IF ABS(S)  2^27 THEN
    IF SIGN(S) > 0 THEN CLAMP S TO 2^27-1
                   ELSE CLAMP S TO 2^27
  IF K2(N) = 1 THEN S = S + P
  IF ABS(S)  2^27 THEN
    IF SIGN(S) > 0 THEN CLAMP S TO 2^27-1
                   ELSE CLAMP S TO 2^27

END OF FUNCTION.
```

The TRUNC function is a two's complement truncature.
As previously mentionned, the second accumulation is controlled by the doubling factor K2(N).
The complete process of computing 16 bit output samples (V_{OUT}) from 16-bit input samples (V_{IN}) appears in figure A4.

Figure A1 : IIR Filter Diagram

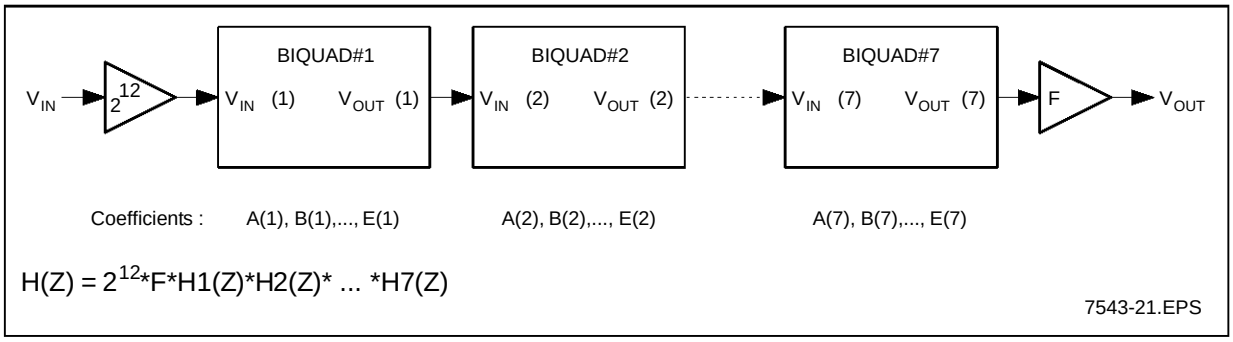
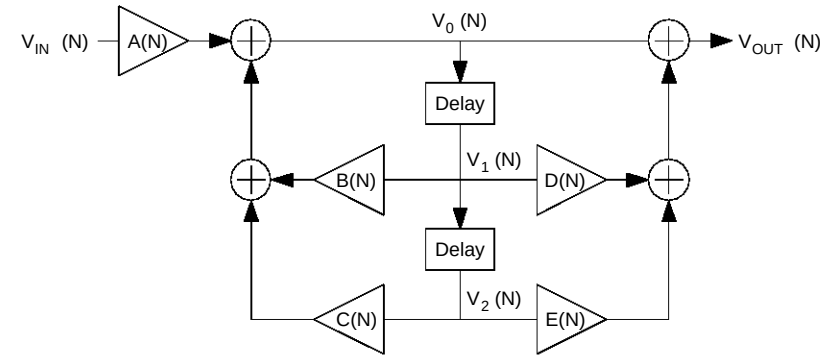


Figure A2 : BIQUAD Structure



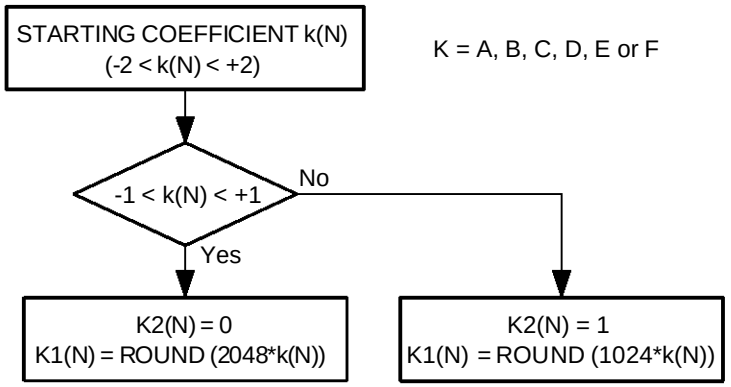
$$Hn(Z) = A\frac{1 + DZ^{-1} + EZ^{-2}}{1 - BZ^{-1} - CZ^{-2}}$$

Equation Set : $V_0(N) = B(N) \times V_1(N) + C(N) \times V_2(N) + A(N) \times V_{IN}(N)$
$V_{OUT}(N) = V_0(N) + D(N) \times V_1(N) + E(N) \times V_2(N)$

Next Step with : $V_2(N) = V_1(N)$
$V_1(N) = V_0(N)$

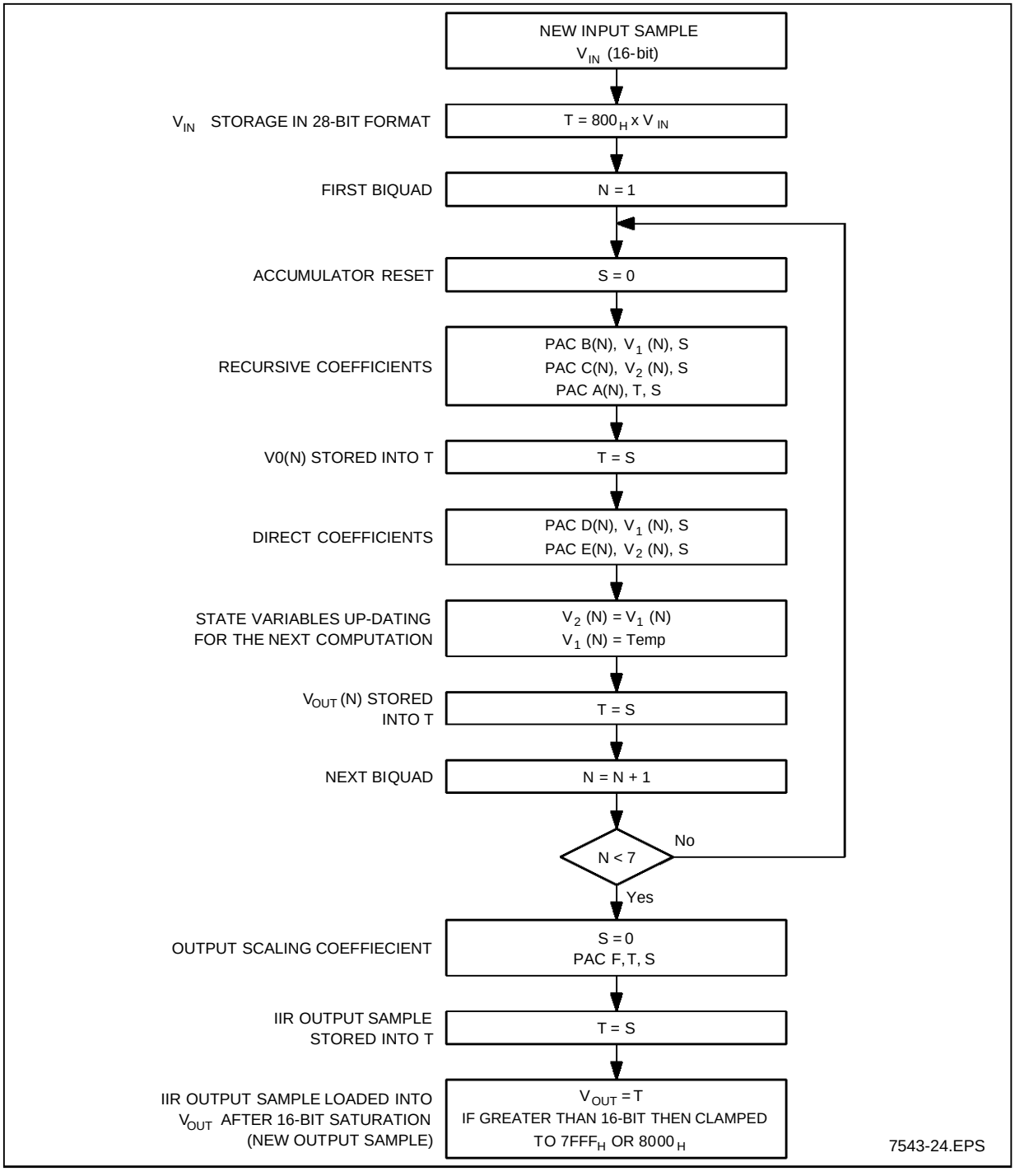
7543-22.EPS

Figure A3 : IIR Coefficients Rounding



7543-23.EPS

Figure A4 : IRR Operating Sequence



APPLICATION NOTE
ST7543 programming Example. Dual Serial Port mode.

Below, find an ST7543 programming example. This example takes into account the hardware and the software configuration.

I. EXAMPLE OF CONFIGURATION (different from power-on default configuration)

- One external clock : 18.432MHz
- Serial port mode : Dual
- Transmit sampling frequency : 7200Hz
- Receive sampling frequency : 9600Hz
- Bit frame clock frequency : 128 x Fsx(r)
- Transmit bit clock frequency : 14400Hz
- Receive bit clock frequency : 14400Hz
- Transmit baud clock frequency : 2400Hz
- Receive baud clock frequency : 2400Hz
- DPLL Tx : free running
- Transmit Filter : Low-Pass (table 43) (1)
- Receive FIlter : Band-Pass (table 45)
- Interpollation Filter : Low-Pass (table 43)

II. HARDWARE CONFIGURATION

- XTAL10 and XTAL11 hard-wired to the external clock.
- TxDI and RxDI must be tied to V_{DD} while the serial interface is not managed by the host processor.
- RC network on NRESET pin. Typically RC = 10ms (R=100kΩ, C=100nF). (This time must include the external clock start time, and the ST7543 set up time.)
- SSIM pin tied to DVDD : Dual serial port mode.
- BFRS pin tied to DVDD : Bit frame frequency set to 128 x Fsx(r).

III. SOFTWARE CONFIGURATION

Writing convention :

'x'	frame number.
FRAME x.1	frame for RAM 1 loading.
FRAME x.2	frame for RAM 2 loading.
FRAME x.3	frame for RAM 3 loading.
'#'	delimits a programmer's remark (comments).
'b'	indicate a binary number.
'h'	indicate an hexadecimal number.
'XXXX'	user defined.

 # SYNCHRONOUS SERIAL INTERFACE A.

#RAM 1 COEFFICIENT LOADING

#

#**FRAME 0.1**. Select the right Sampling frequency and set Stb bit in order to select a RAM

B980h	#TxI0	MS	= 1	Coefficient Loading Mode selected
#		Stb	= 0	Start bit coefficient loading actived
#		QS	= 1	XTAL10 Selected
#		RAi	= 11b	No RAM accessed
#		ADi	= 001b	TxCR1 selected
#		Di	= 80h	Fsx = 7200Hz, Txrclk = 2400Hz
#				TxHSCLK = 6.144MHz
#				Band Split mode inactive
FFFFh	#TxI1			
FFFFh	#TxI2			
FFFFh	#TxI3			

#

#

#**FRAME 1.1** Select RAM 1 and start the coefficient loading of the LowPass filter (table 43),
#and select TxCLK = 14400Hz

E0F0h	#TxI0	MS	= 1	
#		Stb	= 1	
#		QS	= 1	
#		RAi	= 00b	RAM 1 selected
#		ADi	= 000b	TxCR0 selected
#		Di	= F0h	TxCLK = 14400Hz
FFFFh	#TxI1	unused		
0000h	#TxI2	word 1 RAM 1 (1st IIR coefficient)		
0000h	#TxI3	word 2 RAM 1		

#

#

#**FRAME 2.1** RAM 1 coefficient loading, fCOMP and f_{SHIFT} programming and Stb bit ready to select
#an another RAM

A300h	#TxI0	MS	= 1	
#		Stb	= 0	
#		QS	= 1	
#		RAi	= 00b	RAM 1 selected
#		ADi	= 011b	TxCR3 selected
#		Di	= 00h	f_{COMP} = 2400Hz, f_{SHIFT} =Ffsx/2
A000h	#TxI1	word 3 RAM 1		
0000h	#TxI2	word 4 RAM 1		
0000h	#TxI3	word 5 RAM 1		

#

#**FRAME 3.1** RAM 1 coefficient loading, no control register #access

A7FFh	#TxI0			
A000h	#TxI1	word 6 RAM 1		
0000h	#TxI2	word 7 RAM 1		
0000h	#TxI3	word 8 RAM 1		

#

#

#**FRAME 4.1 to FRAME 12.1**
A7FFh #TxI0 idem frame 3.1
XXXXh #TxI1
XXXXh #TxI2
XXXXh #TxI3
#
#
#**FRAME 13.1** Last RAM 1 loading frame.
#
A7FFh #TxI0
0000h #TxI1 word 36 RAM 1
0000h #TxI2 word 37 RAM 1
00B8h #TxI3 word 38 RAM 1
#
#
#
#**RAM 2 COEFFICIENT LOADING**
#
#**FRAME 1.2** Select RAM 2 and start the coefficient loading of the BandPass filter (table 45),
#no control register access.
EFFFh #TxI0 MS = 1
Stb = 1
QS = 1
RAi = 01b RAM 2 selected
ADi = 111b
FFFFh #TxI1 unused
0000h #TxI2 word 1 RAM 2
0000h #TxI3 word 2 RAM 2
#
#
#**FRAME 2.2** RAM 2 coefficient loading, no control register access and Stb bit ready to select another RAM.
AFFFh #TxI0 MS = 1
Stb = 0
QS = 1
RAi = 01b RAM 2 selected
ADi = 111b
A000h #TxI1 word 3 RAM 2
0000h #TxI2 word 4 RAM 2
0000h #TxI3 word 5 RAM 2
#
#
#**FRAME 3.2 to FRAME 12.2**
AFFFh #TxI0 idem frame 2.2
XXXXh #TxI1
XXXXh #TxI2
XXXXh #TxI3
#
#**FRAME 13.2** Last RAM 2 loading frame.
#
AFFFh #TxI0
0000h #TxI1 word 36 RAM 2
0000h #TxI2 word 37 RAM 2
0040h #TxI3 word 38 RAM 2

```
#
#
#
#RAM 3 COEFFICIENT LOADING
#FRAME 1.3 Select RAM 3 and start the coefficient loading of the LowPass filter (table 43),
#no control register access
F7FFh   #TxI0   MS   = 1
#               Stb  = 1
#               QS   = 1
#               RAi  = 10b    RAM 3 selected
#               ADi  = 111b
FFFFh   #TxI1   unused
0000h   #TxI2   word 1 RAM 3
0000h   #TxI3   word 2 RAM 3
#
#
#FRAME 2.3 RAM 3 coefficient loading, no control register access and Stb bit ready to select another RAM
B7FFh   #TxI0
A000h   #TxI1   word 3 RAM 3
0000h   #TxI2   word 4 RAM 3
0000h   #TxI3   word 5 RAM 3
#
#
#FRAME 3.3 to FRAME 12.3
B7FFh   #TxI0   idem frame 3.2
XXXXh   #TxI1   word 6 RAM 3
XXXXh   #TxI2   word 7 RAM 3
XXXXh   #TxI3   word 8 RAM 3
#
#
#FRAME 13.3 Last RAM 3 loading frame.
B2C4h   #TxI0   MS   = 1
#               Stb  = 0
#               QS   = 1
#               RAi  = 10b    RAM 3 selected
#               ADi  = 010    TxCR2 selected
#               Di   = C4     0dB attenuation on Transmit channel
#                             and synchonize the TxCLK clock on TxRCLK
0000h   #TxI1
0000h   #TxI2
00B8h   #TxI3
#
#
#FRAME 14
3FFFh   #TxI0   MS   = 0      DATA mode selected
#               Stb  = 0      ready to select a reading RAM
#               QS   = 1
#               RAi  = 11     No RAM access
#               ADi  = 111    No control register access
XXXXh   #TxI1   TxSig (fig 5bis)
XXXXh   #TxI2   ResSig (fig 5bis)
FFFFh   #TxI3   unused
```

 # SYNCHRONOUS SERIAL INTERFACE B. (2)

```
#
#FRAME 0. Select the right Sampling frequency.
0105h   #Trl0    ADi   = 001b   RxCR1 selected
#                Di    = 05h    Fsr = 9600Hz, Rxrclk = 2400Hz
#                                RxHSCLK = 6.144MHz
#                                ECK = 1
FFFFh   #Trl1
FFFFh   #Trl2
FFFFh   #Trl3
#
#
#FRAME 1. Select the right receive bit clock (RxCLK) frequency.
00F0h   #Trl0    ADi   = 000b   RxCR0 selected
#                Di    = F0h    RxCLK = 14400Hz
FFFFh   #Trl1
FFFFh   #Trl2
FFFFh   #Trl3
#
#
#FRAME 2. No phase shift selected.
0200h   #Trl0    ADi   = 010b   RxCR2 selected
#                Di    = 00h    No phase shift
FFFFh   #Trl1
FFFFh   #Trl2
FFFFh   #Trl3
#
#
#FRAME 3. Synchronization of RxCLK on RxRCLK.
0304h   #Trl0    ADi   = 011b   RxCR1 selected
#                Di    = 04h    synchronize RxCLK on RxRCLK.
FFFFh   #Trl1
FFFFh   #Trl2
FFFFh   #Trl3
#
#
#FRAME 4
FFFFh   #Trl0    ADi   = 111    No control register access
XXXXh   #Trl1    EYEX-EYEY (fig 5bis)
FFFFh   #Trl2    reserved (fig 5bis)
FFFFh   #Trl3    reserved
#
```

(2) A and B interfaces can be used simultaneously.

APPLICATION NOTE
Filter coefficient coding in ST7543 time-slot format

The following is an example of filter coefficient coding in ST7543 time-slot format. This example is corresponding to the Low-Pass filter defined in the DATASHEET (see Table 43).

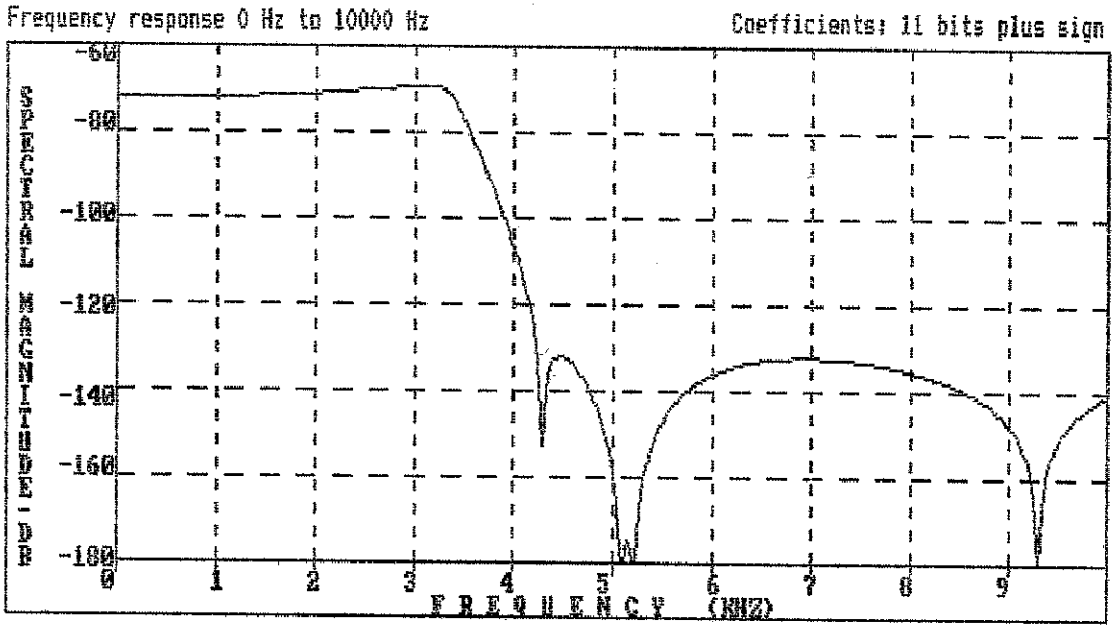
I. FILTER CHARACTERISTICS

Type	: Elliptique Low-Pass.
Order	: 8
Sampling Frequency	: 4*7.2kHz = 28.8kHz.
PassBand	: 3200Hz.
StopBand	: 4200Hz.
PassBand ripple	: 0.1dB.
Stopband loss	: 60dB.
Coefficient wordlength	: 11 bits + sign.

NOTA: The design filter must include a sinx/x correction at fs=7.2kHz (the sample input at fs=7.2kHz and are sampled at 4 x 7.2kHz in the IIR filter).

II. TRANSFER FUNCTION

Figure A5 : Sampling frequency = 28800Hz



7543-25.TIF

Decimal value and 11bits + sign format for coefficients of second-order sections: $A\frac{Z^{\wedge}2 + D\,Z + E}{Z^{\wedge}2 - B\,Z - C}$

A	D	E	B	C
1.0000000 1024 * 2	0.0000000 0	0.0000000 0	0.0000000 0	0.0000000 0
1.0000000 1024 * 2	0.0000000 0	0.0000000 0	0.0000000 0	0.0000000 0
1.0000000 1024 * 2	0.0000000 0	0.0000000 0	0.0000000 0	0.0000000 0
0.0263672 54	0.8784180 1799	1.0000000 1024 * 2	1.3261720 1358 * 2	-0.4765625 -976
0.1455078 298	-0.8422852 -1725	1.0000000 1024 * 2	1.3662111 1399	-0.7026367 -1439
0.0737305 151	-1.1875000 -1216 * 2	1.0000000 1024 * 2	1.4296880 1464 * 2	-0.9130859 -1870
0.3349609 686	-0.8891602 -1821	1.0000000 1024 * 2	1.1992190 1228 * 2	-0.7358398 -1507
0.0112305 23	0.0000000 0	0.0000000 0	0.0000000 0	0.0000000 0

III.COEFFICIENT CODING IN ST7543 TIME-SLOT FORMAt

Example of subroutine to code the coefficients in the ST7543 time-slot format.

```
SUB CODE(A(),NbBiquad,AA())
LOCAL i,EXTRABIT()
  FOR i=1 To NbBiquad
    IF ABS(A(i)) =1 THEN
      EXTRABIT(i)= -32768
      AA(i) = CINT((A(i)/2) * 2048)
    ELSE
      EXTRABIT(i) = 0
      AA(i) = CINT(A(i) * 2048)
    END IF
      AA(i) = (AA(i) << 3) AND 32767
      AA(i) = (AA(i) OR EXTRABIT(i))
  NEXT
END SUB
```

With :

INPUT :

NbBiquad Number of biquadratic function.

A() Coefficient in decimal format.

OUTPUT :

AA() Coefficient in ST7543 time-slot format.

Writing convention:

ABS() return an absolute value.

CINT() convert its argument to an integer.
(if the fractional part of an argument is equal to 0.5, it is rounded toward the even number).

< <n Left shift of n bit.

Filter Coefficient in Hexadecimal format (see Table 43).

No	B	C	A	D	E
1	0000	0000	A000	0000	0000
2	0000	0000	A000	0000	0000
3	0000	0000	A000	0000	0000
4	AA70	6180	01B0	3838	A000
5	ABB8	5308	0950	4A18	A000
6	ADC0	4590	04B8	DA00	A000
7	A660	50E8	1570	4718	A000
8	0000	0000	00B8	0000	0000