

TC74AC166P, TC74AC166F, TC74AC166FN

8 - BIT SHIFT REGISTER (P - IN, S - OUT)

The TC74AC166 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

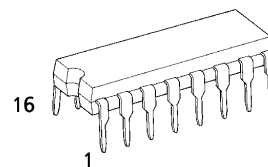
It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

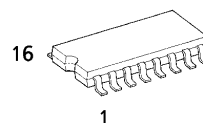
FEATURES:

- High Speed..... $f_{\text{MAX}} = 170\text{MHz}(\text{typ.})$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}(\text{Min.})$
- Symmetrical Output Impedance..... $|I_{\text{OH}}| = |I_{\text{OL}}| = 24\text{mA}(\text{Min.})$
Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range..... $V_{\text{CC}}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74HC166

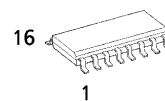
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

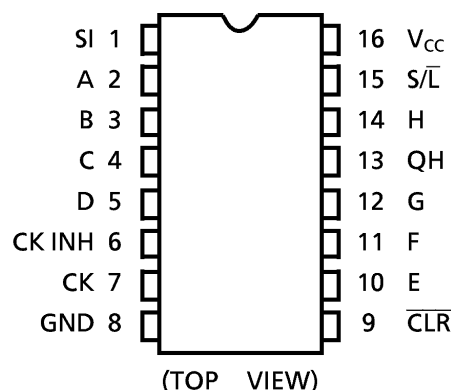


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

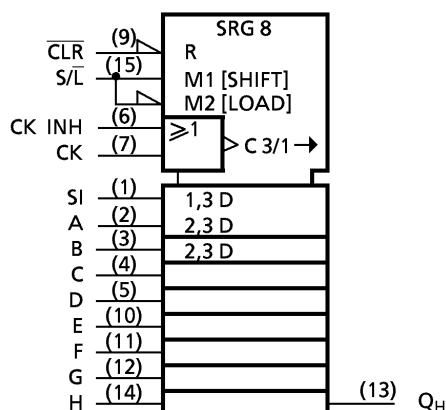


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



961001EBA2

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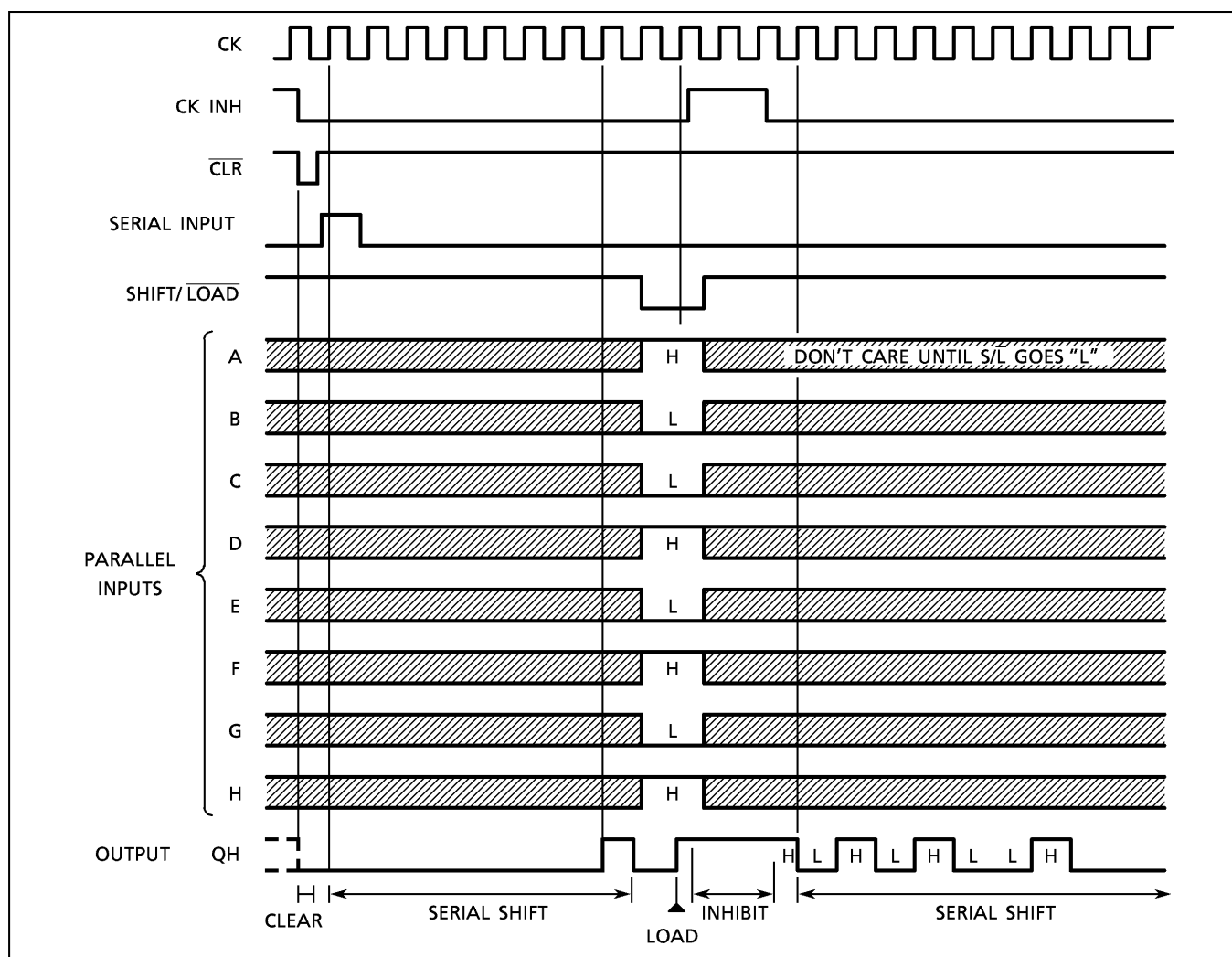
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLR	SHIFT/LOAD	CK INH.	CK	SERIAL IN	PARALLEL A H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	X		X	X	NO CHANGE		
H	L	L		X	a h	a	b	h
H	H	L		H	X	H	QAn	QGn
H	H	L		L	X	L	QAn	QGn
H	X	H	X	X	X	NO CHANGE		

X : Don't Care

a h : The level of steady state input voltage at inputs A through H respectively

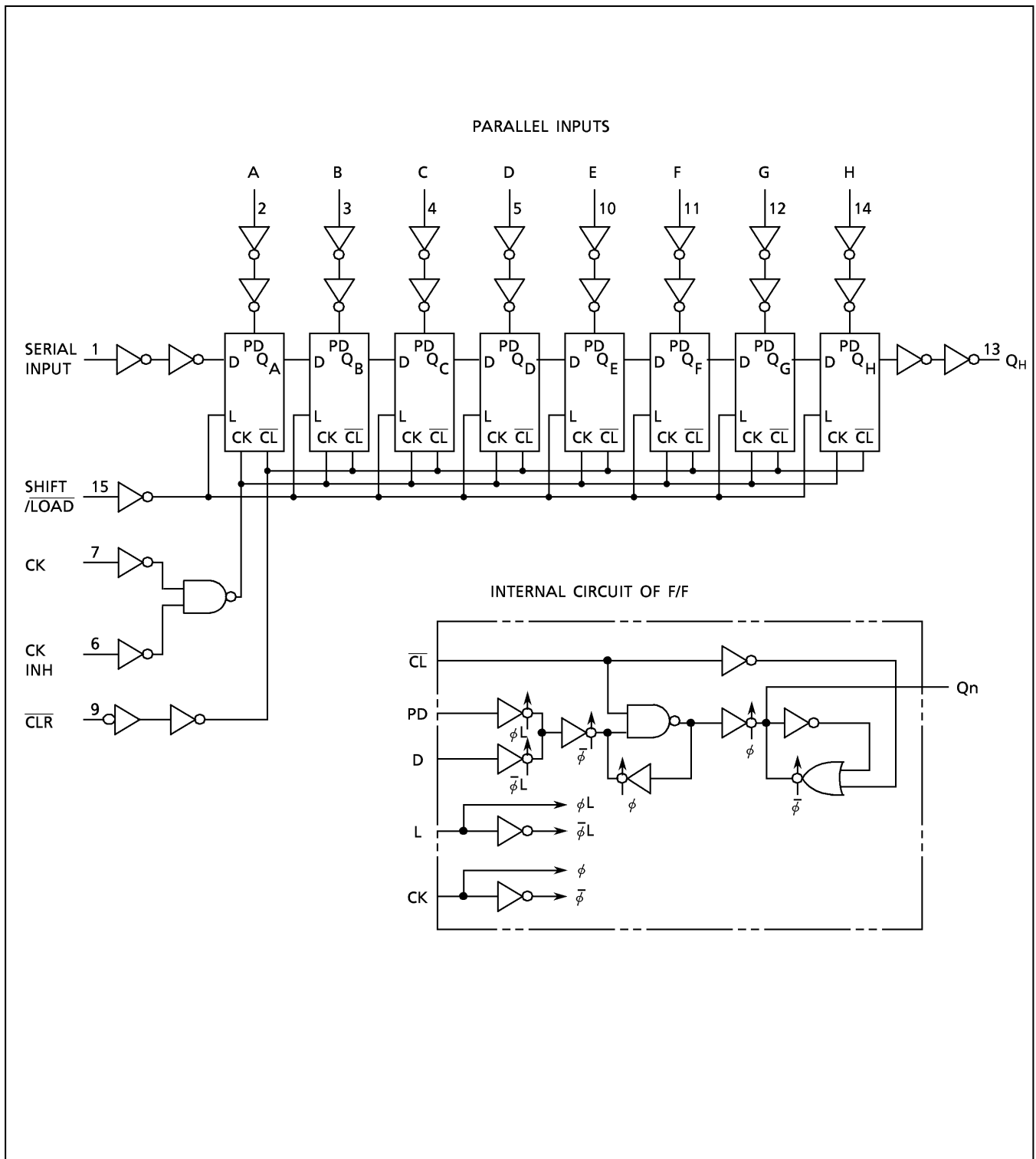
TIMING CHART



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			$I_{OH} = -4\text{mA}$	3.0	2.58	—	—	2.48	
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 12\text{mA}$	3.0	—	—	0.36	—	
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	1.65	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3	7.0	7.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	5.0	
Minimum Pulse Width ($\overline{\text{CLR}}$)	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	8.0 5.0	8.0 5.0	8.0 5.0	
Minimum Set-up Time (SI, PI)	t_s		3.3 ± 0.3 5.0 ± 0.5	8.0 4.0	8.0 4.0	8.0 4.0	
Minimum Set-up Time (S/ $\overline{\text{L}}$)	t_s		3.3 ± 0.3 5.0 ± 0.5	7.0 4.0	7.0 4.0	7.0 4.0	
Minimum Hold Time (SI, PI)	t_h		3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	0.5 0.5	
Minimum Hold Time (S/ $\overline{\text{L}}$)	t_h		3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{\text{CLR}}$)	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	4.0 1.5	4.0 1.5	4.0 1.5	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500 Ω , Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK—QH)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	9.4	16.1	1.0	18.3	ns
			5.0 ± 0.5	—	6.6	10.0	1.0	11.4	
Propagation Delay Time ($\overline{\text{CLR}}$ —QH)	t _{pHL}		3.3 ± 0.3	—	9.2	15.2	1.0	17.4	
			5.0 ± 0.5	—	6.4	9.6	1.0	10.9	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	55	105	—	55	—	MHz
			5.0 ± 0.5	90	150	—	90	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	67	—	—	—	

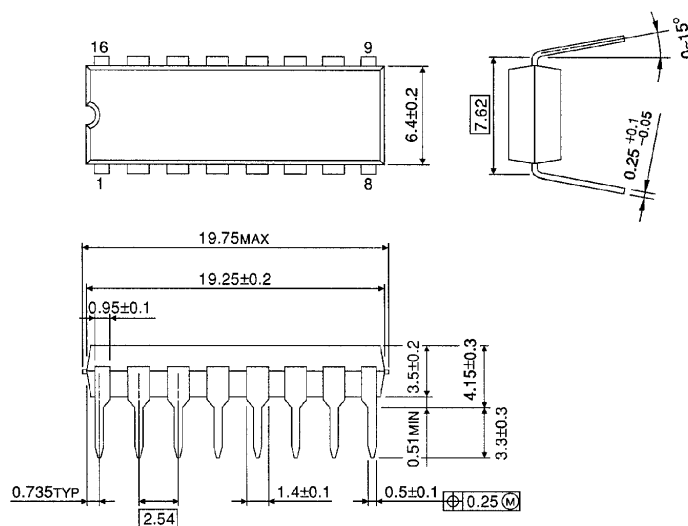
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

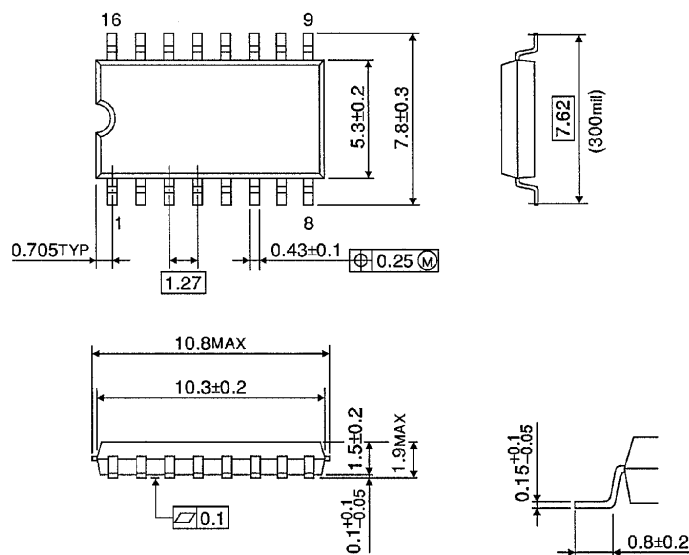
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

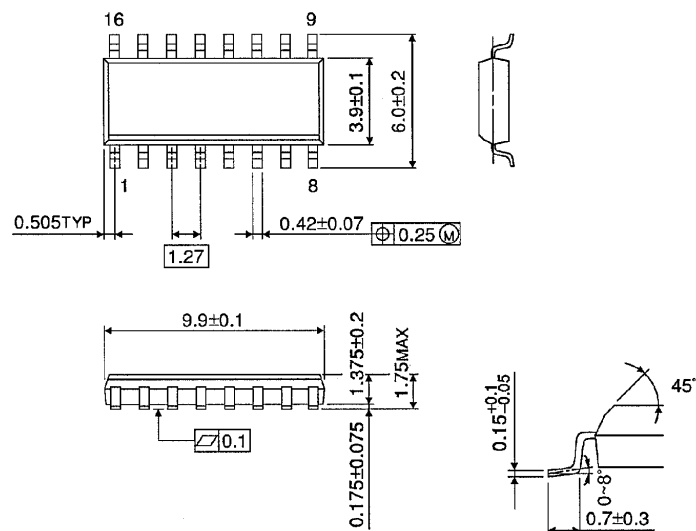


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)