

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT240P, TC74ACT240F, TC74ACT240FW, TC74ACT240FT TC74ACT244P, TC74ACT244F, TC74ACT244FW, TC74ACT244FT

OCTAL BUS BUFFER

TC74ACT240P/F/FW/FT INVERTED, 3-STATE OUTPUTS

TC74ACT244P/F/FW/FT NON-INVERTED, 3-STATE OUTPUTS

The TC74ACT240 and 244 are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74ACT240 is an inverting 3-state buffer while the 74ACT244 is non-inverting. Both devices have two active-low output enables.

These devices are designed to be used in such applications as 3-state memory address drivers.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $t_{pd} = 5.0\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IL} = 0.8\text{V}(\text{Max.})$
 $V_{IH} = 2.0\text{V}(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F240/244

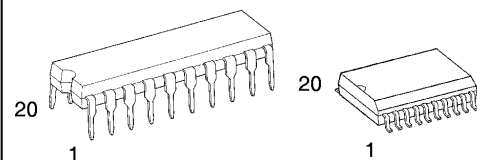
TRUTH TABLE

INPUTS		OUTPUTS	
$\bar{G}$	A_n	$Y_n(244)$	$\bar{Y}_n(240)$
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care

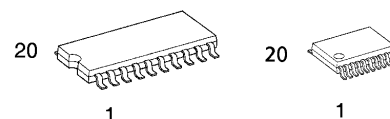
Z : High Impedance

(Note) The JEDEC SOP (FW) is not available in Japan.



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)

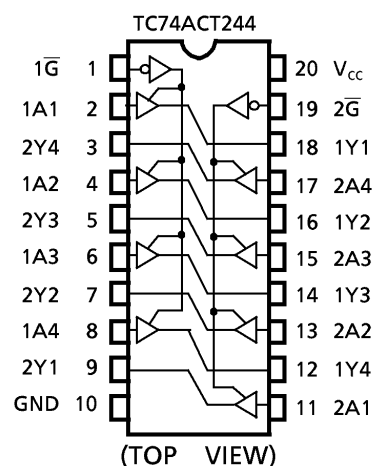
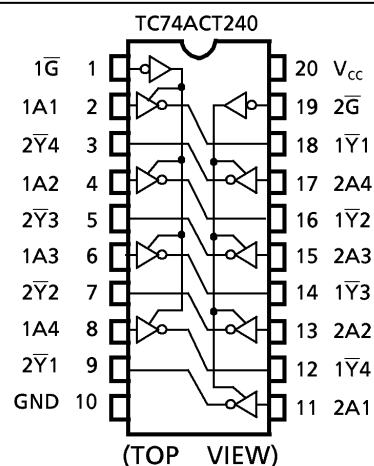
FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)



F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)

FT (TSSOP20-P-0044-0.65)
Weight : 0.08g (Typ.)

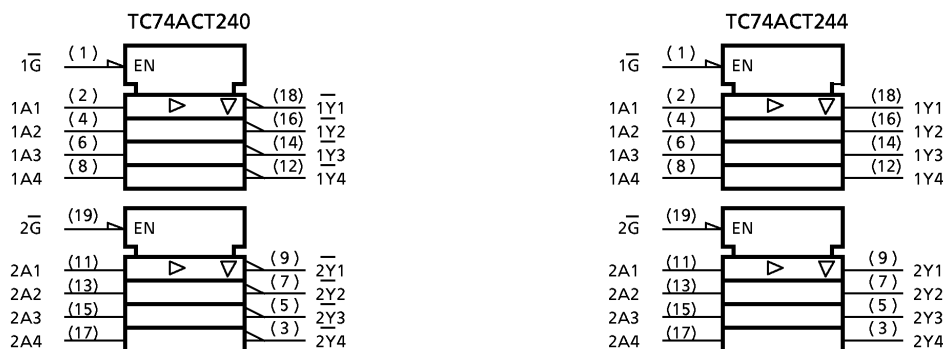
PIN ASSIGNMENT



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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	0~10	ns/V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}		4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50μA I _{OH} = -24mA I _{OH} = -75mA*	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	— — —	4.4 3.80 3.85	— — —	V
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA I _{OL} = 24mA I _{OL} = 75mA*	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	
	I _C	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND	5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH} t _{pHL}		5.0 ± 0.5	—	5.7	8.0	1.0	9.0	ns
Output Enable Time	t _{pZL} t _{pZH}		5.0 ± 0.5	—	6.0	9.0	1.0	10.5	
Output Disable Time	t _{pLZ} t _{pHZ}		5.0 ± 0.5	—	5.9	8.5	1.0	10.0	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Output Capacitance	C _{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)	TC74ACT240		—	25	—	—	—	
		TC74ACT244		—	29	—	—	—	

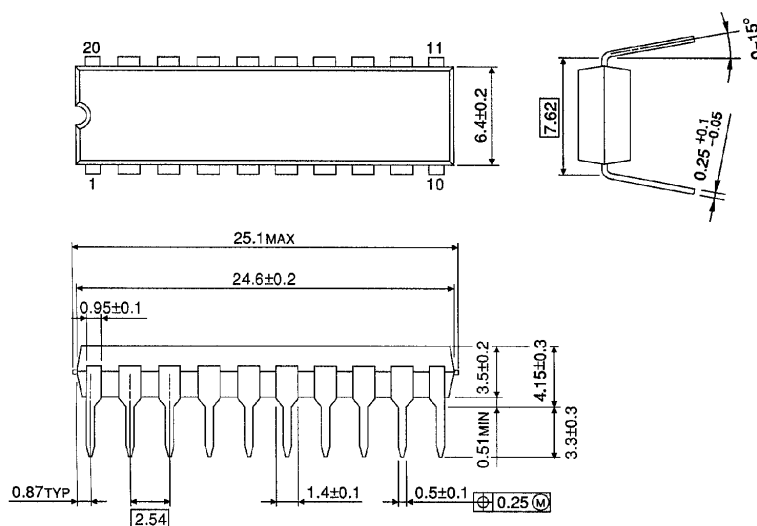
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 (\text{per bit})$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

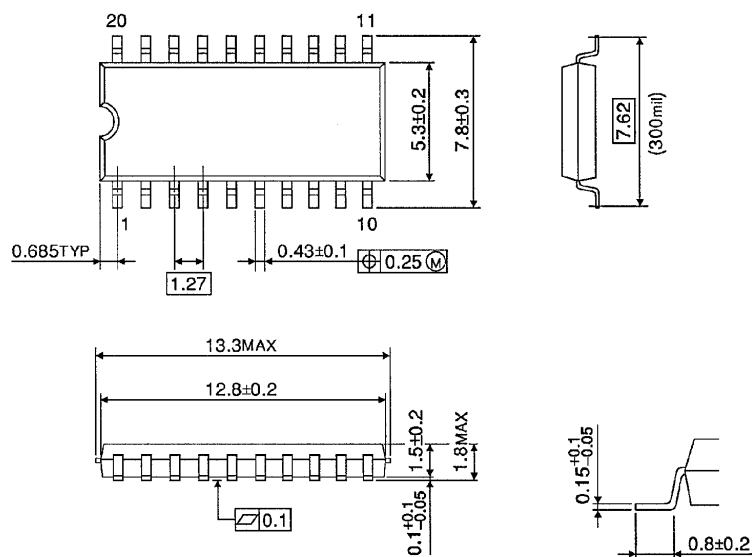
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

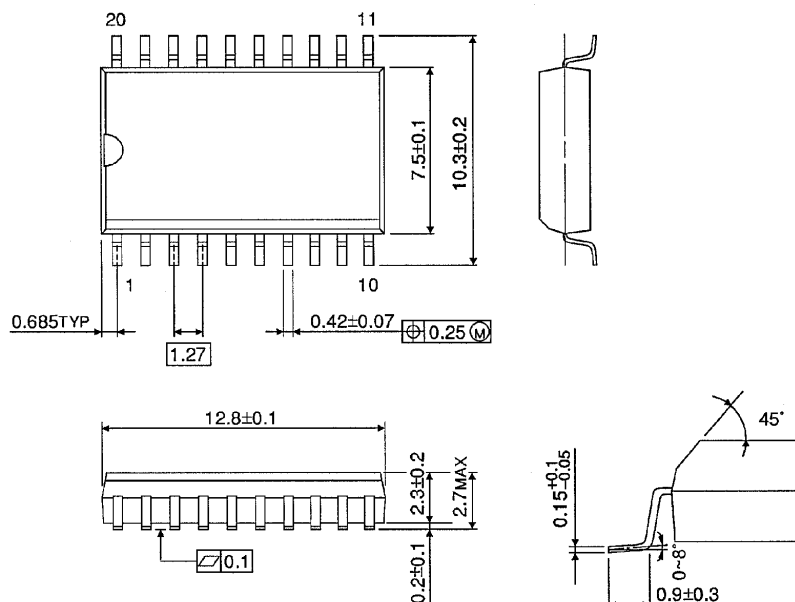


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

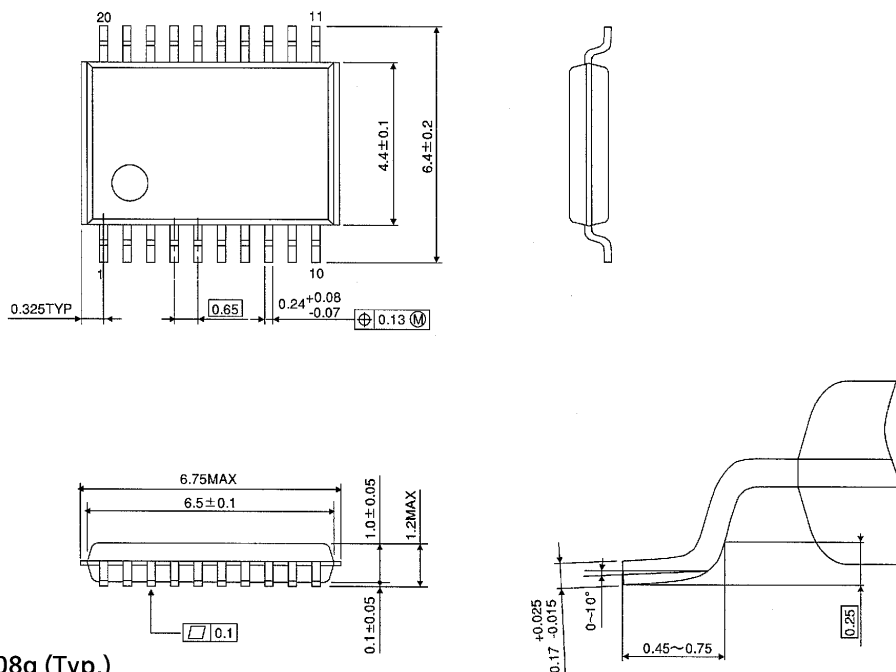
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)