

TC74LVX374F, TC74LVX374FW, TC74LVX374FT

OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUT

The TC74LVX374 is a high speed CMOS OCTAL D-FLIP FLOP fabricated with silicon gate C²MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

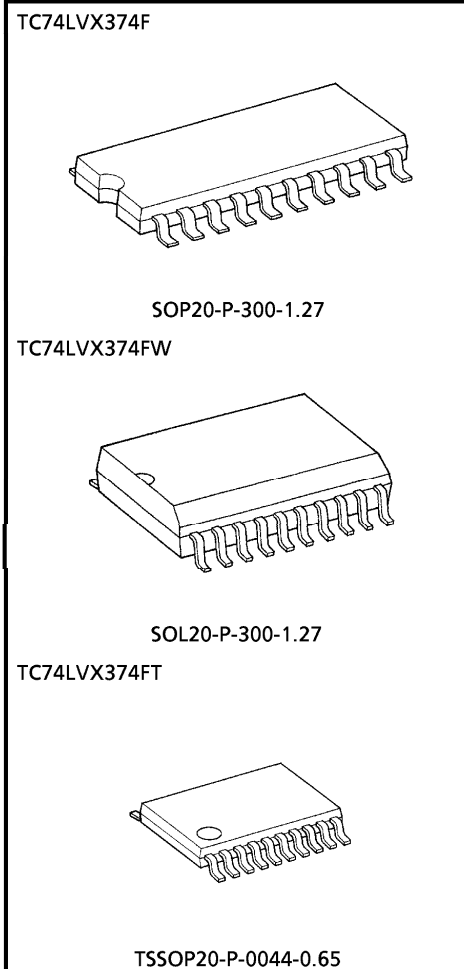
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $f_{MAX} = 160\text{MHz}$ (Typ.) ($V_{CC} = 3.3\text{V}$)
- Low power dissipation : $I_{CC} = 4\mu\text{A}$ (Max.) ($T_a = 25^\circ\text{C}$)
- Input voltage level : $V_{IL} = 0.8\text{V}$ (Max.) ($V_{CC} = 3\text{V}$)
 $V_{IH} = 2.0\text{V}$ (Min.) ($V_{CC} = 3\text{V}$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{PLH} \approx t_{PHL}$
- Low noise : $V_{OLP} = 0.8\text{V}$ (Max.)
- Pin and function compatible with 74HC374

(Note) The JEDEC SOP (FW) is not available in Japan.

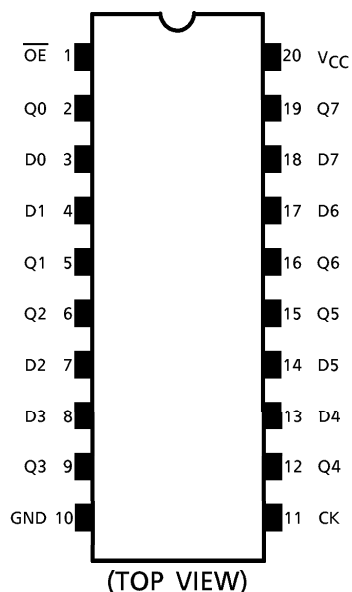


Weight	
SOP20-P-300-1.27	: 0.22g (Typ.)
SOL20-P-300-1.27	: 0.46g (Typ.)
TSSOP20-P-0044-0.65	: 0.08g (Typ.)

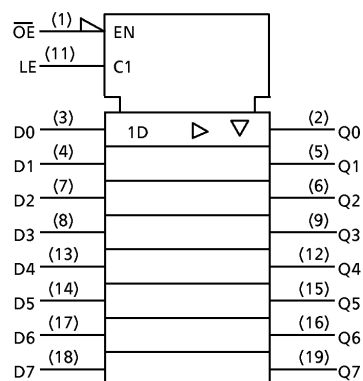
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PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

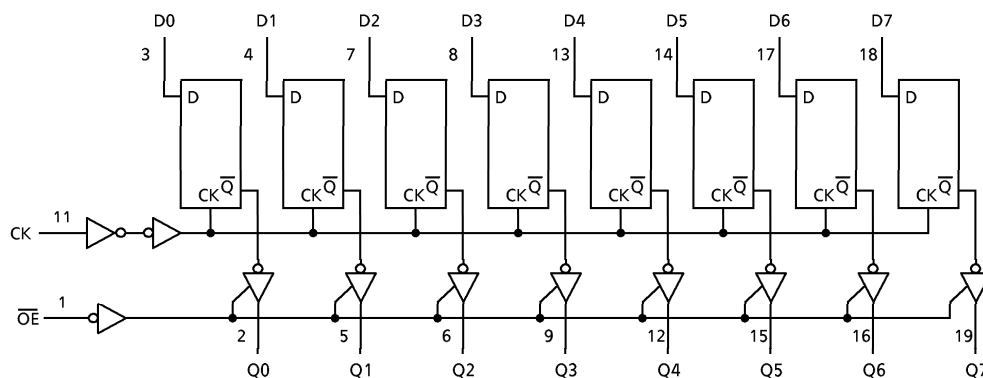
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

X : Don't Care

Z : High Impedance

Qn : No Change

SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM- BOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	“H” Level	V _{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	“L” Level	V _{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH}	I _{OH} = - 50μA	2.0	1.9	2.0	—	1.9	—	V
			or V _{IL}	I _{OH} = - 50μA	3.0	2.9	3.0	—	2.9	—	
				I _{OH} = - 4mA	3.0	2.58	—	—	2.48	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
			or V _{IL}	I _{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
3-state Output Off-state Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		3.6	—	—	± 0.25	—	± 2.5	μA
Input Leakage Current		I _{IN}	V _{IN} = 5.5V or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C	UNIT
			V _{CC} (V)	LIMIT		
Minimum Pulse Width (CK)	t_W (H) t_W (L)		2.7	7.5	8.0	ns
			3.3 ± 0.3	5.0	5.5	
Minimum Set-up Time	t_s		2.7	6.5	6.5	ns
			3.3 ± 0.3	4.5	4.5	
Minimum Hold Time	t_h		2.7	2.0	2.0	ns
			3.3 ± 0.3	2.0	2.0	

AC characteristics (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		2.7	15	—	8.5	16.3	ns
				50	—	11.0	19.8	
			3.3 ± 0.3	15	—	6.7	10.6	
				50	—	9.2	14.1	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	2.7	15	—	7.6	14.5	ns
				50	—	10.1	18.0	
			3.3 ± 0.3	15	—	5.9	9.3	
				50	—	8.4	12.8	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	2.7	50	—	11.5	18.5	ns
			3.3 ± 0.3	50	—	9.6	13.2	
Maximum Clock Frequency	f_{MAX}		2.7	15	60	115	—	ns
				50	45	60	—	
			3.3 ± 0.3	15	100	160	—	
				50	60	95	—	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	
Input Capacitance	C_{IN}	(Note 2)	—			4	10	pF
Output Capacitance	C_{OUT}		—			6	—	pF
Power Dissipation Capacitance	C_{pD}	(Note 3)	—			32	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{pD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{pD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

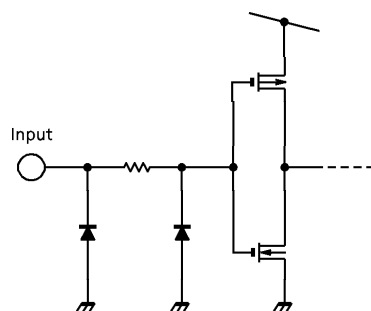
And the total C_{pD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{pD}(\text{total}) = 20 + 12 \cdot n$$

Noise characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$)

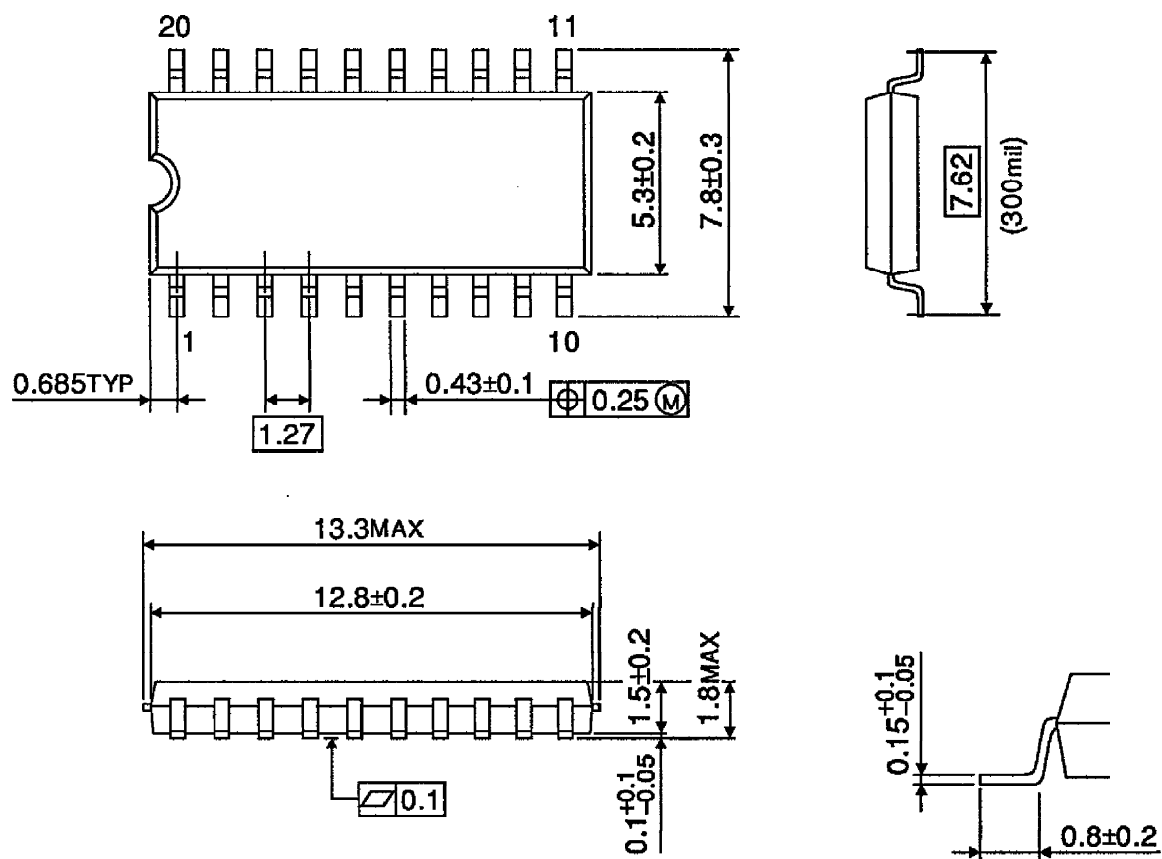
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP20-P-300-1.27

Unit : mm

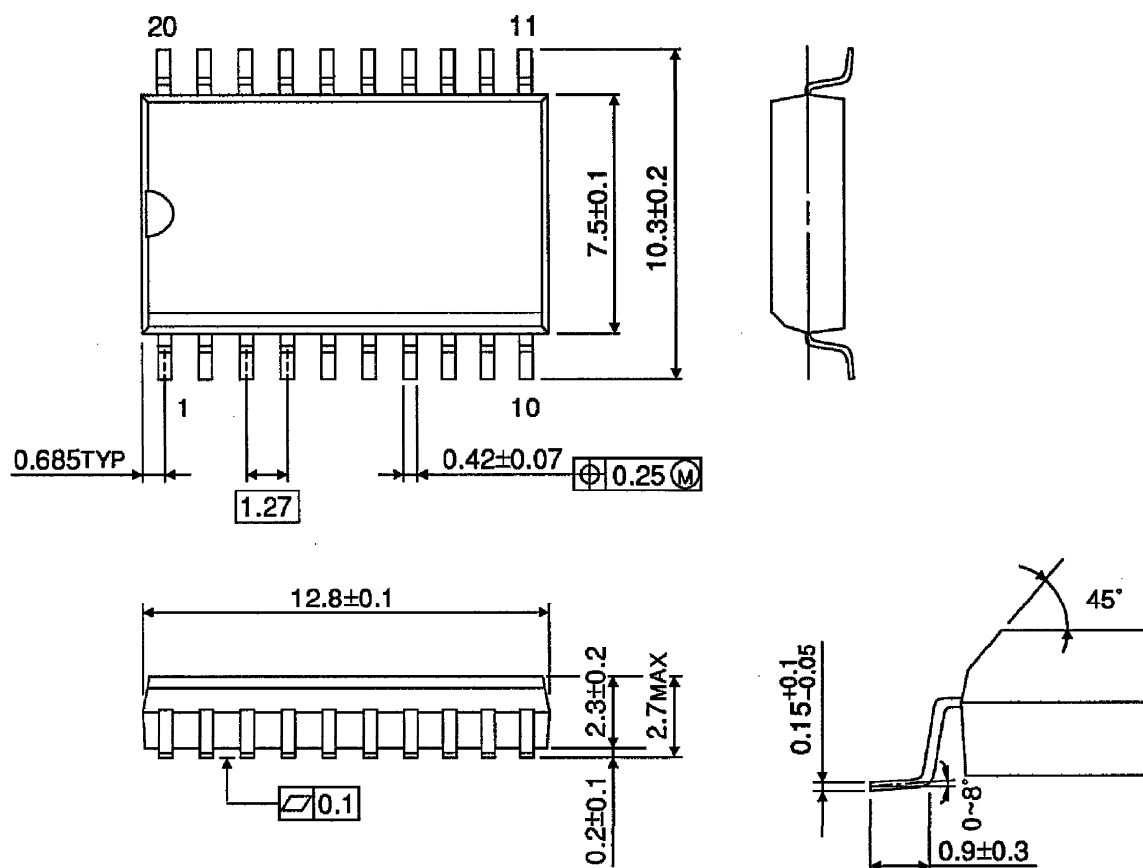


Weight : 0.22g (Typ.)

OUTLINE DRAWING
SOL20-P-300-1.27

Unit : mm

(Note) This package is not available in Japan.

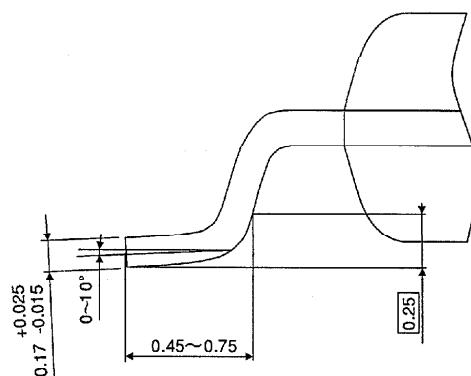
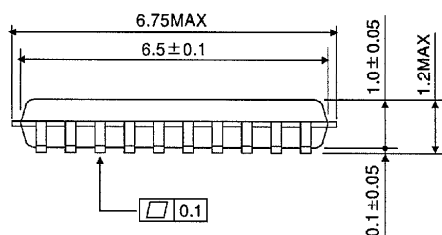
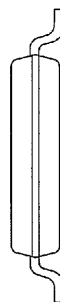
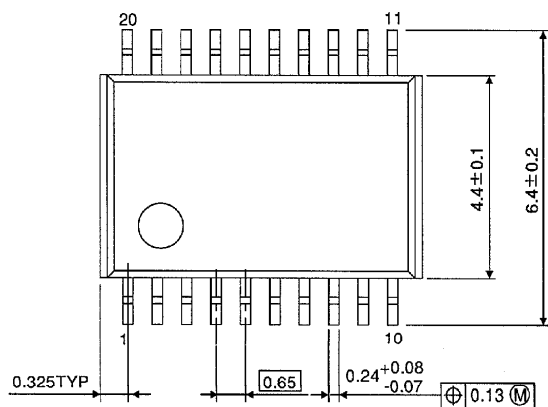


Weight : 0.46g (Typ.)

OUTLINE DRAWING

TSSOP20-P-0044-0.65

Unit : mm



Weight : 0.08g (Typ.)