

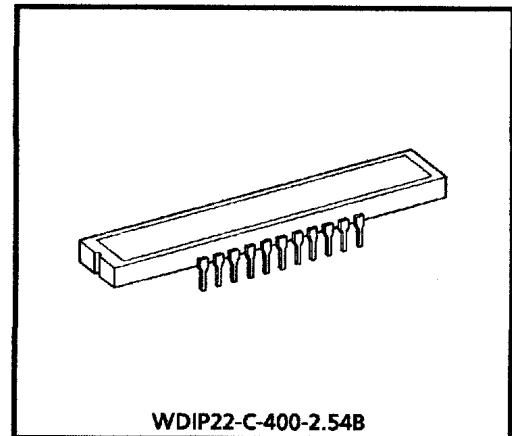
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD1500C

The TCD1500C is a high sensitive and low dark current 5340-elements linear image sensor. The sensor can be used for facsimile, imagescanner and OCR. The signal pre-processing circuit which is composed of Sample and Hold circuit and Pre-amplifier circuit. The device contains a row of 5340 photodiodes, which provide a 16 lines/mm (400DPI) across a A3 size paper and besides 24 lines/mm (600DPI) across a A4 size paper.

FEATURES

- Number of Image Sensing Elements : 5340
- Image Sensing Element Size : 7 μ m by 7 μ m on 7 μ m centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 2 phase
- Internal Circuit : S/H circuit, Pre-Amplifier circuit
- Package : 22 pin cerdip



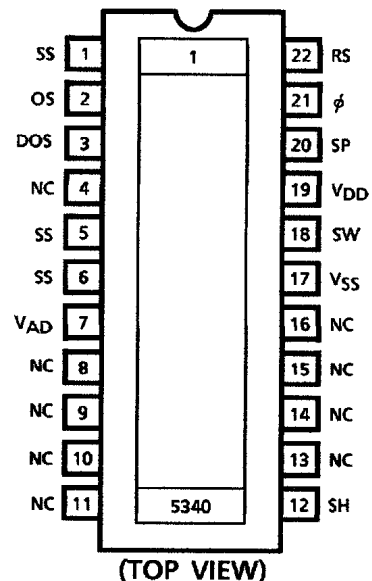
Weight : 5.4g (Typ.)

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V ϕ	-0.3~15	V
Shift Pulse Voltage	V _{SH}		V
Reset Pulse Voltage	V _{RS}		V
Sample and Hold Pulse Voltage	V _{SP}		V
Power Supply Voltage (Analog)	V _{AD}		V
Power Supply Voltage (Driver)	V _{DD}		V
Operating Temperature	T _{opr}		-25~60
Storage Temperature	T _{stg}	-40~100	°C

(Note 1) All voltage are with respect to SS and V_{SS} terminals (Ground).

PIN CONNECTIONS

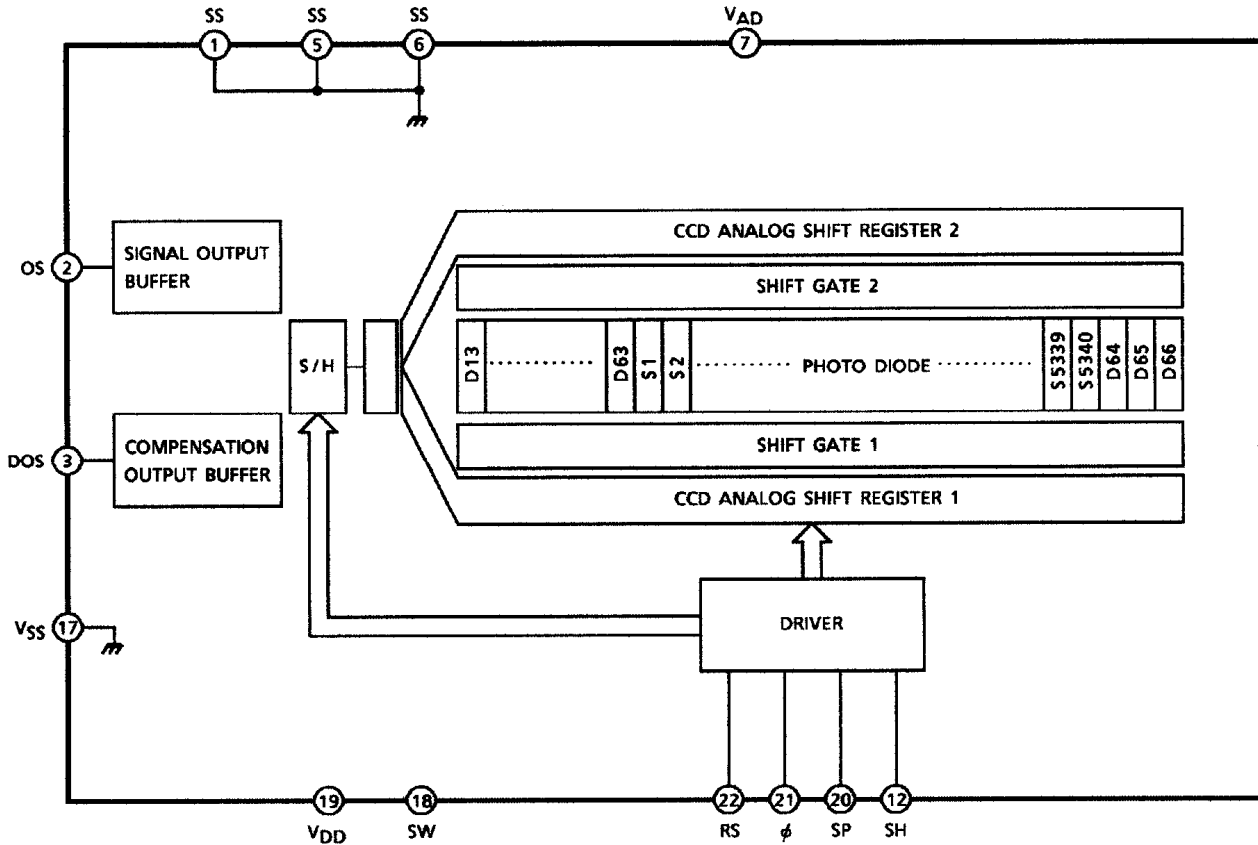


(TOP VIEW)

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

CIRCUIT DIAGRAM



PIN NAMES

ϕ	Clock
SH	Shift Gate
RS	Reset Gate
SP	Sample Hold Gate
OS	Signal Output
DOS	Compensation Output
VAD	Power (Analog)
VDD	Power (Driver)
SS	Ground (Analog)
VSS	Ground (Driver)
SW	Final Clock Select Switch
NC	Non Connection

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, VAD = 12V, VDD = 12V, Vφ = VSH = VRS = 5V (PULSE), fφ = 0.5MHz, fRS = 1MHz,
tINT (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	3.8	4.8	5.8	V/lx-s	
Photo Response Non Uniformity	PRNU	—	—	10	%	(Note 2)
	PRNU (3)	—	3	8	mV	(Note 3)
Register Imbalance	RI	—	—	3	%	(Note 4)
Saturation Output Voltage	VSAT	1.0	1.5	—	V	(Note 5)
Saturation Exposure	SE	0.17	0.3	—	lx-s	(Note 6)
Dark Signal Voltage	VDRK	—	—	2	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	—	—	3	mV	(Note 7)
Analog Current Dissipation	IAD	—	—	20	mA	
Driver Current Dissipation	IDD	—	—	10	mA	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	ZO	—	0.5	1	kΩ	
Dynamic Range	DR	—	1500	—		(Note 8)
DC Signal Output Voltage	VOS	3.5	4.5	6.0	V	(Note 9)
DC Compensation Output Voltage	VDOS	3.5	4.5	6.0	V	(Note 9)
DC Mismatch Voltage	VOS-VDOS	—	—	100	mV	

(Note 2) Measured at 50% of SE (Typ.)

$$\text{Definition of PRNU : PRNU} = \frac{\Delta\bar{x}}{\bar{x}} \times 100 (\%)$$

Where \bar{x} is average of total signal outputs and $\Delta\bar{x}$ is the maximum deviation from \bar{x} under uniform illumination.

(Note 3) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.)

(Note 4) Measured at 50% of SE (Typ.)

RI is defined as follows:

$$RI = \frac{\sum_{n=1}^{5339} |x_n - x_{n+1}|}{5339 \times \bar{x}} \times 100 (\%)$$

Where x_n and x_{n+1} are signal outputs of each pixel. \bar{x} is average of total signal outputs.

(Note 5) VSAT is defined as minimum saturation output voltage of all effective pixels.

(Note 6) Definition of SE : $SE = \frac{VSAT}{R}$ (lx-s)

OPERATING CONDITION

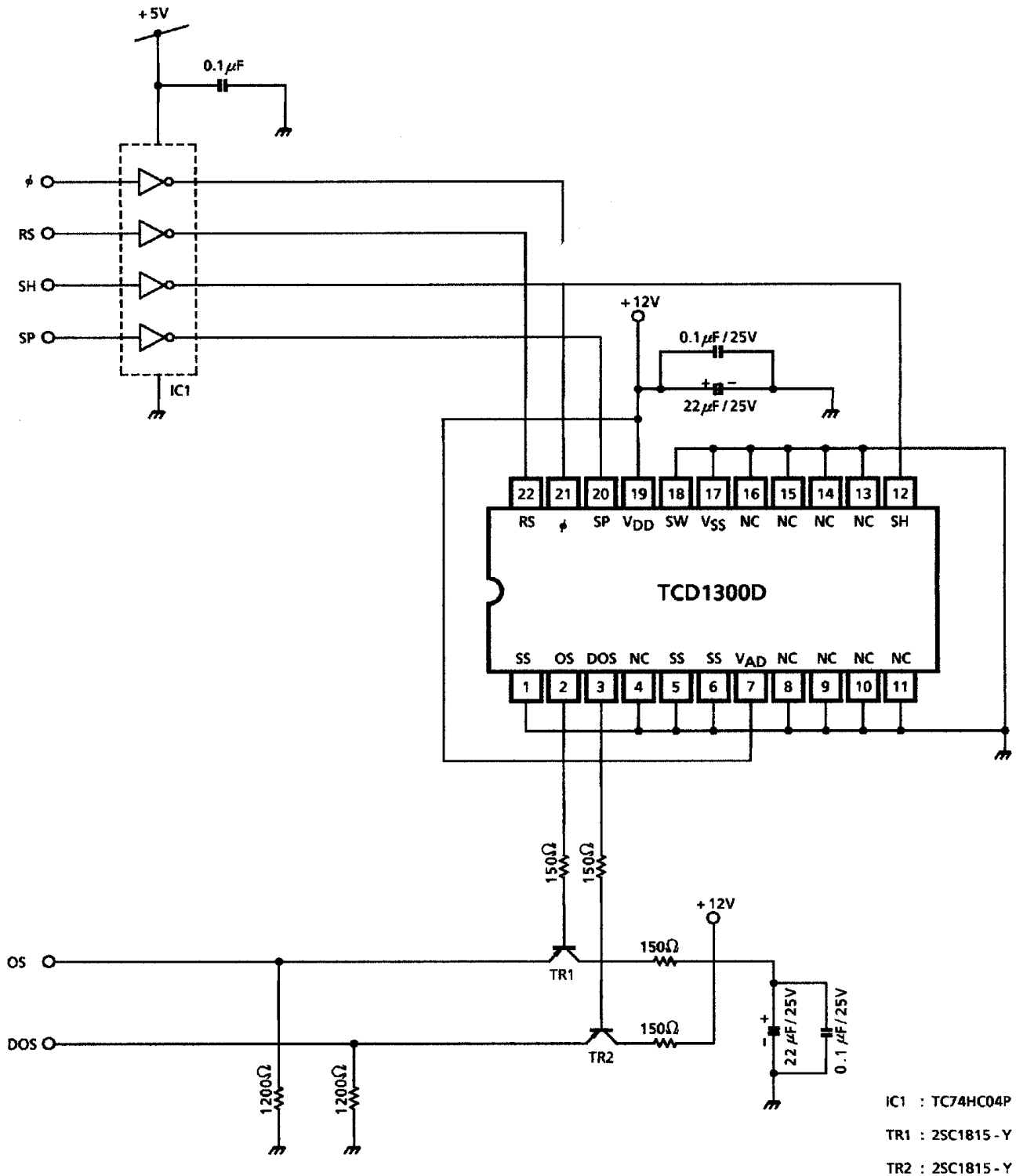
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	V_{ϕ}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Shift Pulse Voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Reset Pulse Voltage	"H" Level	V_{RS}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Sample and Hold Pulse Voltage (Note 9)	"H" Level	V_{SP}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Switch Voltage	"H" Level	V_{SW}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Power Supply Voltage (Analog)		V_{AD}	11.4	12	13	V
Power Supply Voltage ((Driver)		V_{DD}	11	12	13	V

(Note 9) Supply "H" level to SP terminal when sample-and-hold circuitry is not used.

CLOCK CHARACTERISTICS (Ta = 25°C)

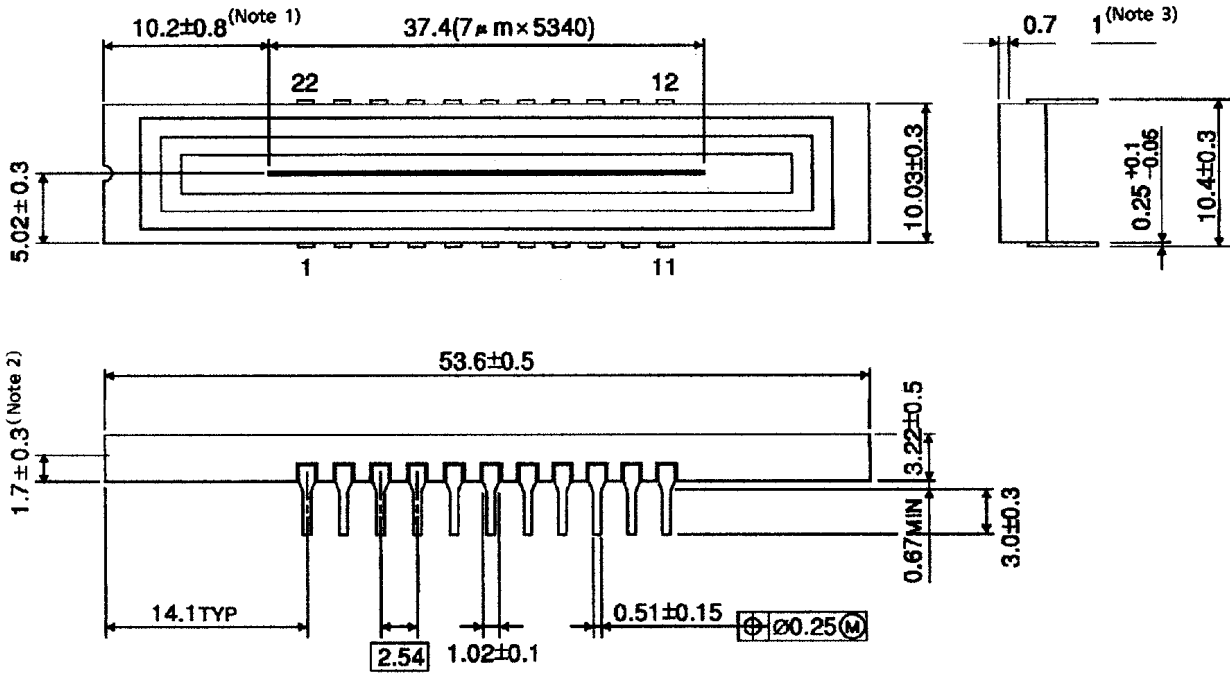
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	—	0.5	4.0	MHz
Reset Pulse Frequency	f_{RS}	—	1	8.0	MHz
Sample and Hold Pulse Frequency	f_{SP}	—	1	8.0	MHz
Clock Capacitance	C_{ϕ}	—	—	10	pF
Final Stage Clock Capacitance	C_{ϕ}	—	—	10	pF
Shift Gate Capacitance	C_{SH}	—	—	10	pF
Sample and Hold Gate Capacitance	C_{SP}	—	—	10	pF
Switch Capacitance	C_{SW}	—	—	10	pF

TYPICAL DRIVE CIRCUIT



OUTLINE DRAWING
WDIP22-C-400-2.54B (C)

Unit : mm



- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)

Weight : 5.4g (Typ.)