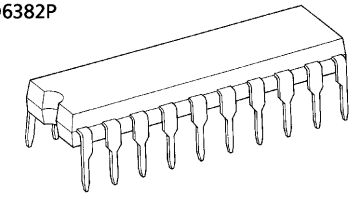
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD6380P, TD6380N, TD6380Z, TD6381P, TD6381N, TD6381Z, TD6382P, TD6382N, TD6382Z

FREQUENCY SYNTHESIZER FOR TV / CATV

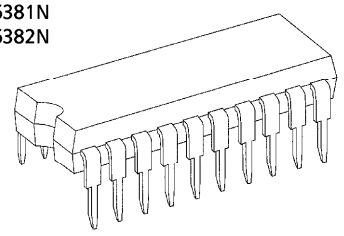
A series of TD6380~6382 are a single-chip frequency synthesizer IC, which can configure high-performance frequency synthesizer systems in combination with a 4bit μCPU controller.
This IC integrates high input sensitivity ECL prescaler, I^2L programmable counter, PLL logic and bandswitch drive decoder in a small package.

TD6380P
TD6381P
TD6382P



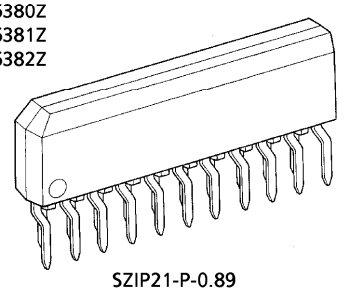
DIP20-P-300-2.54A

TD6380N
TD6381N
TD6382N



SDIP20-P-300-1.78

TD6380Z
TD6381Z
TD6382Z



SZIP21-P-0.89

FEATURES

- High input sensitivity
  f_{in} = 80~100MHz : – 20dBmW (50Ω) (Min.)
  f_{in} = 0.1~1GHz : – 27dBmW (50Ω) (Min.)
  f_{in} = 1~1.2GHz : – 17dBmW (50Ω) (Min.) (TD6381 only)
- Simple control bus : 18 / 19bit serial input
- 5V single power supply operation
- Bandswitch driver : 4 channels
- The frequency step will be as follows :

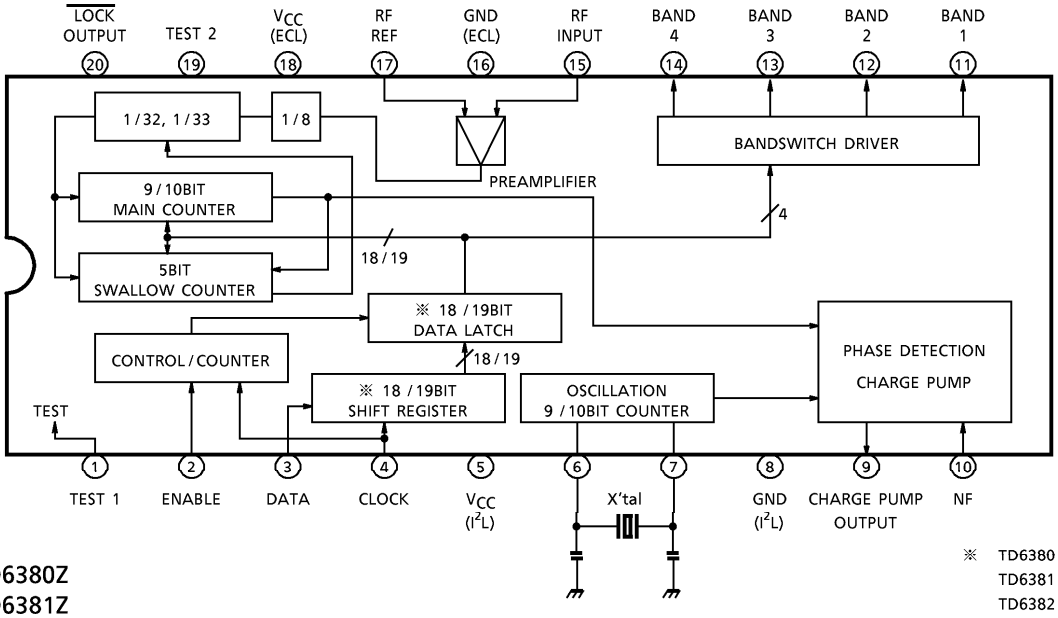
IC	CRYSTAL	STEP	MAX. OPERATING FREQUENCY
6380	4.0 MHz	62.5 kHz	1.0 GHz
6381	3.2 MHz	50 kHz	1.2 GHz
6382	4.0 MHz	31.25 kHz	1.0 GHz

(Note) Handle with care as this product is weak at surge voltage.

Weight
DIP20-P-300-2.54A : 2.25g (Typ.)
SDIP20-P-300-1.78 : 1.02g (Typ.)
SZIP21-P-0.89 : 1.00g (Typ.)

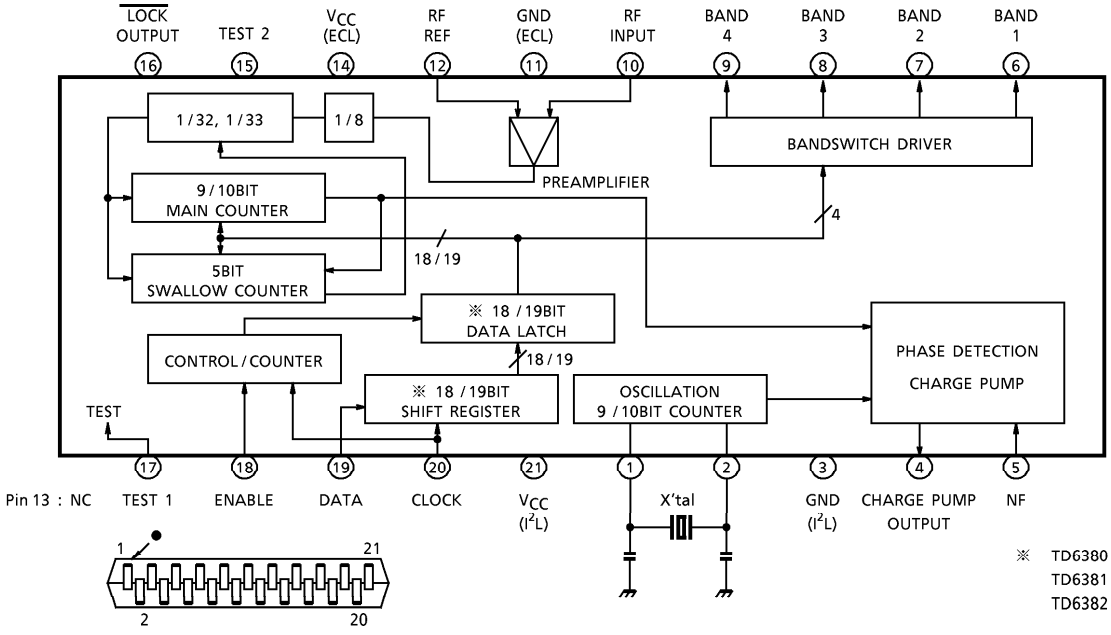
BLOCK DIAGRAM

TD6380P / N
TD6381P / N
TD6382P / N



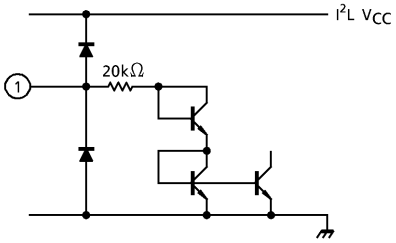
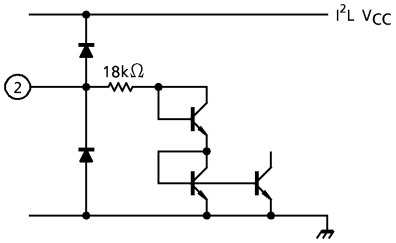
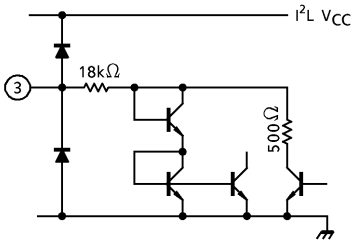
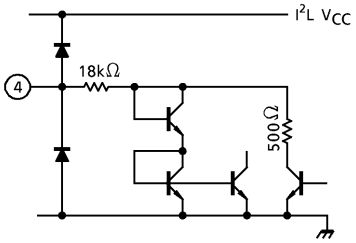
※ TD6380 : 18BIT
TD6381 : 19BIT
TD6382 : 19BIT

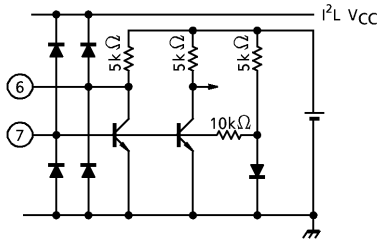
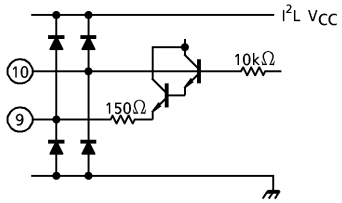
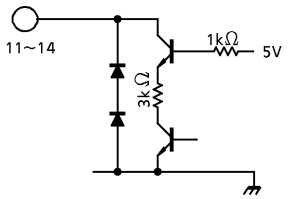
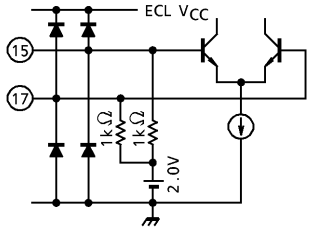
TD6380Z
TD6381Z
TD6382Z



※ TD6380 : 18BIT
TD6381 : 19BIT
TD6382 : 19BIT

TERMINAL FUNCTION (The pin no is indicated in the case of P-package.)

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Test Pin 1	Low level : this will be in normal use operation mode when connected to GND or open. In order to prevent a static breakdown, it will be more effective to connect to GND. High level : this will be in test mode when connected to V_{CC}.	
2	Enable Input	This is an enable pulse input terminal at normal use operation. This will be a test mode select terminal of test mode by means of the pin 1 mode select pin. In order to prevent a static breakdown, it will be effective to connect in series a resistor of about 1kΩ. The pins 3 and 4 below are the same as this pin.	
3	Data Input	This is a data input terminal in normal mode. In test mode 1 or 2, this will be a main counter output terminal. In test mode 3, this can be an external input terminal of comparison signal of phase comparator (a counter output terminal in normal mode).	
4	Clock Input	This is a clock pulse input terminal in normal mode. In test mode 1 or 2, this will be an output terminal of reference signal whose crystal oscillator is divided by 2^9 or 2^{10}. In test mode 3, this can be an input terminal of external reference signal.	
5	Logic V_{CC}	This is logic circuit power supply. Connect a bypass capacitor between this pin and pin 8.	—

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
6, 7	Crystal Oscillation	This is a crystal oscillation terminal to make the reference signal. Make sure to use the logic GND of pin 8 as this oscillates in a big amplitude (about 800mV$_{p-p}$).	
8	Logic GND	This is used for crystal oscillator GND as is logic GND. Never wire this pin close to the high frequency GND of pin 16.	—
9 10	Frequency phase Comparator Output	In normal use, this compares a high frequency wave input with frequency data and feeds back its difference by means of the supply pump.	
11 ~ 14	Bandswitch	This can make the 4 band switching operate independently. The external driver can freely be operated anywhere between 1~4 pins. Connect an unused pin to the bandswitch power supply.	
15 17	Reference bias by RF Input	This is an input terminal of local oscillation of tuner. In order to prevent disturbance or unwanted resonance, use the pattern of short distance or lead wire for pin 15. Also, connect a bypass capacitor to pin 16 for pin 17 as well.	
16	High Frequency GND	This is mainly used for a bypass capacitor of pins 17 and 18 as is high frequency GND. Also the pattern should be laid out so as to be separated from the logic GND of pin 8.	—

RECOMMENDED SUPPLY VOLTAGE
(The pin no. is indicated in the case of P-package.)

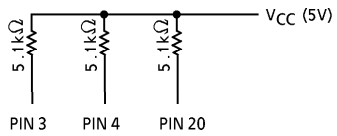
PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
5	ECL V_{CC}	4.5	5	5.5	V
18	I^2L V_{CC}	4.5	5	5.5	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C)

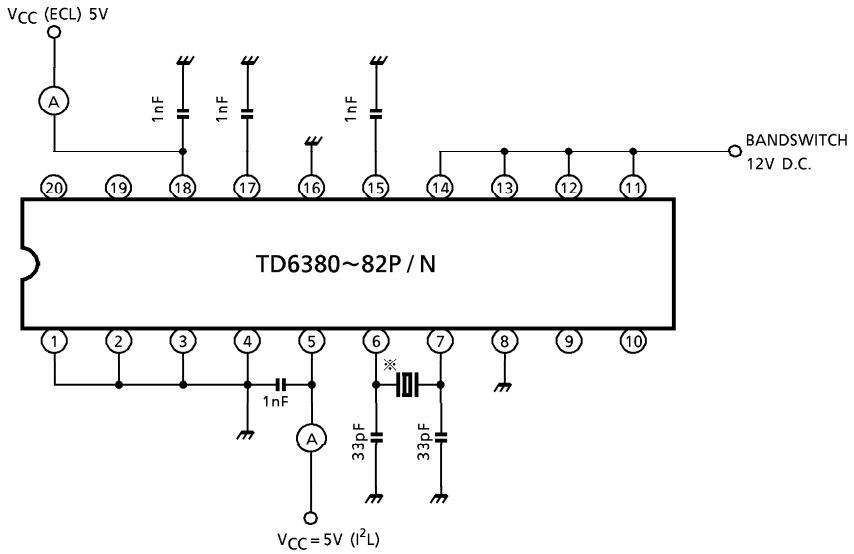
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	(ECL)	I_{CC1}	—		14	40	66	mA
	(I^2L)	I_{CC2}	—		6	13	20	
Bandswitch Max. Voltage		V_B MAX.	—	Band 1~4	12	—	15	V
DC Voltage		V_{15}	—	—	1.7	2.0	2.3	V
		V_{17}	—	—	1.7	2.0	2.3	
DC Current High Level		I_{IH}	—	V_{in} = 5V (Note 1)	—	180	300	μA
Input Voltage	"H" Level	V_{IH}	—	(Note 1)	3.0	—	—	V
	"L" Level	V_{IL}	—		—	—	0.8	
Input Voltage	"H" Level	V_{OH}	1	(Note 2)	3.8	—	—	V
	"L" Level	V_{OL}	1		—	—	0.5	
N/F Leak Current		I_L	—	(Note 3)	−0.2	—	0.2	μA
RF Input Sensitivity		V_{in1}	3	f_{in} = 80-100MHz	−20	—	3	dBmW (50Ω)
		V_{in2}	3	f_{in} = 100-1000MHz	−27	—	3	
		V_{in3}	3	f_{in} = 1~1.2GHz	−17	—	3	
Setup Time		T_S	—	Data timing chart	2	—	—	μs
Enable Hold Time		T_{SL}	—		2	—	—	
Enable Inhibit Time		T_{NE}	—		6	—	—	
Clock Inhibit Time		T_{NC}	—		6	—	—	
Clock Width		T_C	—		2	—	—	
Enable Setup Time		T_L	—		10	—	—	
Data Hold Time		T_H	—		2	—	—	

(Note 1) TEST1, Enable, Clock, $\overline{\text{Lock}}$: applied to input mode.
(Note 2) Data, Clock, $\overline{\text{Lock}}$: applied to output mode.
(Note 3) Pin 10 : 2.1V, Pin 9 : Open

TEST CIRCUIT 1
Test Mode (The pin no. is indicated in the case of P-package.)



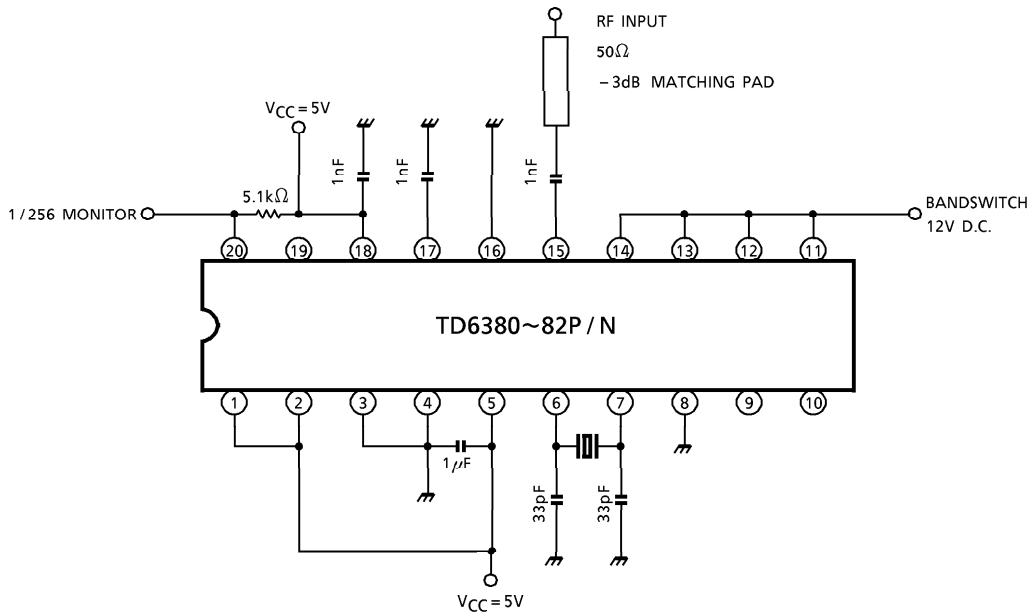
TEST CIRCUIT 2
Supply test circuit



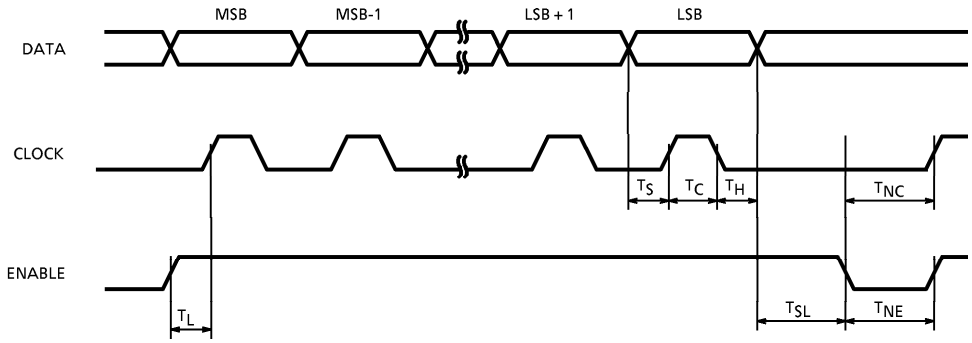
※ Crystal oscillator specification

TD6380	:	4.0MHz	Serial resistance	:	Below 100Ω
TD6381	:	3.2MHz	Parallel capacitance	:	16pF ± 1pF
TD6382	:	4.0MHz	Frequency tolerance	:	Within ± 25ppm
			Temperature tolerance	:	Within ± 30ppm (Ta = – 20~75°C)

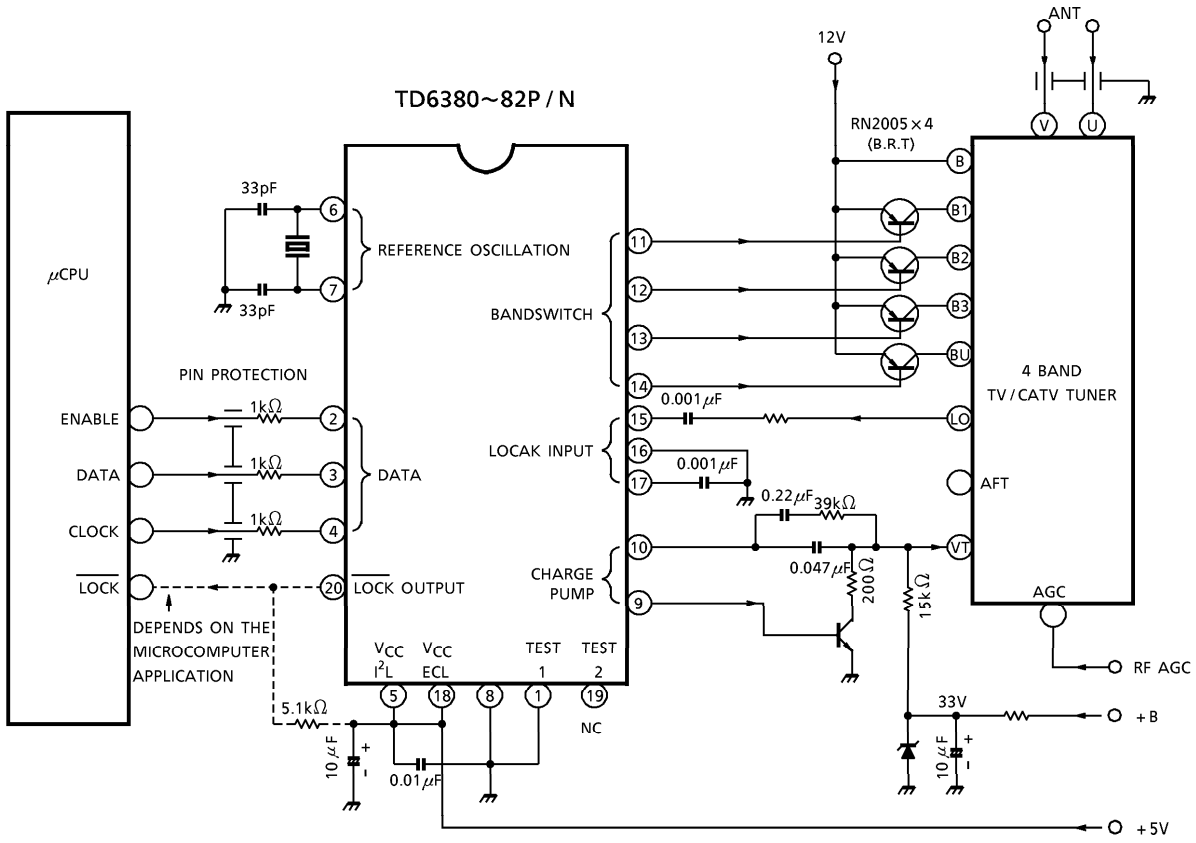
TEST CIRCUIT 3
Input Sensitivity Test Circuit



DATA TIMING CHART (Rising timing)



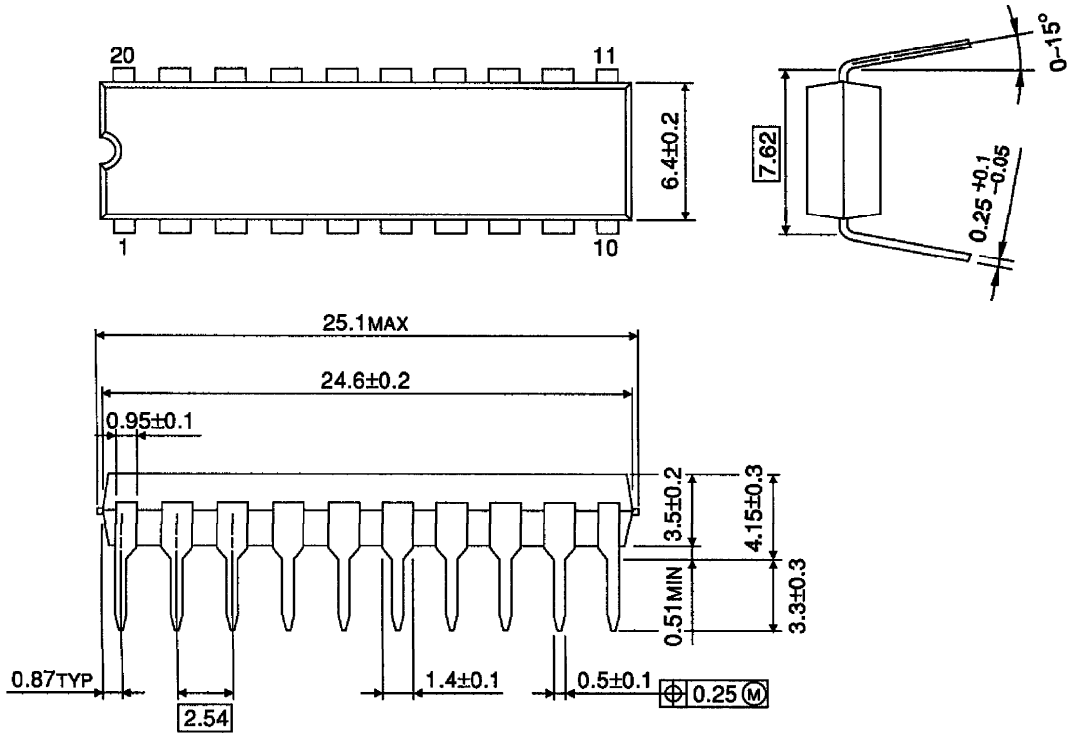
APPLICATION CIRCUIT EXAMPLE OF FREQUENCY SYNTHESIZER



OUTLINE DRAWING

DIP20-P-300-2.54A

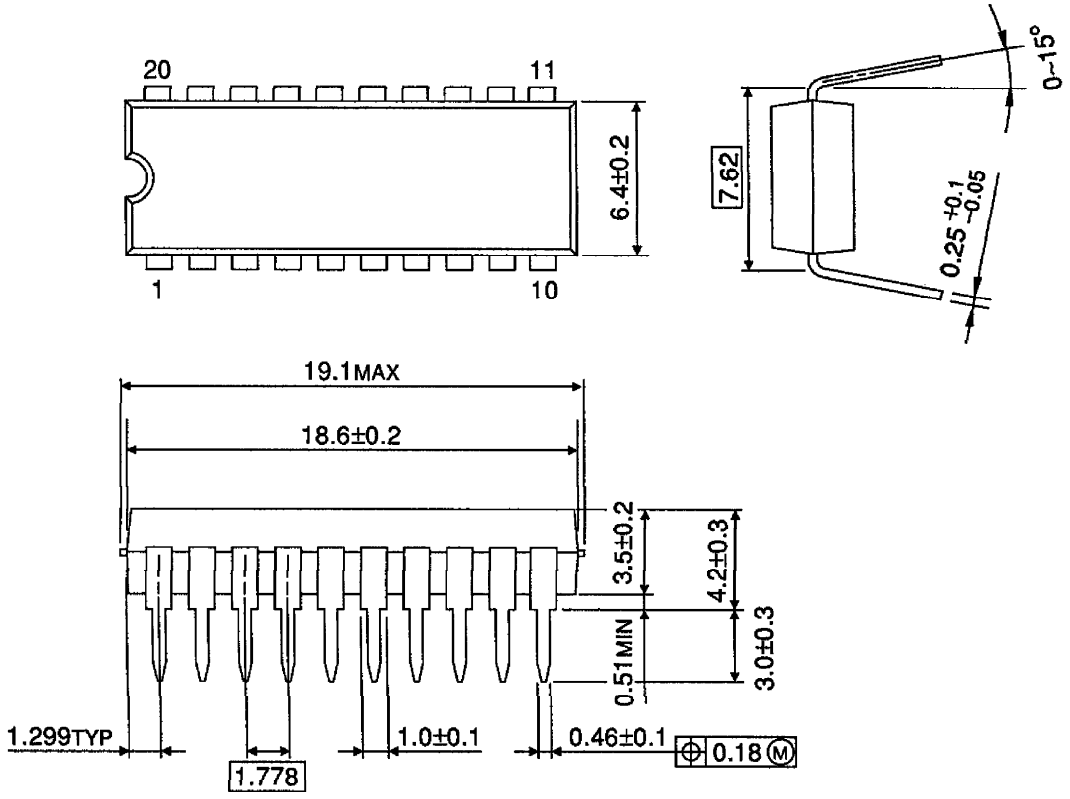
Unit : mm



Weight : 2.25g (Typ.)

OUTLINE DRAWING

SDIP20-P-300-1.78 Unit : mm

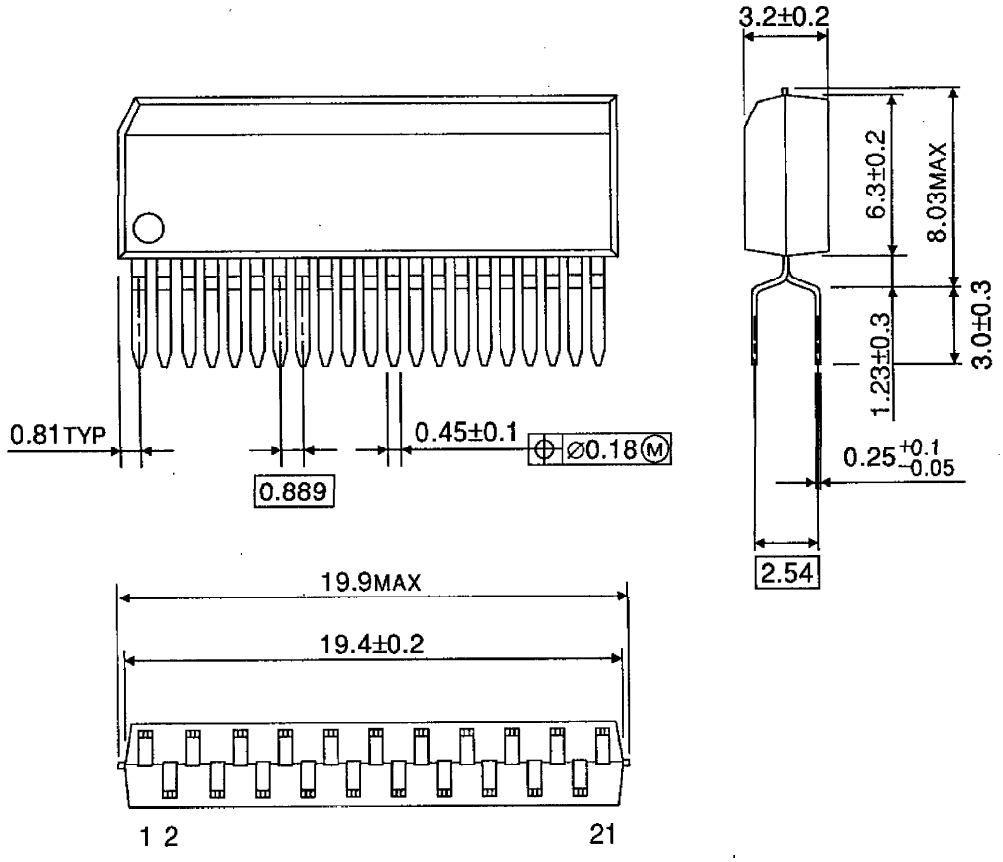


Weight : 1.02g (Typ.)

OUTLINE DRAWING

SZIP21-P-0.89

Unit : mm



Weight : 1.00g (Typ.)