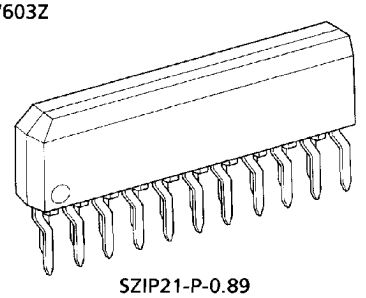
TENTATIVE TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD7603Z, TD7603F

FREQUENCY SYNTHESIZERS FOR TV / CATV

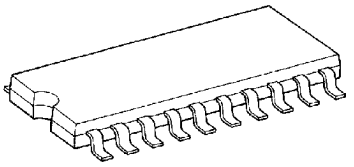
The TD7603Z, TD7603F is a single-chip frequency synthesizer IC, which can configure high-performance frequency synthesizer systems in combination with a μCPU controller.
This IC integrates high input sensitivity ECL prescaler, I^2L programmable counter, PLL logic and bandswitch drive decoder in a small package.

TD7603Z



SZIP21-P-0.89

TD7603F



SOP20-P-300-1.27

Weight
SZIP21-P-0.89 : 1.00g (Typ.)
SOP20-P-300-1.27 : 0.25g (Typ.)

FEATURES

- High-sensitivity input

  f_{in} = 80~100MHz : – 20dBmW (50Ω) (Min.)
  f_{in} = 0.1~1GHz : – 27dBmW (50Ω) (Min.)
  f_{in} = 1~1.3GHz : – 17dBmW (50Ω) (Min.)

- 5V single power supply operation.
- Wide operating frequency range : 1.3GHz
- Simple control bus line : I^2C bus
- Bandswitch driver : 4 channels
- The frequency step, maximum operating frequency will be as follows.

CRYSTAL OSCILLATOR FREQUENCY	FREQUENCY STEP	MAXIMUM OPERATING
4.0MHz	62.5kHz	1.3GHz
3.2MHz	50kHz	1.3GHz
4.0MHz	31.25kHz	1.0GHz

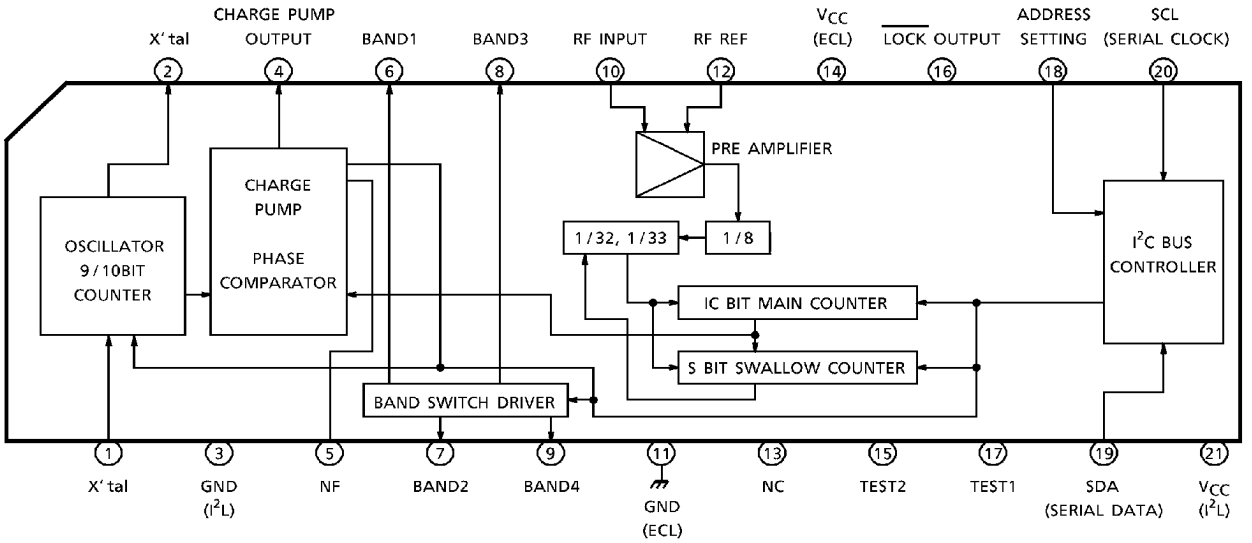
- The data power-on reset function.

(Note) These devices are easy to be damaged by high static voltage or electric fields.
In regards to this, please handle with care.

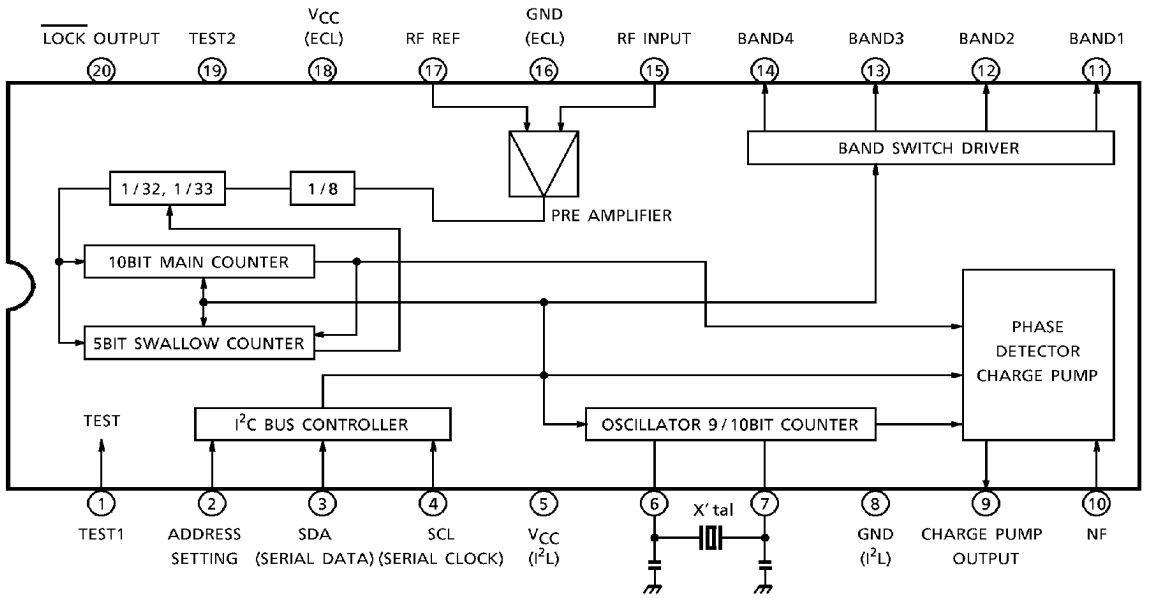
961001EBA1

BLOCK DIAGRAM

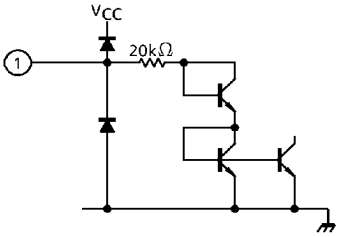
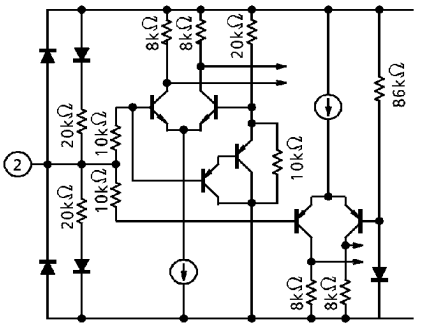
TD7603Z

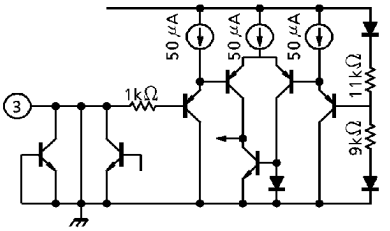
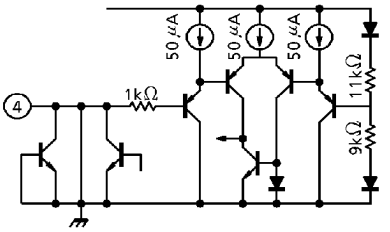
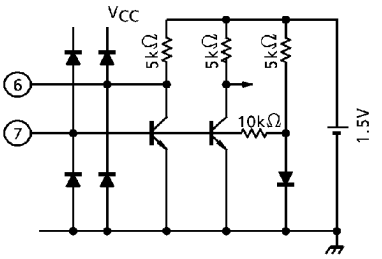


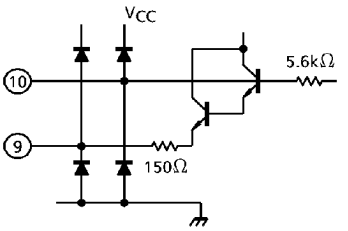
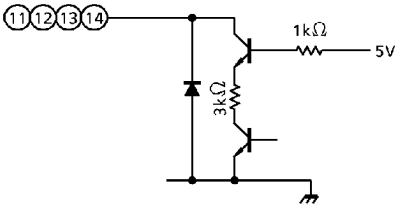
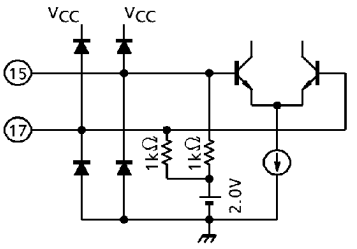
TD7603F

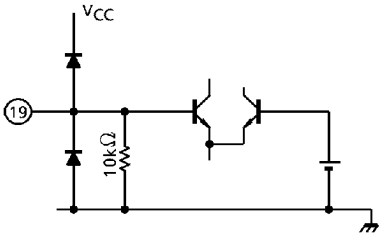
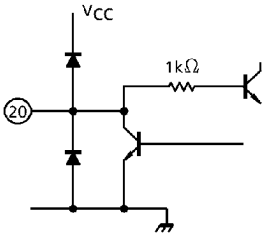


PIN FUNCTIONS
(Pin numbers is indicated in the case of TD7603F flat package)

<table>
<tr><th>PIN No.</th><th>PIN NAME</th><th>FUNCTION</th><th>INTERNAL CIRCUIT</th></tr>
<tr><td>1</td><td>Test Pin 1</td><td>This pin switches between NORMAL and TEST modes.
<table><tr><th>VOLTAGE FOR THIS PIN</th><th>MODE</th></tr><tr><td>GND (Or Low Level)</td><td>Operating Mode for normal use</td></tr><tr><td>V_{CC} (Or High Level)</td><td>TEST Mode</td></tr></table>Operating (NORMAL) mode can be selected even if this pin is left open.
However, we recommend connecting this pin to one level or the other.</td><td> 
</td></tr>
<tr><td>2</td><td>Address Setting Pin</td><td>The Function of this pin varies according to the setting of pin 1.
The following table shows the details.
<table><tr><th>PIN 1 SETTING</th><th>FUNCTION OF THIS PIN</th></tr><tr><td>NORMAL Mode</td><td>Sets the subaddress</td></tr><tr><td>TEST Mode</td><td>Selects TEST1, TEST2, or TEST3</td></tr></table>The DC voltage supplied to this pin sets the subaddress.
<table><tr><th>DC VOLTAGE TO THIS PIN</th><th colspan="2">SUBADDRESS SETTING</th></tr><tr><td>0~0.5V</td><td>0</td><td>1</td></tr><tr><td>2.0~3.0V (Or Open)</td><td>1</td><td>0</td></tr><tr><td>4.5~5.0V</td><td>1</td><td>1</td></tr><tr><td>0~5.0V</td><td>0</td><td>1</td></tr></table>The DC voltage supplied to this pin performs the TEST switching.
<table><tr><th>VOLTAGE TO THIS PIN</th><th>TEST SWITCHING</th></tr><tr><td>Low Level</td><td>TEST1</td></tr><tr><td>Low Level</td><td>TEST2</td></tr><tr><td>High Level</td><td>TEST3</td></tr></table></td><td> 
</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>PIN NAME</th><th>FUNCTION</th><th>INTERNAL CIRCUIT</th></tr>
<tr><td>3</td><td>Serial Data Input Pin</td><td>The Function of this pin varies according to the setting of pin 1. The following table shows the details.
<table>
<tr><th colspan="2">SETTING OF PIN 1</th><th>FUNCTION OF THIS PIN</th></tr>
<tr><td colspan="2">NORMAL Mode</td><td>Serial data input pin</td></tr>
<tr><td rowspan="3">TEST Modes</td><td>TEST1</td><td>Main counter output pin</td></tr>
<tr><td>TEST2</td><td>Same as TEST1</td></tr>
<tr><td>TEST3</td><td>Input pin for external phase comparator compare signal</td></tr>
</table>
When this pin is used for serial data input, the characteristics of the pin are as follows :
The input level threshold voltage is approximately 2.3V. The maximum current output from this pin is around 50μA.</td><td> 
</td></tr>
<tr><td>4</td><td>Serial Clock Input Pin</td><td>The function of this pin varies according to the setting of pin 1. The following table show the details.
<table>
<tr><th colspan="2">SETTING OF PIN 1</th><th>FUNCTION OF THIS PIN</th></tr>
<tr><td colspan="2">NORMAL Mode</td><td>Serial clock pulse input pin</td></tr>
<tr><td rowspan="3">TEST Modes</td><td>TEST1</td><td>Reference signal (Crystal oscillator output divided by $2^9 = 512$) output pin</td></tr>
<tr><td>TEST2</td><td>Same as TEST1</td></tr>
<tr><td>TEST3</td><td>Input pin for external phase comparator reference signal</td></tr>
</table></td><td> 
</td></tr>
<tr><td>5</td><td>Logic System V_{CC} Pin</td><td>Logic circuit power supply pin.
Supply 5V ± 0.5V to this pin from an external source. Connect a bypass capacitor between this pin and pin 8.</td><td>—</td></tr>
<tr><td>6
7</td><td>Crystal Oscillator Pins</td><td>These pins connect the crystal oscillator to generate the reference signal. The signal from the pins has a large amplitude (around 800mV_{p-p}). Therefore, be sure to use pin 8 as the crystal oscillator GND. If pin 16 is inadvertently used as the crystal oscillator GND, high-frequency circuitry may malfunction.</td><td> 
</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>PIN NAME</th><th>FUNCTION</th><th>INTERNAL CIRCUIT</th></tr>
<tr><td>8</td><td>Logic System GND</td><td>This is the logic circuit GND pin. Connect a bypass capacitor between this pin and pin 5. Be sure to electrically isolate the circuit where this pin is connected and the circuit where pin 16 is connected.</td><td>—</td></tr>
<tr><td>9
10</td><td>Frequency / Phase Comparator Output Pins</td><td>The function of these pins varies according to the setting of pin 1. The following table shows the details.
<table>
<tr><th colspan="2">SETTING OF PIN 1</th><th>FUNCTION OF THESE PINS</th></tr>
<tr><td colspan="2">NORMAL Mode</td><td>Frequency / phase comparator output pin</td></tr>
<tr><td rowspan="3">TEST Modes</td><td>TEST1</td><td>—</td></tr>
<tr><td>TEST2</td><td>—</td></tr>
<tr><td>TEST3</td><td>Checks operation of phase comparator.</td></tr>
</table>
The frequency / phase comparator output is the result of comparing the frequency and phase of the reference signal and the high-frequency input signal. The result is supplied to the current pump circuit as the error signal. Pin 9 supplies the output of the current pump circuit to the tuner.</td><td> 
</td></tr>
<tr><td>11
12
13
14</td><td>Band Switching Pins</td><td>These pins output the bad switch signal to the band switch driver. The operation of the driver switches the tuner reception band. Any of the drivers can be activated independently (separately). Connect pins not in use to the band switching power supply line.</td><td> 
</td></tr>
<tr><td>15
17</td><td>RF Deferential Input Reference Bias Pin 17, Local Oscillator (built into tuner) Input Pin 15</td><td>To stop interference from unnecessary external signals via pin 15, and to prevent unnecessary oscillation related to pin 15, make the circuit pattern or wiring connected to pin 15 as short as possible. This also applies to pin 17. In addition, connect a bypass capacitor between pins 17 and 16.</td><td> 
</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>PIN NAME</th><th>FUNCTION</th><th>INTERNAL CIRCUIT</th></tr>
<tr><td>16</td><td>High-frequency System GND Pin</td><td>This is the ground pin for high-frequency circuits. Connect one bypass capacitor between this pin and pin 17, and another between this pin and pin 18. Electrically isolate the GND circuit of this pin and the GND circuit of pin 8.</td><td>—</td></tr>
<tr><td>18</td><td>High-frequency System V_{CC}</td><td>This is the high-frequency circuit power supply pin. Supply 5V ± 0.5V to this pin from an external source. Connect a bypass capacitor between this pin and pin 8.</td><td>—</td></tr>
<tr><td>19</td><td>Test Pin</td><td>The function of this pin varies according to the setting of pin 1. The following table shows the details.
<table>
<tr><th colspan="2">SETTING OF PIN 1</th><th>FUNCTION OF THIS PIN</th></tr>
<tr><td colspan="2">NORMAL Mode</td><td>Use prohibited (Left open)</td></tr>
<tr><td rowspan="3">TEST Modes</td><td>TEST1</td><td>Use prohibited (Left open)</td></tr>
<tr><td>TEST2</td><td>Main counter Input pin</td></tr>
<tr><td>TEST3</td><td>Use prohibited (Left open)</td></tr>
</table>
In TEST mode (TEST2), this pin can input an external signal direct to the main counter, bypassing the 1/8 prescaler.</td><td> 
</td></tr>
<tr><td>20</td><td>$\overline{LOCK}$ Output Pin</td><td>The function of this pin varies according to the setting of pin 1. The following table shows the details.
<table>
<tr><th colspan="2">SETTING OF PIN 1</th><th>FUNCTION OF THIS PIN</th></tr>
<tr><td colspan="2">NORMAL Mode</td><td>Connect a pull-up resistor between this pin and the V_{CC} pin. When the PLL circuit is locked, the output of this pin is low level.</td></tr>
<tr><td rowspan="3">TEST Modes</td><td>TEST1</td><td>TEST mode (TEST1 and TEST2) switching.</td></tr>
<tr><td>TEST2</td><td>TEST mode (TEST1 and TEST2) switching.</td></tr>
<tr><td>TEST3</td><td>Output a high-frequency input signal divided by 256. This signal is used to measure the prescaler input sensitivity.</td></tr>
</table></td><td> 
</td></tr>
</table>

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	6.5	V
ECL Input Voltage	V_{in1}	2.0	V_{p-p}
Logic Input Voltage	V_{in2}	$-0.3 \sim V_{CC}$	V
Power Dissipation	P_D	(Note 1)	mW
Operating Temperature	T_{opr}	$-20 \sim 75$	°C
Storage Temperature	T_{stg}	$-55 \sim 150$	°C

(Note 1) TD7603Z : 890mW
TD7603F : 925mW

(Note 2) When using the device at above Ta = 25°C, decrease the power dissipation by 7.2mW for TD7603Z and 7.4mW for TD7603F for each increase of 1°C.

(Note 3) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

RECOMMENDED POWER SUPPLY VOLTAGE

PIN No.		PIN NAME	MIN.	TYP.	MAX.	UNIT
FLP	ZIP					
18	14	V_{CC} (ECL)	4.5	5.0	5.5	V
5	21	V_{CC} (I^2L)	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5V, Ta = 25°C)

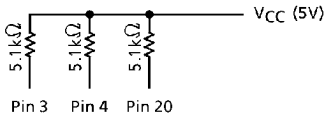
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	(ECL)	I_{CC1}	2	—	17	29	41	mA
	(I^2L)	I_{CC2}	2		8	15	23	
Maximum Band Switching Voltage		V_B MAX.	—	Bands1~4	12	—	15	V
Maximum Band Switching Input Current		I_B MAX.	—	V_{CC} = 5V	0.7	—	2.2	mA
DC Voltage		V_{15}	—	(Flat Package)	1.7	2.0	2.3	V
		V_{17}	—	(Flat Package)	1.7	2.0	2.3	
DC Current High Level		I_{IH}	—	V_{in} = 5V (Note 1)	—	180	300	μA
Input Voltage	High Level	V_{IH}	—	(Note 1)	3.0	—	—	V
	Low Level	V_{IL}	—		—	—	0.8	
Output Voltage	High Level	V_{OH}	1	(Note 2)	3.8	—	—	V
	Low Level	V_{OL}	1		—	—	0.5	
Input Current	High Level	I_{IH}	—	V_{in} = 5V	—	—	10	μA
	Low Level	I_{IL}	—	V_{in} = 0V	—	—	−20	
N/F Leak Current		I_L	—	(Note 3)	−0.2	—	0.2	μA
RF Input Sensitivity		V_{in1}	3	800-100MHz	−24	—	3	dBmW (50Ω)
		V_{in2}	3	100-1000MHz	−27	—	3	
		V_{in3}	3	1000-1300MHz	−17	—	3	
Data Input Timing		—	—	See 4. data input timing chart	—	—	—	—

(Note 1) Applicable for TEST1 clock and $\overline{LOCK}$ in input mode.
(Note 2) Applicable for data clock and $\overline{LOCK}$ in output mode.
(Note 3) Pin 10 : 2.1V, Pin 9 : Open (F package)

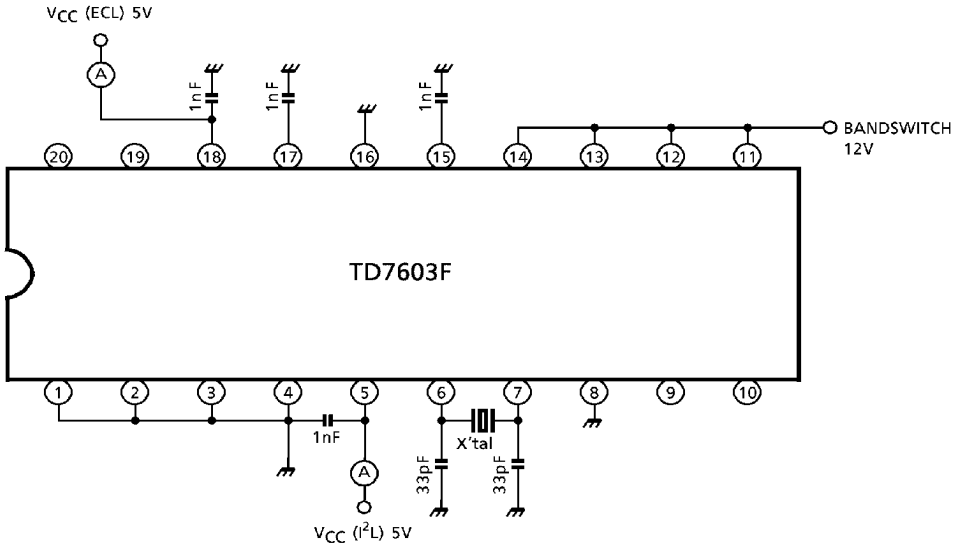
TEST MODE (Pin numbers is indicated in the case of TD7603F flat package.)

	NORMAL	MODE1	MODE2	MODE3
TEST1 (Pin 1)	L	H	H	H
Address Specification (Pin 2)	Subaddress	L	L	H
$\overline{\text{LOCK}}$ (Pin 20)	$\overline{\text{LOCK}}$	H (Pin 15 input)	L (Pin 19 input)	1 / 256 (Pin 15 input)
CLOCK (Pin 4)	Clock input	Reference signal output	Reference signal output	PD reference signal input
DATA (Pin 3)	Data input	Main counter output	Main counter output	PD compare signal input
TEST2 (Pin 19)	Inhibit	Inhibit	Divider input	Inhibit
RF INPUT (Pin 15)	RF input	RF input	Inhibit	RF input

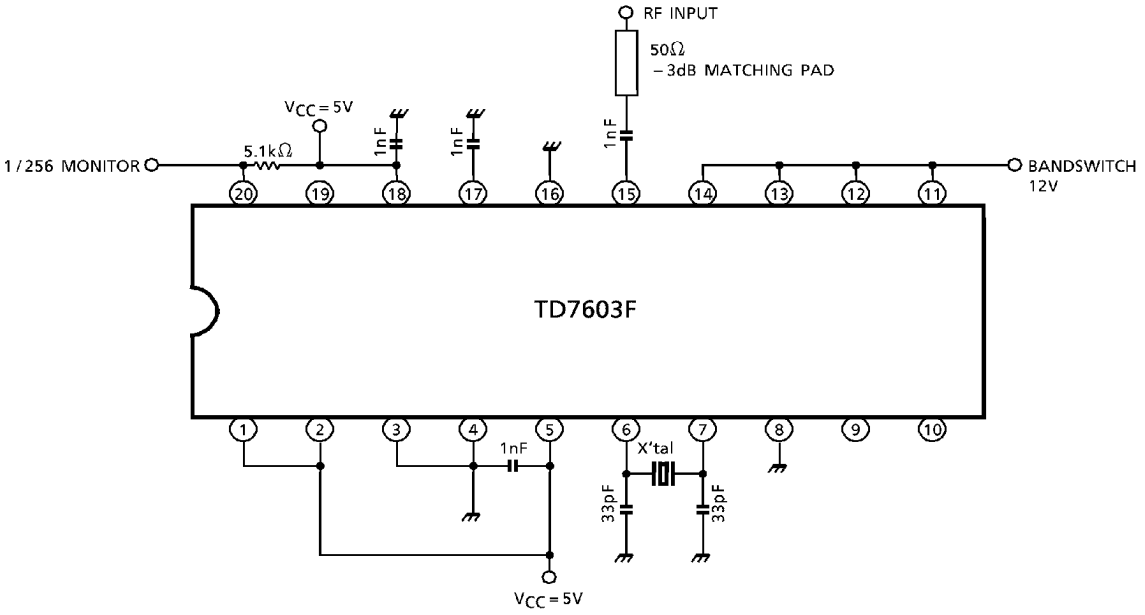
TEST CIRCUIT 1 : TEST Mode (Pin numbers are for the flat package.)



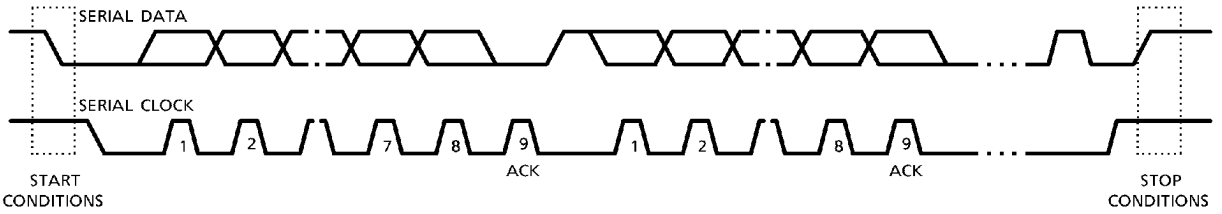
TEST CIRCUIT 2 : Power supply current measuring circuit (Pin numbers are for the flat package.)



TEST CIRCUIT 3 : Input sensitivity measuring circuit (Pin numbers are for the flat package.)



DATA INPUT TIMING CHART



ADDRESS	MAIN ADDRESS					SUBADDRESS (NOTE 1)		0	A (NOTE 2)
	1	1	0	0	0	MA1	MA2		
DIVIDER DATA (1)	0	MSB		MAN COUNTER DATA (10BIT)					A
DIVIDER DATA (2)					SWALLOW COUNTER DATA (5BIT)			LSB	A
TEST DATA	* (NOTE 3)	*	CL (NOTE 4)	PS (NOTE 5)	*	*	*	*	A
BAND DATA	*	*	*	*	BAND SWITCHING DATA (4BIT) BAND4	BAND3	BAND2	BAND1	A

(NOTE 1) SUBADDRESS SELECTOR

V_{CC} = 5V

MA1	MA2	VOLTAGE APPLIED TO ADDRESS SELECTOR
0	0	GND~0.5V
0	1	GND~5.0V (Anywhere in this range)
1	0	2.0~3.0V (Can be left open)
1	1	4.5~5.0V

(NOTE 2) A is the acknowledge bit. As WRITE mode only is supported, the TD7603 sends this bit by setting serial data to low impedance.

(NOTE 3) An asterisk (*) indicates "don't care".

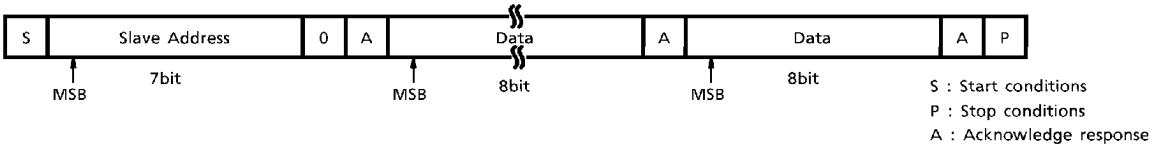
(NOTE 4) CL performs reference signal switching.
"0" indicates crystal oscillator / 2^9. "1" indicates crystal oscillator / 2^{10}.

(NOTE 5) The PS bit can be used to cut current to the preamp and prescaler when the IC is not operating. "0" indicates normal operation. "1" indicates preamp and prescaler not operating.

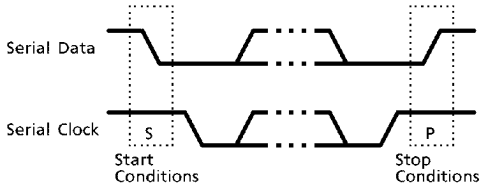
OUTLINE OF I²C BUS CONTROL FORMAT

The TD7603Z bus control format conforms with the Philips I²C bus control format.

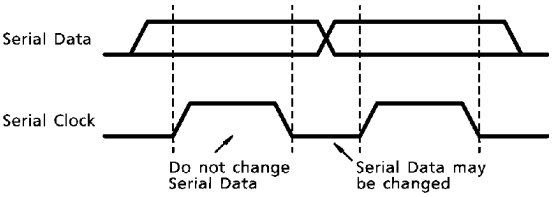
Data transfer format



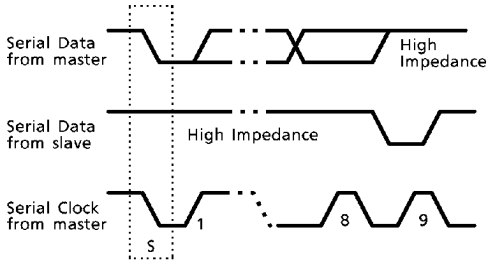
(1) Start, stop conditions



(2) Bit transfer



(3) Acknowledge response

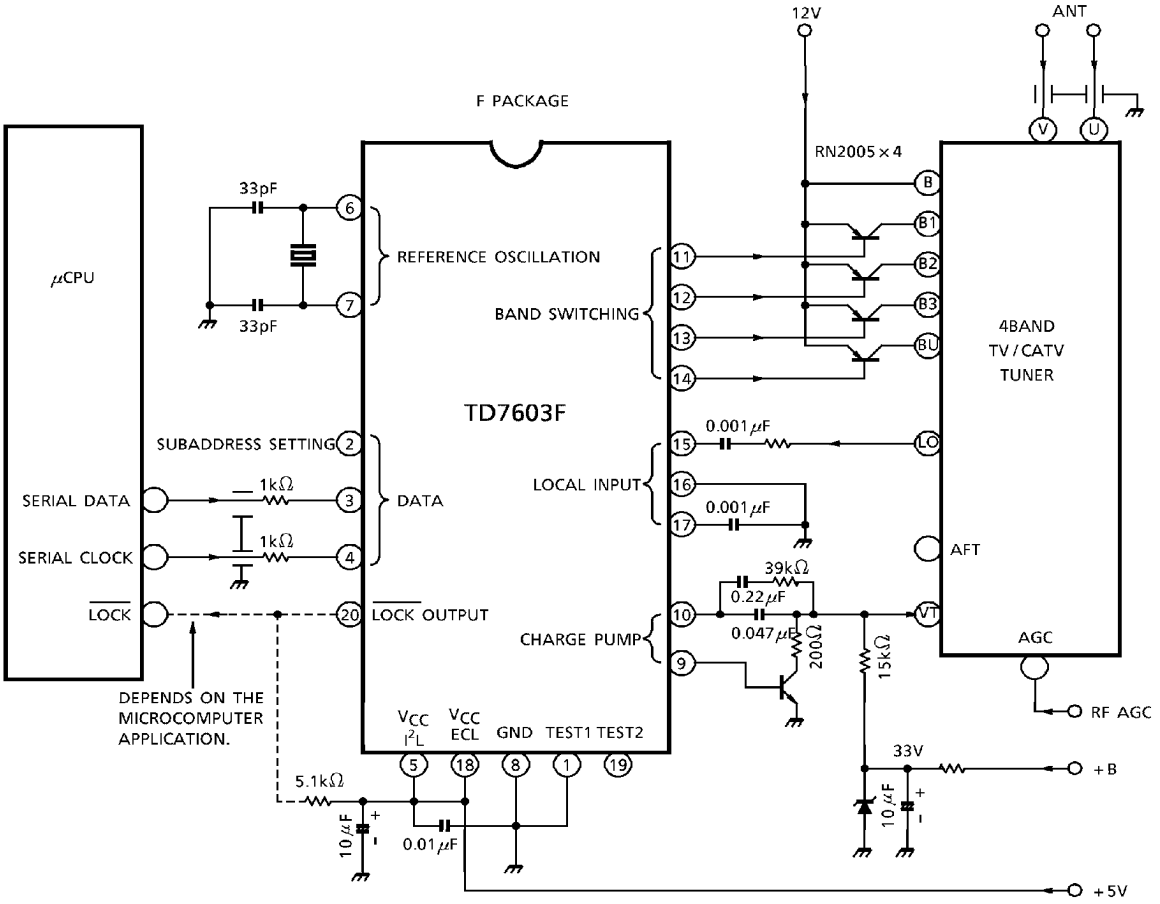


(4) Slave addresses

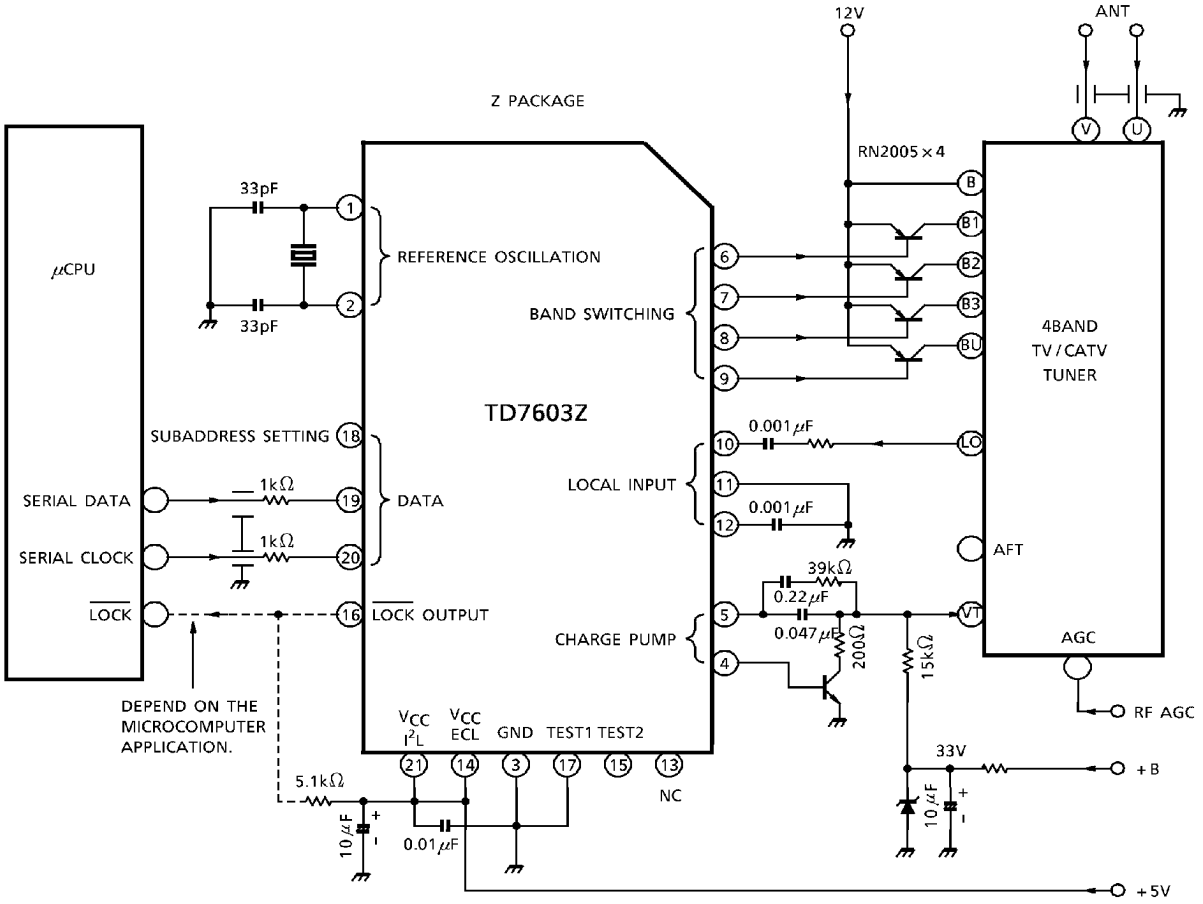
A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	0	0	*	*	0

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Tights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

SYSTEM APPLICATION DIAGRAM (For F-package)



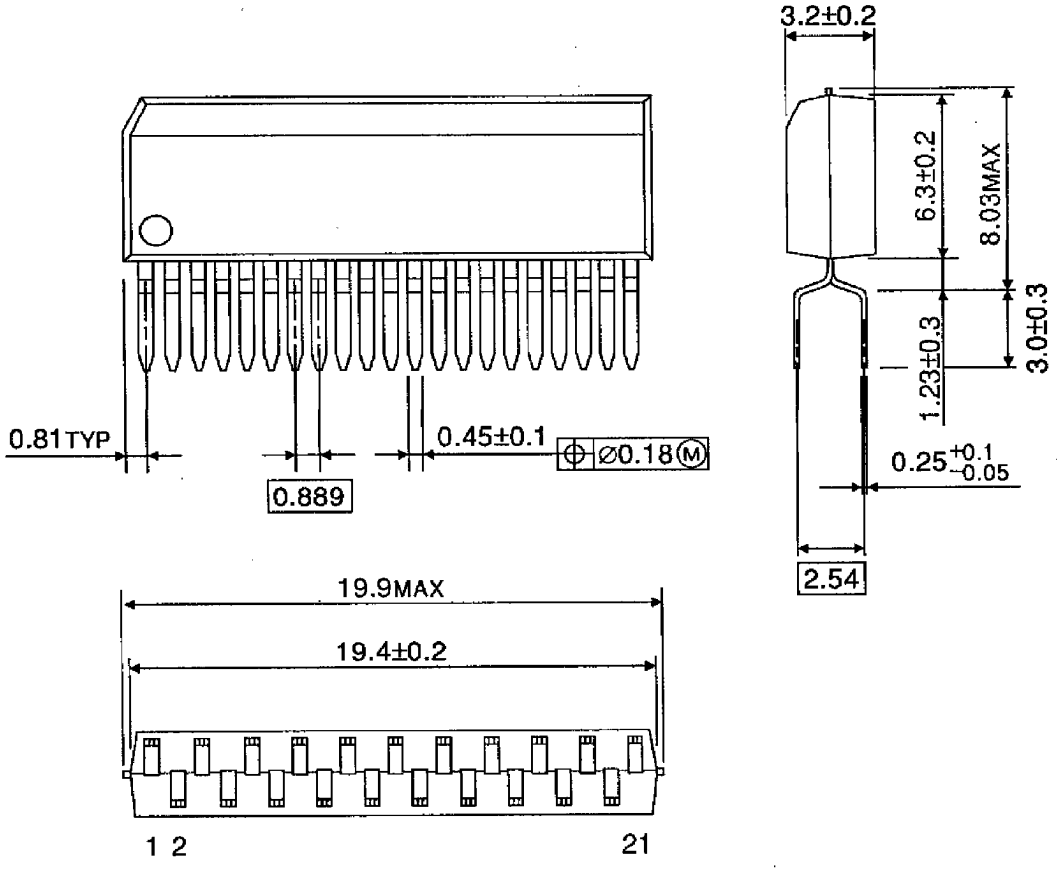
SYSTEM APPLICATION DIAGRAM (For Z-package)



OUTLINE DRAWING

SZIP21-P-0.89

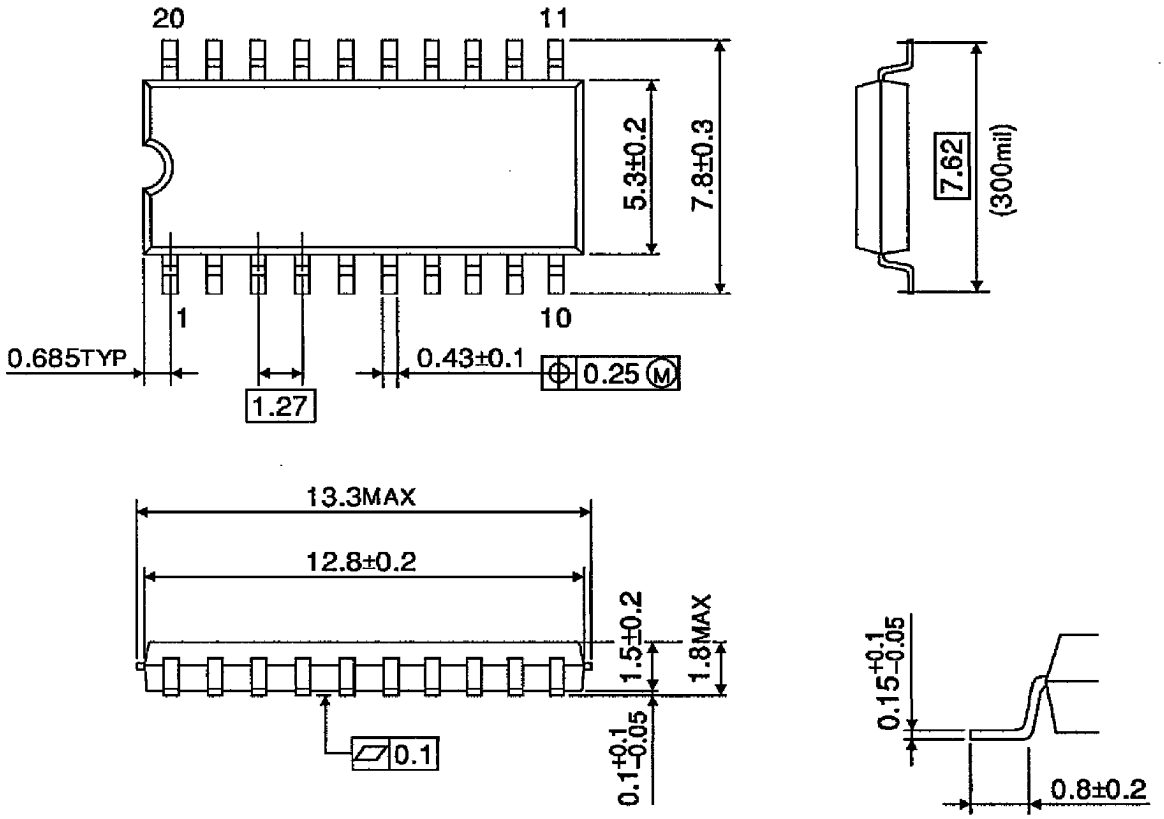
Unit : mm



Weight : 1.00g (Typ.)

OUTLINE DRAWING

SOP20-P-300-1.27 Unit : mm



Weight : 0.25g (Typ.)