SONY

1. Type No. / Manufacturer's Name 製品名・製造メーカ名

TDA6120 Series / PHILIPS SEMICONDUCTORS

2. Structure 構造

MIXED BIP / DMOS

3. Use / Function 用途・機能

30MHz / 125Vpp Video Output Amplifier

4. Package / Materials 外形

DBS 13P / Plastic

4.1 Dimensions 外形寸法 Unit 単位：mm

See Page 18

△3 この部品にはSS-00259-1に指定する物質を含んだ材料は、使用してはならない。
This part should not contain any substances which are specified in SS-00259-1.

4.2 Material & Finish of leads 端子の材質・処理

1	Material 端子の材質	Cu Zn
2	Finish めっき	Unplated

Electrostatic breakdown level 静電気強度ランク	
200pF	300 V Over
0 kΩ	

HISTORY ×COUNT	SUFFIX REPL.	ECN-NO.	DATE	REVISION	SIGN.
△6×		–	' . .		
△5×		–	' . .		
△4×		–	' . .		
△3×1		ZZ-A01367	'02.11.14	Addition of notice (SS-00259) P1×1	松村
△2×20		KV-A21983	'00.9.20	新規登録部品追加 P9-1, P12-1, P12-2, P18-1 更新No. P1×2, P2×1, P3×5, P8~9×1, P10~12×1, P18×1, P22×2	丹羽
△1×		KV-712832	'97.10.31	P/T RELEASE	k.k

AMF CHECK

AMF

AMP

TENTATIVE PART NO.

0 – – See – Page2

TITLE / DESCRIPTION

(E) IC TDA6120 Series △2 Refer to P.2

(J) IC TDA6120 Series

PLANNED BY	CHECKED BY	APPROVED BY	APPROVED BY
D C 開連技・部品 '97.10.24 石川	D C 開連技・部品 '97.10.27 松崎		D C 開連技・部品 '97.10.27 松崎

PART NO. 8–759 –See Page2

DRAWING NO. SB- V 2645

SHEET 1/22 △2 26

A4

F spec -R221

SCALE FOR MICROFILM 50 0

DRAWING

SONY STANDARD

SONY

TYPE NAME	PART NUMBER	0 NUMBER	REMARKS
TDA6120Q	8-759-488-28	0-610-556-01	Tube
△ TDA6120Q/N2/S1	8-759-680-01	0-610-885-01	Tube

50
SCALE FOR MICROFILM
0

DRAWING

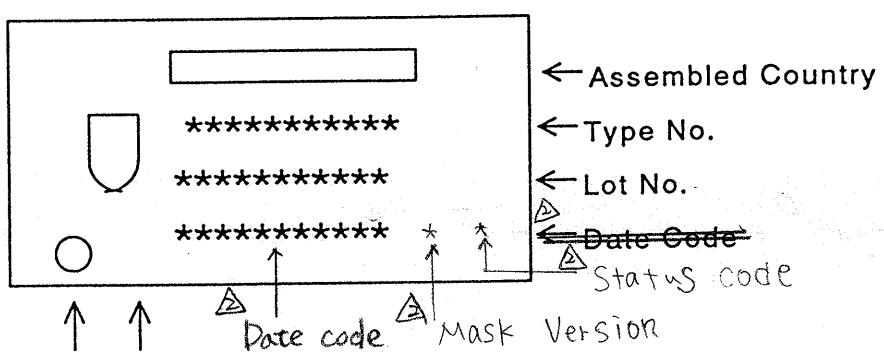
SONY STANDARD

TITLE / DESCRIPTION		DRAWING NO.	SHEET
(E) IC TDA6120 Series		SB- V2645	2
(J)			

A4

TENTATIVE PART NO

Marking　　捺　印



△2 マスクバージョンの表示例
N1バージョン→ 1
N2バージョン→ 2

MECHANICAL CHARACTERISTICS AND ENDURANCE
環境及び耐久性基準ソニー技術標準 SS00159 に準ずる。

TITLE / DESCRIPTION		DRAWING NO.	SHEET
(E) IC TDA6120 Series		SB- V2645	3
(J)			

A4

TENTATIVE PART NO

1. General description

The TDA6120Q is a single 30MHz/125Vpp monolithic video output amplifier in a DBS13P (Dil Bended Sil 13 pins Power) package SOT141RFG, using high-voltage DMOS technology, and is intended to drive the cathodes of a CRT in High Definition TV's or monitors.

2. Features

The features are:

- High large signal bandwidth of 32MHz typ. at 125 Vpp,
- High small signal bandwidth of 47MHz typ. at 60 Vpp,
- Rise/fall time of 12.5ns for 125 Vpp,
- High slew rate of 10 V/ns,
- Low static power dissipation of 2.1W at 200V supply voltage,
- High maximum output voltage,
- Bandwidth independant of voltage gain,
- Maximum overall voltage gain over 46dB,
- High Power Supply Rejection Ratio,
- Fast cathode-current measurement output for dark-current control loop,
- Differential voltage input.

3. Package outline

The encapsulation SOT141RFG is a 13 pins Power DBS (Dil Bended Sil) package. The thermal resistance of the package is:

$R_{th,j\text{-}case} = 2.0$ K/W

An external heatsink is necessary (conditions see 10.1).

4. Block diagram

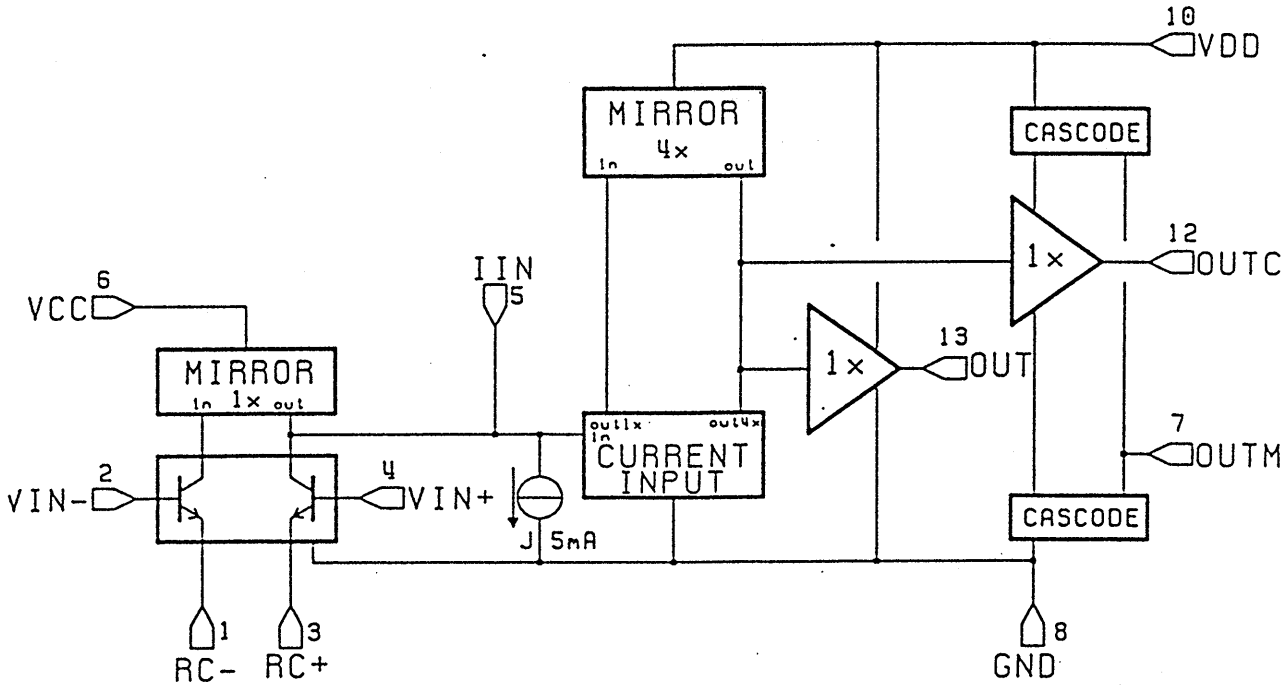


Figure 4-1 Block diagram

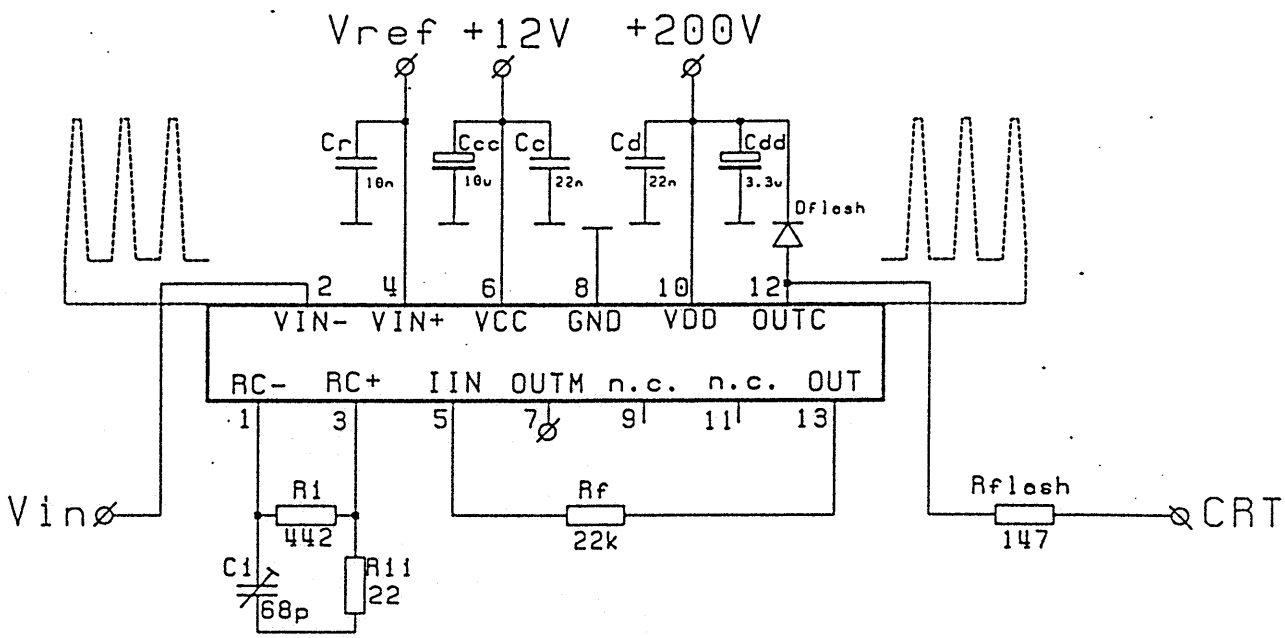


Figure 4-2 Top view

SCALE FOR MICROFILM 50 0

DRAWING

SONY STANDARD

TITLE / DESCRIPTION (E)	IC	TDA6120 Series	DRAWING NO.	SHEET
(J)			SB- V2645	6

A4

TENTATIVE PART NO

5. Pinning

The pinning of the TDA6120Q is shown below:

1 RC- inverting input pre-emphasis network

2 VIN- inverting voltage input

3 RC+ non-inverting input pre-emphasis network

4 VIN+ non-inverting voltage input

5 IIN feedback current input

6 VCC low supply voltage (12V)

7 OUTM cathode current measurement output

8 GND power ground and heatsink

9 n.c.

10 VDD high supply voltage (200V)

11 n.c.

12 OUTC cathode output

13 OUT feedback output

TDA6120Q
P/N: 8-759-488-28

(Voltages with respect to pin 8 (ground) unless otherwise specified, currents specified as in fig 4-1)

TABLE 6-1

No.	Parameter	Symbol	Min	Max	Unit
101	Supply Voltage High	V_{dd}	0	280	V
102	Supply Voltage Low	V_{cc}	0	24	V
104	Voltage-Input Voltage	V_{vin+}, V_{vin-}	0	V_{cc}	V
105	Differential Mode Voltage-Input Voltage	$V_{vin+} - V_{vin-}$	$-V_{cc}$	V_{cc}	V
106	Pre-emphasis Input Voltage	V_{rc+}, V_{rc-}	0	V_{cc}	V
107	Differential Mode Pre-emphasis Input Voltage	$V_{rc+} - V_{rc-}$	$-V_{cc}$	V_{cc}	V
108	Current-Input Voltage	V_{iin}	0	$2V_{be}$	V
109	Measurement Output Voltage	V_{outm}	0	24	V
110	Output Voltage	V_{out}, V_{outc}	0	V_{dd}	V
111	Storage Temperature	T_{stg}	-55	150	°C
112	Junction Temperature	T_j	-20	150	°C
113	Voltage peak (ESD-HBM)	V_{esd}-HBM	-	2000 Note 1	V
114	Voltage peak (ESD-MM)	V_{esd}-MM	-	300 Note 2	V

Note 1: 1250V for IIN (pin 5) and
750V for OUTM (pin 7)

Note 2: 200V for IIN (pin 5) and OUTM (pin 7)

TDA 6120 Q
P/N : 8-759-488-28

6. Ratings

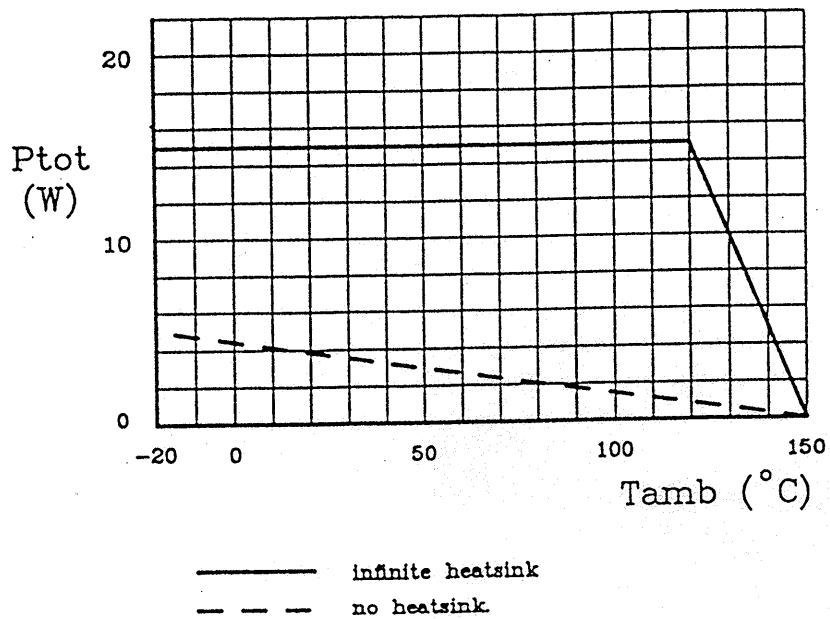


Figure 6-1 Power derating curves.

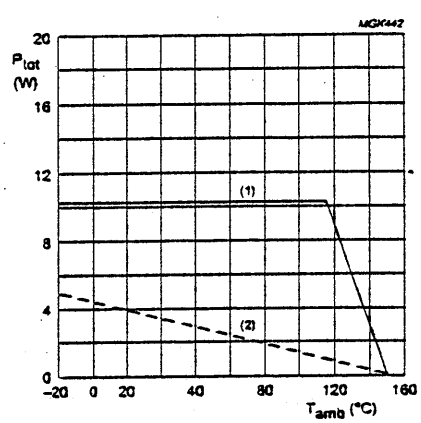
TDA6120Q/N2/S1
P/N: 8-759-680-01

Video output amplifier

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	high supply voltage		0	280	V
V_{CC}	low supply voltage		0	20	V
V_i	input voltage (pins 2 and 4)		0	V_{CC}	V
$V_{i(dif)}$	differential mode input voltage (pins 2 and 4)		$-V_{CC}$	V_{CC}	V
$V_{i(pe)}$	pre-emphasis input voltage (pins 1 and 3)		0	V_{CC}	V
$V_{i(dif)(pe)}$	differential mode pre-emphasis input voltage (pins 1 and 3)		$-V_{CC}$	V_{CC}	V
V_{IIN}	input voltage (pin 5)		0	$2V_{BE}$	V
V_{OUTM}	measurement output voltage		0	20	V
V_o	output voltage (pins 12 and 13)		0	V_{DD}	V
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−20	+150	°C
V_{ESD}	voltage peak human body model		−	2000	V
	voltage peak machine model		−	300	V



(1) Infinite heatsink.
(2) No heatsink.

Power derating curve.

②頁追加

TITLE/DESCRIPTION	DRAWING NO.	SHEET
(E) IC	SB- V 2645	9-1
(J)		

A4
'96. 2

TENTATIVE PART NO. 0-610-885-01

F spec - B223-2

△ TDA 6120Q
P/N: 8-759-680-01

7. Characteristics

- Operating range:
$T_{junction}$ = -20 to 150 °C,
V_{dd} = 180 to 250 V,
V_{cc} = 10.8 to 13.2 V,
V_{outm} = 4 to 20V,
V_{vin+} = 1.5 to 5 V.
V_{vin-} = 1.5 to 5 V.

-Test conditions (unless otherwise specified): T_{amb} = 25 °C, V_{dd} = 200 V, V_{cc} = 12 V, V_{vin+} = 3 V, V_{outm} = 6 V, C_L = 10 pF (C_L consists of parasitic and cathode capacitance), $R_{TH,heatsink}$ = 4 K/W. (Test circuit: see figure 7-1.)

TABLE 7-1

No	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
1	Quiescent High Voltage Supply Current	V_{OUTC} = 100V	I_{dd}	8	10	12	mA
2	Quiescent Low Voltage Supply Current	V_{VIN-} = V_{VIN+}	Icc	25	31	39	mA
3	Input Bias Current (pin 2,4)	V_{OUTC} = 100V	I_{bias}		30		uA
5	DC Output Voltage (pin 12,13)	V_{VIN-} = V_{VIN+}	$V_{outc,dc}$	80	100	120	V
6.	DC Output Voltage Temperature Drift (pin 12,13)	V_{VIN-} = V_{VIN+}	$\delta V_{outc,dc}$			5	V
7	Offset Current of Measurement Output	Note 1	$I_{outm,off}$	-40	40	120	uA
8	Linearity of Current Transfer	-1mA<I_{OUTC}<+1mA	ΔI_{outm} / ΔI_{outc}	0.9	1.0	1.1	
9	Input Capacitance (pin 2,4)	$V_{OUTC-dc}$ = $V_{outc,max}$	$C_{in,CM}$		3		pF
11	Maximum Dynamic Peak Output Current (pin 12)	20V<V_{OUTC}<V_{dd}-20V	$I_{outc,max}$		100		mA

△ TDA 6120 Q
P/N : 8-759-680-01

7. Characteristics

TABLE 7-1 [continued]

No	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
12	Minimum Output Voltage (pin 12)		$V_{outc,min}$		4	10	V
13	Maximum Output Voltage (pin 12)		$V_{outc,max}$	$V_{dd}-10$	$V_{dd}-6$		V
14	Internal Gain		Aint	1.68	1.87	2.08	
15	Small Signal Bandwidth (pin 12)	$V_{OUTC-ac}=60V_{pp}$ $V_{OUTC-dc}=100V$	BW_s	40	47		MHz
16	Large Signal Bandwidth (pin 12)	$V_{OUTC-ac}=125V_{pp}$ $V_{OUTC-dc}=100V$	BW_l	28	32		MHz
17	Cathode Output Propagation Time : 50% input - 50% output (pin 12) (See fig. 7-2 and 7-3)	$V_{OUTC-ac}=125V_{pp}$ $V_{OUTC-dc}=100V$ square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	T_p	10		15	ns
18	Cathode Output Rise Time : 10% output - 90% output (pin 12) (See fig. 7-2)	$V_{OUTC-ac}=125V_{pp}$ $V_{OUTC-dc}=100V$ square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	T_r	10	14	18	ns
19	Cathode Output Fall Time : 90% output - 10% output (pin 12) (See fig. 7-3)	$V_{OUTC-ac}=125V_{pp}$ $V_{OUTC-dc}=100V$ square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	T_f	10	12.5	15	ns
20	Settling Time : 50%input -(99%<output<101%) (pin 12) (See fig. 7-2 and 7-3)	$V_{OUTC-ac}=125V_{pp}$ $V_{OUTC-dc}=100V$ square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	T_s			250	ns

△ TDA6120Q
P/N : 8-759-680-01

TABLE 7-1 [continued]

No	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
21	Slew Rate between 30V - (Vdd-30V) (pin 12)	V_{VIN-} = $2V_{pp}$ square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	SR-rise SR-fall		8 10		V/ns V/ns
22	Cathode Output Voltage Overshoot (pin 12) (See fig. 7-2 and 7-3)	$V_{OUTC-ac}$=$125V_{pp}$ $V_{OUTC-dc}$=100V square wave: f<1MHz $T_{f,VIN-}$ = 10ns $T_{r,VIN-}$ = 10ns	OV-rise OV-fall		5 20		% %
23	High Voltage Power Supply Rejection Ratio	f < 50kHz	PSRR Note 2		44		dB
24	Low Voltage Power Supply Rejection Ratio	f < 50kHz	PSRR Note 2		48		dB

Note 1:
The operating range of the measurement output OUTM is 4 to 20V. Below 4V OUTM acts as a voltage source with an output resistance such that the maximum

current coming from OUTM is 2mA.

Note 2:
PSRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

TDA6120Q/2N/S1
P/N: 8-759-680-01

CHARACTERISTICS

Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V; V_{CC} = 10.8 to 13.2 V; V_{OUTM} = 3 to 16. 5 V; V_{VIN-} = 1.5 to V_{CC} - 6 V; V_{VIN+} = 1.5 to V_{CC} - 6 V.
Test conditions: T_j = 25 °C; V_{DD} = 200 V; V_{CC} = 12 V; V_{VIN+} = 3 V; V_{OUTM} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\,h}$ = 4 K/W; test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(q)}$	quiescent high voltage supply current	V_{OUTC} = 100 V	9	11	13	mA
$I_{CC(q)}$	quiescent low voltage supply current	$V_{VIN-} = V_{VIN+}$	35	45	55	mA
I_{bias}	input bias current (pins 2 and 4)	V_{OUTC} = 100 V	–	76	–	µA
V_{OUTC}	DC output voltage (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	85	103	120	V
$\Delta V_{OUTC(T)}$	DC output voltage temperature drift (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$ temperature range 30°C < Tj < 110°C	-100	-25	+55	mV/°C
$I_{(offset)OUTM}$	offset current of measurement output	note 1	-30	0	30	µA
$\Delta I_{OUTM}/\Delta I_{OUTC}$	linearity of current transfer	–50 µA < I_{OUTC} < +50 µA; note 1	–	1.0	–	
C_i	input capacitance (pins 2 and 4)	$V_{OUTC} = V_{OUTC(max)}$	–	4	–	pF
$I_{OUTC(max)}$	maximum dynamic peak output current (pin 12)	20 V < V_{OUTC} < V_{DD} – 20 V	–	100	–	mA
$V_{OUTC(min)}$	minimum output voltage (pin 12)		–	4	10	V
$V_{OUTC(max)}$	maximum output voltage (pin 12)		V_{DD} – 10	V_{DD} – 6	–	V
$V_{CC(sw)}$	V_{CC} switch level at which pins OUT and OUTC become HIGH		–	8.8	–	V
G_{int}	internal gain		1.68	1.87	2.08	
B_s	small signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 60 V (p-p); $V_{OUTC(DC)}$ = 100 V	40	47	–	MHz
B_l	large signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V	28	32	–	MHz
t_{pd}	cathode output propagation time 50% input to 50% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	10	–	15	ns

△ 夏追加

TDA6120Q/2N/S1
P/N: 8-759-680-01

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{o(r)}$	cathode output rise time 10% output to 90% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.6	10	12.5	18	ns
$t_{o(f)}$	cathode output fall time 90% output to 10% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.7	10	12.5	15	ns
t_{st}	settling time 50% input to (99% ≤ output < 101%) (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	–	350	ns
SR_r	slew rate rise between 30 V to (V_{DD} – 30 V) (pin 12)	V_{VIN-} = 2 V (p-p) square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns	–	8	–	V/ns
SR_f	slew rate fall between (V_{DD} – 30 V) to 30 V (pin 12)	V_{VIN-} = 2 V (p-p) square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns;	–	10	–	V/ns
O_{Vr}	cathode output voltage overshoot rise (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	5	–	%
O_{Vf}	cathode output voltage overshoot fall (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	20	–	%
PSRRh	high voltage power supply rejection ratio	f < 50 kHz; note 2	–	44	–	dB
PSRRl	low voltage power supply rejection ratio	f < 50 kHz; note 2	–	48	–	dB

Notes

1. The operating range of the measurement output OUTM is 3 to 16.5 V. Below 3 V, OUTM acts as a voltage source with an output resistance such that the maximum current input from OUTM is 1.25 mA.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

△2 頁追加

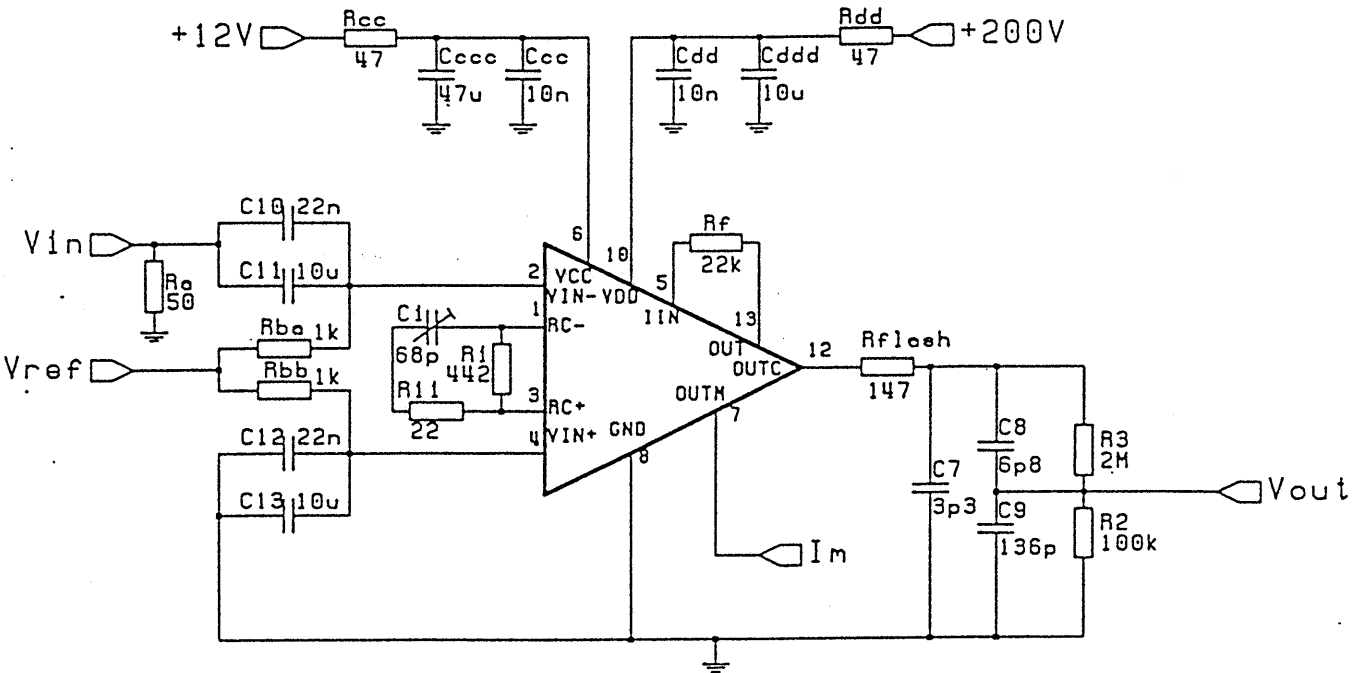


Figure 7-1 Testcircuit with gain of 40 dB.

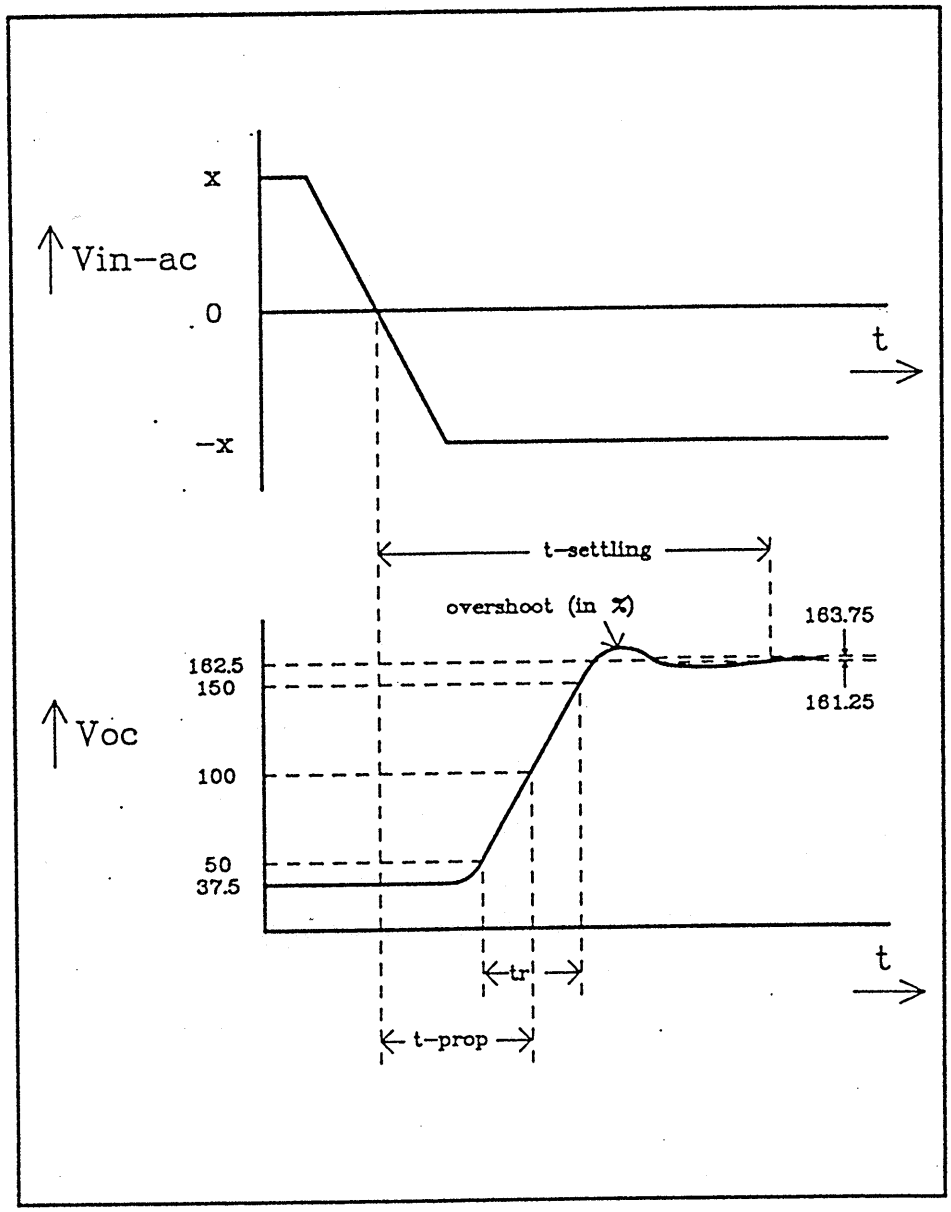


Figure 7-2 Output (pin 12 and 13; rising edge) as a function of input signal

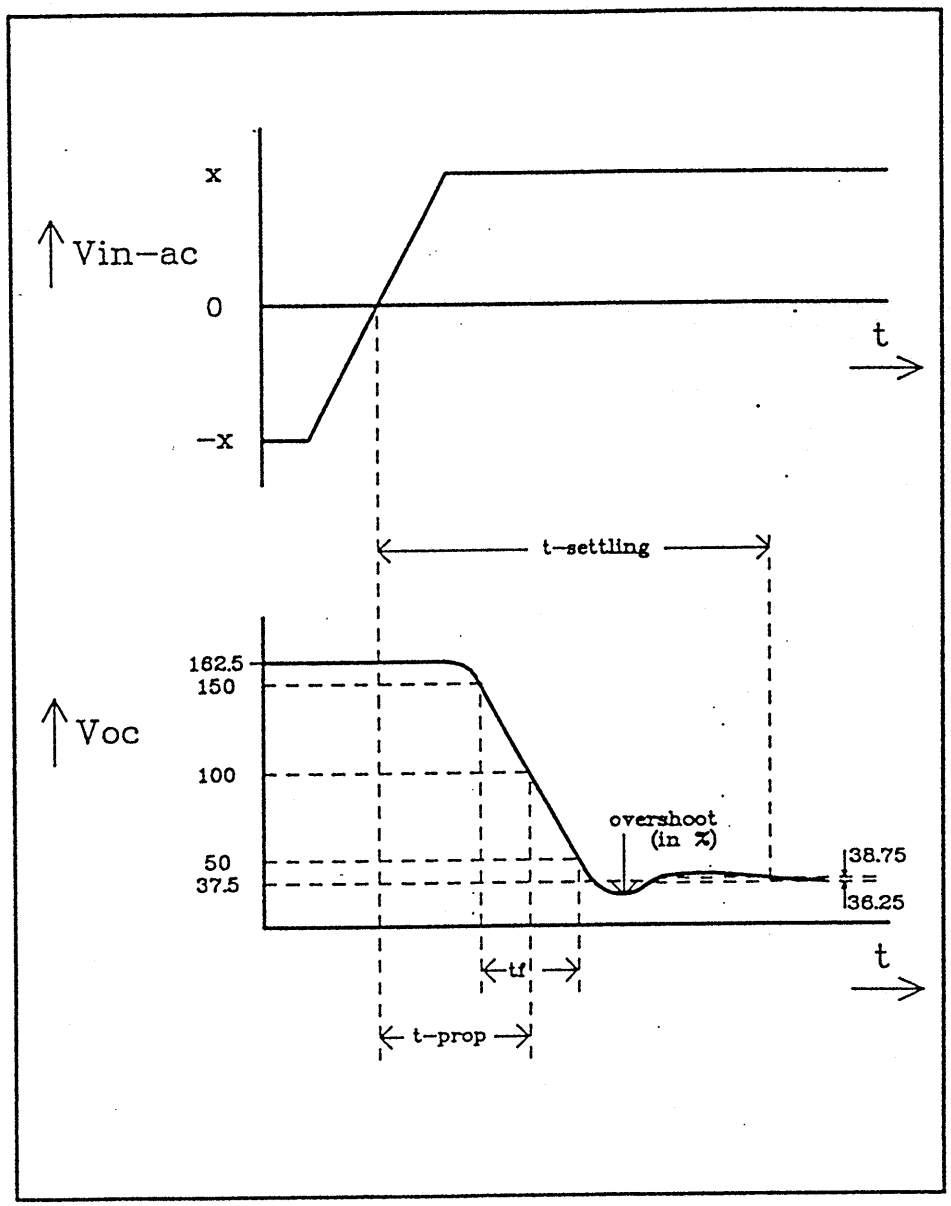


Figure 7-3 Output (pin 12 and 13; falling edge) as a function of input signal

8. Notes

8.1 Flashover Protection

The TDA6120Q does NOT include protection diodes that clamp the cathode output pin to the high voltage supply pin during a CRT flashover discharge. Therefore an external high voltage reverse biased diode has to be connected between the OUTC pin and the VDD pin. An externa 220Ω carbon high-voltage resistor in combination with a 2kV spark gap between the cathode and ground will limit the maximum clamp current (for this resistor-value, the CRT has to be connected to the main PCB). This external network causes an increase in the rise- and falltimes of about 1 ns and a decrease in the overshoot of about 3%.

VDD-GND must be decoupled:

a) By a capacitor > 22nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pin 10 and pin 8; definitely within 5 mm.
b) By a capacitor > 3.3 µF on the picture tube base printed circuit board (common for three output stages).

9. Quality specification

Quality specification SNW-FQ-611 part E is applicable.

10. Test- and application- information

10.1 Dissipation

Regarding dissipation, distinction must be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6120Q is due to supply currents,

and currents in the feedback network and CRT.

$$P_{stat} = V_{dd}*I_{dd} - V_{oc}*(V_{oc}/Rf-I_{oc}),$$

where Rf = feedback resistance, and
Ioc = DC cathode current.

The dynamic dissipation equals:

$$P_{dyn} = V_{dd}*(C_l+C_f+C_{int})*f*V_{o,pp}*b,$$

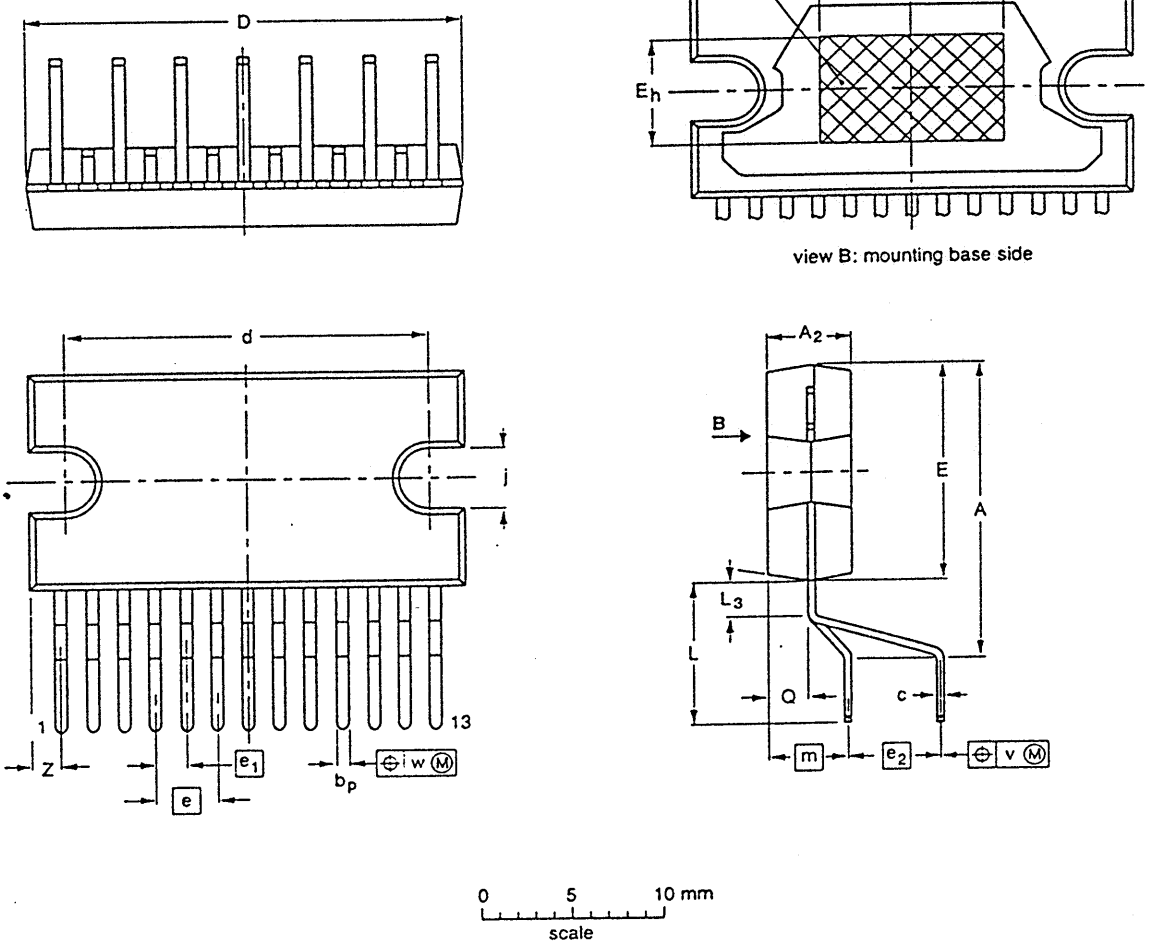
where C_l = load capacitance,
C_f = feedback capacitance,
C_{int} = effective internal load capacitance (about 7pF),
f = frequency,
$V_{o,pp}$ = peak to peak output voltage, and
b = non-blanking duty-cycle (0.8).

The IC must be mounted on the picture tube base printed circuit board to minimize the load capacitance C_l.

△ TDA6120Q

CHAPTER 2 P/N: 8-759-488-28
IC Package Range and Dimensions

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm) SOT141-8



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-8						~~92-11-17~~ 95-03-11

TITLE / DESCRIPTION		DRAWING NO.	SHEET
(E) IC TDA6120 Series		SB- V 2645	18
(J)			

A4

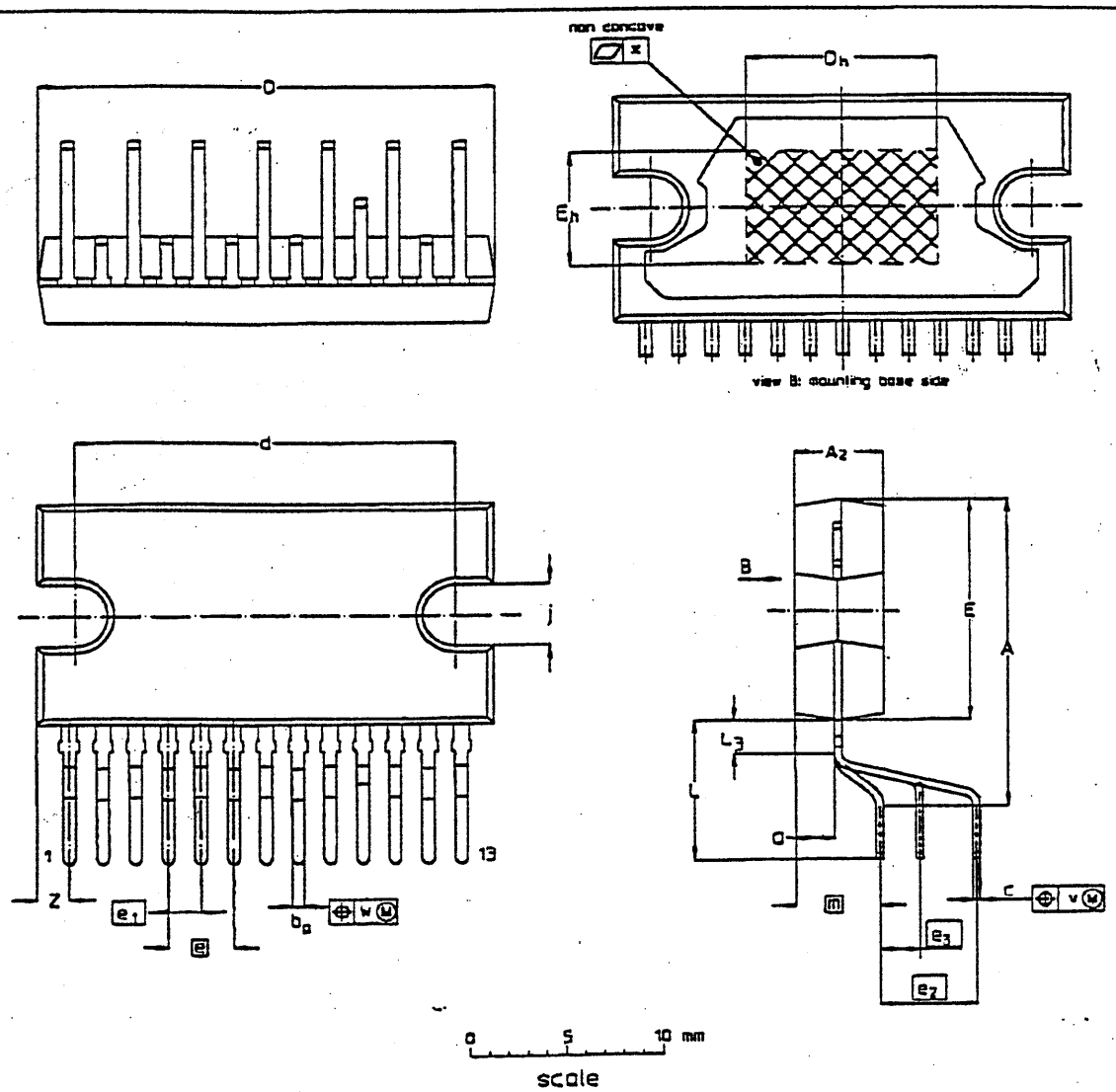
TENTATIVE PART NO

SONY

TDA6120Q/N2/S1

P/N: 8-759-620-01

TBS13P:plastic Tripple bent Sil power package: 13 leads



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	D[1]	d	D_h	E[1]	e	e_1	e_2	e_3	E_h	j	L	L_3	m	Q	v	w	x	Z[1]	
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	2.1	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45	

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT 578-1						

△ 頁追加

TITLE/DESCRIPTION		DRAWING NO.	SHEET
(E)	IC	SB- V 2645	18-1
(J)	IC		

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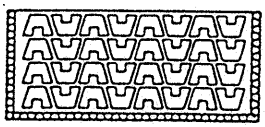
'96. 2

TENTATIVE PART NO. 0-610-885-01

F spec - B221-2

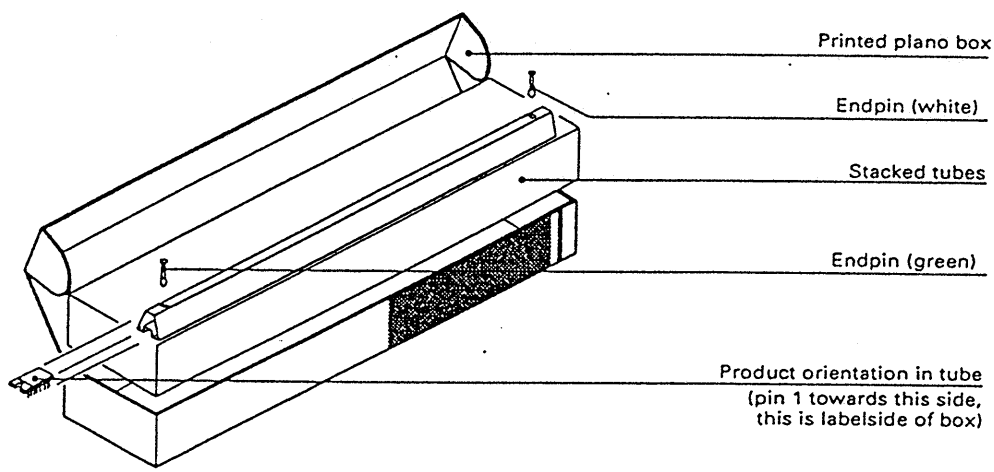
SONY STANDARD DRAWING FOR MICROFILM SCALE 0 50

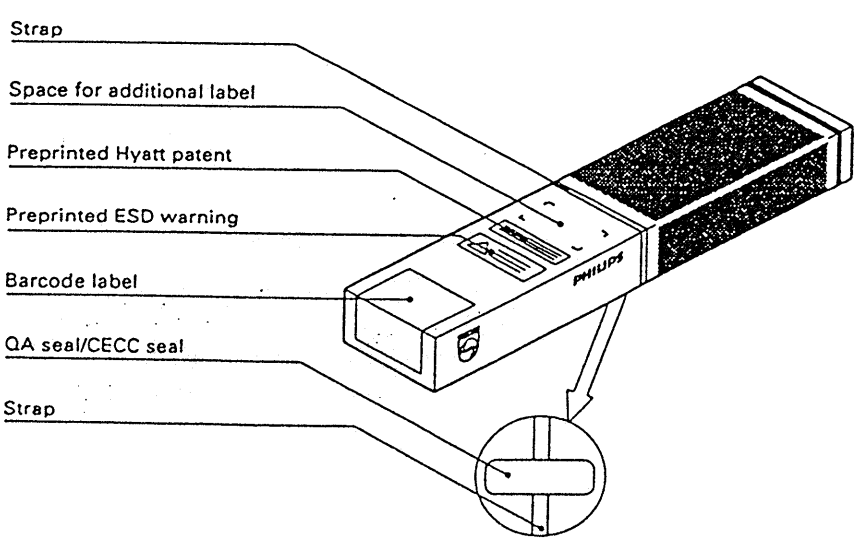
Packing for DIP (Tube/Pin)



Stacking method

Item	Material	Weight (g)
Box	Cardboard carbon coated	145
Seal	Acrylate	0.2
Labels	Paper	1.65
Endstops	Poly Vinyl Chloride	9
Tubes	Poly Vinyl Chloride	800
Strap	Poly Propylene	0.7





TITLE / DESCRIPTION		DRAWING NO.	SHEET
(E) IC TDA6120 Series		SB- V 2645	19
(J)			

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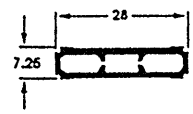
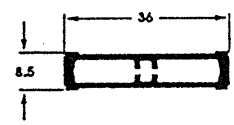
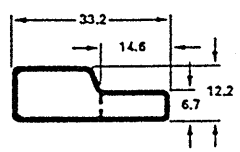
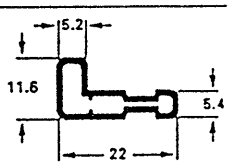
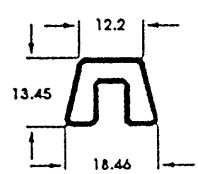
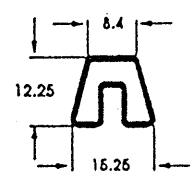
TENTATIVE PART NO

TUBE PACKING – THROUGH HOLE

package name	Philips package type/ outline code[1)]	carrier length (mm)	end stop	SPQ	carriers per box	PQ	outer box dimensions (mm)	carrier profile
DBS9MPF	SOT111	501	plug	22	34	748	530×136×65	
SIL9MP	SOT142	501	plug	22	34	748	530×136×65	
SIL9MPF	SOT110	501	plug	22	34	748	530×136×65	
SIL9P	SOT131	575	plug	23	24	552	595×137×68	
SIL13P	SOT193	575	plug	23	24	552	595×137×68	
DBS9P	SOT157	575	plug	23	24	552	595×137×68	
DBS13P	SOT141	575	plug	23	24	552	595×137×68	
DBS17P*	SOT243	575	plug	23	24	552	595×137×68	
RBS9MPF	SOT352	501	plug	22	42	924	530×136×65	
DIP22	SOT116	501	pin	17	32	544	530×136×65	
DIP22	SOT116	575	pin	21	40	840	595×137×68	
DIP24	SOT248	501	pin	15	32	480	530×136×65	
SDIP24	SOT234	575	pin	25	40	1000	595×137×68	
SDIP32	SOT232	575	pin	19	40	760	595×137×68	
DIP8	SOT97	501	pin	50	40	2000	532×142×63	

Note

1) If only a package type code is given, the data supplied is applicable to all its outline versions.

___. Marking on the supply package　納入梱包への表示

The following items shall be marked indelibly and legibly on each unit pack.
最小梱包単位に、次の事項を記入すること。

(1) Manufacturer's name or trade mark.　製造者名（略称も可）または略号
(2) Month and year of production or code.　製造年月日または略号
(incruding Lot No.)　（ロット番号を含む）
(3) Type No. and classification.　型名および選別ランク
(4) Part No. of Sony.　ソニーの部品番号

___. Approval　検　定

___.1 Prior to delivery, supplier shall submit the following to the local purchasing department for approval:
納入者は納品に先立ち、下記のものを担当購買部門に提出し検定を受けること。

(1) Semiconductor Approval Application sheets　半導体納入仕様書 ___4___ copies
(2) Reliability test results (data)　信頼性試験データ _____ copies
(3) Sample for approval evaluation　検定サンプル _____ pieces

** For the number of copies and quantity of samples, supplier shall consult with the local purchasing department.
コピー部数／サンプル数は担当資材部門と協議。

Semiconductor Approval Application shall be listed the following items.
半導体納入仕様書は、次の事項を記載すること。

a) All items designated in the specification. Furthermore, dimensions in detail, materials employed, finish and specifications.
○本仕様書に指定された各項目さらに細部の寸法、使用される材質・処理および規格を明記。

b) When materials such as thermoplastics and other inflammable are used, the following shall be clearly indicated:
(Except for ordinary Epoxy Molding Compound.)
1) list of materials and manufacturer's name
2) Trade name and type
3) Flammability classification in UL
4) UL File No.
○熱可塑性プラスティック他の可燃性材料については、下記事項を明記。（通常のエポキシモールドは除外）
1) 材料名・材料メーカーのリスト
2) 商品名および型名
3) ＵＬの難燃性グレード
4) ＵＬファイルナンバー

c) For tin or zinc plated (including chromate treatment) products, specify whisker prevention methods.
○錫めっき・亜鉛めっき（クロメート処理も含む）した製品については、ウィスカー対策の方法を明記。

d) If requested by Sony, include name of manufacturing plant, a chart detail process employed and person(s) responsible for quality control in the Approval Application or in an attached sheet.
○ソニーから要求がある場合は、製造所名・製造工程表・品質責任者を半導体納入仕様書または、添付の資料へ明記。

e) Specifications, which are different from those requested by Sony, shall be marked with "▲" in red and also listed on the cover of Approval Application.
○本仕様書の要求と異なる規格値等は赤▲印を付け、さらに表紙に明記。

___.2 Prior to the alternation of specifications (including materials and construction) and/or manufacturing plant and/or production process etc., supplier shall consult with Sony and acquire approval as specified in the foregoing paragraph.
仕様（材料・構造を含む）、製造所・製造工程等の変更を希望する場合は、ソニーと事前協議のうえ前項の要領にて検定を受けること。

___.3 For procedures and filling out the Approval Application, refer to "SEMICONDUCTOR DEVICES' APPROVAL APPLICATION PROCEDURE" (English manual only).
For procedures in Japan (domestic rule), refer to Sony technical manual "STM-0028".
手続と半導体納入仕様書の記載については、「半導体デバイス検定手続」（英語版のみ）を参照。
日本（国内ルール）の手続は、ソニー技術マニュアル STM-0028『半導体納入仕様書提出要領（納入者用）』を参照。

SONY

_____. Referential contents table of information for board assembly [Semiconductor devices]
実装関連情報参照目次 [半導体ﾃﾞﾊﾞｲｽ用]

		Items for board assembly 実装関連仕様項目	Segment for checking 区分	Page 参照頁	Remarks 備考
Outline / Structure 外形 / 構造	① *	Dimensions / Torelance 外形寸法 / 公差	See Dimensions. 外形寸法の項に記載	18,	② 18-1
	② *	Lead pitch, Lead length, Dimensions リードピッチ / 長さ / 寸法	See Dimensions. 外形寸法の項に記載	18,	② 18-1
	③	Conceptual drawing of construction 構造概略図	Special construction only 特殊な構造の場合のみ記載		
	④ *	Material and Treatment of terminal leads 端子の材質・処理	Refer to cover sheet. 表紙を参照	1	
	⑤	Detail of soldering area of a terminal lead 端子のはんだ付け部分詳細図	☐specified, ☑not specified 記載有り 記載無し		
	⑥	Referential weight of the device 部品重量（参考値）	☐specified, ☑not specified 記載有り 記載無し		
	⑦ *	Pinning diagram or pin assignment 端子接続図、または端子の割付	See Pinning diagram 端子接続の項に記載		
	⑧ *	Mechanical index for direction 方向を示す指標	See Dimensions or Marking 外形寸法またはﾏｰｷﾝｸﾞに記載	4	
Characteristics for board assembly 実装仕様	Resistance to soldering heat はんだ耐熱性 ⑨ *	for dip soldering はんだディップ耐熱	☐specified, ☑not specified 記載有り 記載無し		
	Resistance to soldering heat はんだ耐熱性 ⑩ *	for reflow soldering はんだリフロー耐熱	☐specified, ☑not specified 記載有り 記載無し ☐Permitted cycles of heat 許容リフロー回数 (____ times)		
	⑪	Conditions for Hand soldering 手はんだの条件	☐specified, ☑not specified 記載有り 記載無し		
	⑫	Unsealed storage condition 開封保存条件	☐specified, ☑not specified 記載有り 記載無し		
Type and Material of supply packaging 供給梱包の形態と材質		☐ Axial tape packaging アキシャル・テーピング → ☐ reel リール / ☐ zig zag つづら折り・カートン ☐ Radial tape packaging ラジアル・テーピング → ☐ reel リール / ☐ zig zag つづら折り・カートン ☐ Embossed tape packaging エンボス・テーピング ☐ Adhesive tape packaging 粘着型・紙テーピング ☐ Hard tray adoptable for dry heat 耐熱型ハード・トレイ ☐ Hard tray 非耐熱ハード・トレイ ☐ Stick type スティック ☐ Other type of tray その他のトレイ ☑ Others その他		19	
	⑬ *	Total number on unit Package 梱包単位上の標準収納数量	☑specified, ☐not specified 記載有り 記載無し	20	
Spec. for tape packaging テーピング仕様	⑭ *	Thickness, Width テープ厚み, テープ幅	See Tape packaging テーピングの項に記載		
	⑮ *	Pitch of sproket hole and parts 送りピッチ, 部品ピッチ	See Tape packaging テーピングの項に記載		
	⑯ *	Hight on the board after insertion 基板面高さ (for insert lead type)	See Tape packaging テーピングの項に記載		
	⑰ *	Alignment of devices 部品整列方向	See Tape packaging テーピングの項に記載		
	⑱ *	Size of reel or carton box リール寸法, カートン寸法	See Tape packaging テーピングの項に記載		
Spec. for tray トレイ仕様	⑲ *	Tray dimensions トレイ寸法図	See Tray dimensions トレイ寸法の項に記載		
	⑳ *	Alignment of devices (or position of #1-pin) 部品整列方向（または、#1-pin位置）	Refer to Tray dimensions トレイ寸法の項を参照		

TITLE/DESCRIPTION
(E) IC TDA6120 Series
(J)

DRAWING NO. SB- V 2645

SHEET 22

A4
94.8

TENTATIVE PART NO. _____

Semi. Ref. contents for Board ass'y F spec-B243
半導体実装関連情報 F 仕

SCALE FOR MICROFILM 50 0

DRAWING

SONY STANDARD