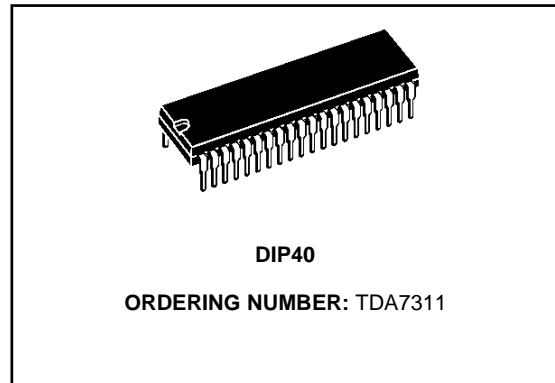


SERIAL BUS CONTROLLED AUDIO PROCESSOR

PRODUCT PREVIEW

- INPUT MULTIPLEXER
 - TWO STEREO DIFFERENTIAL INPUTS
 - TWO STEREO SINGLE ENDED INPUTS
 - ONE MONO DIFFERENTIAL INPUT
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- TREBLE AND BASS CONTROL
- FOUR SPEAKER ATTENUATORS:
 - 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SPI COMPATIBLE SERIAL BUS



Control is accomplished by serial bus microprocessor interface.

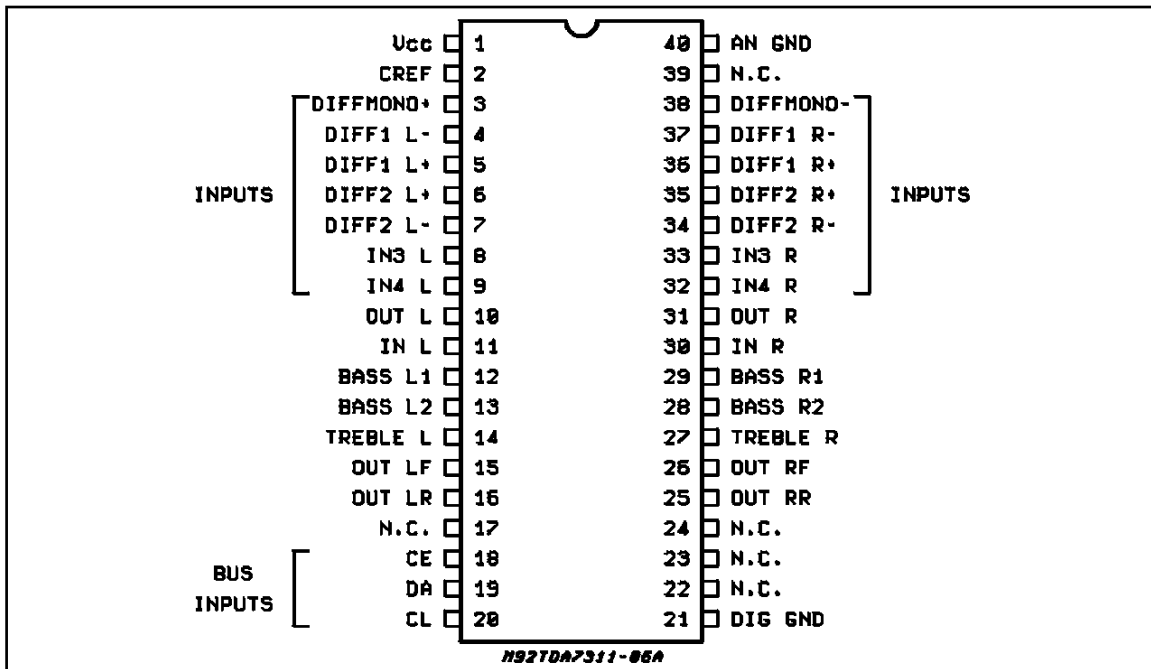
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

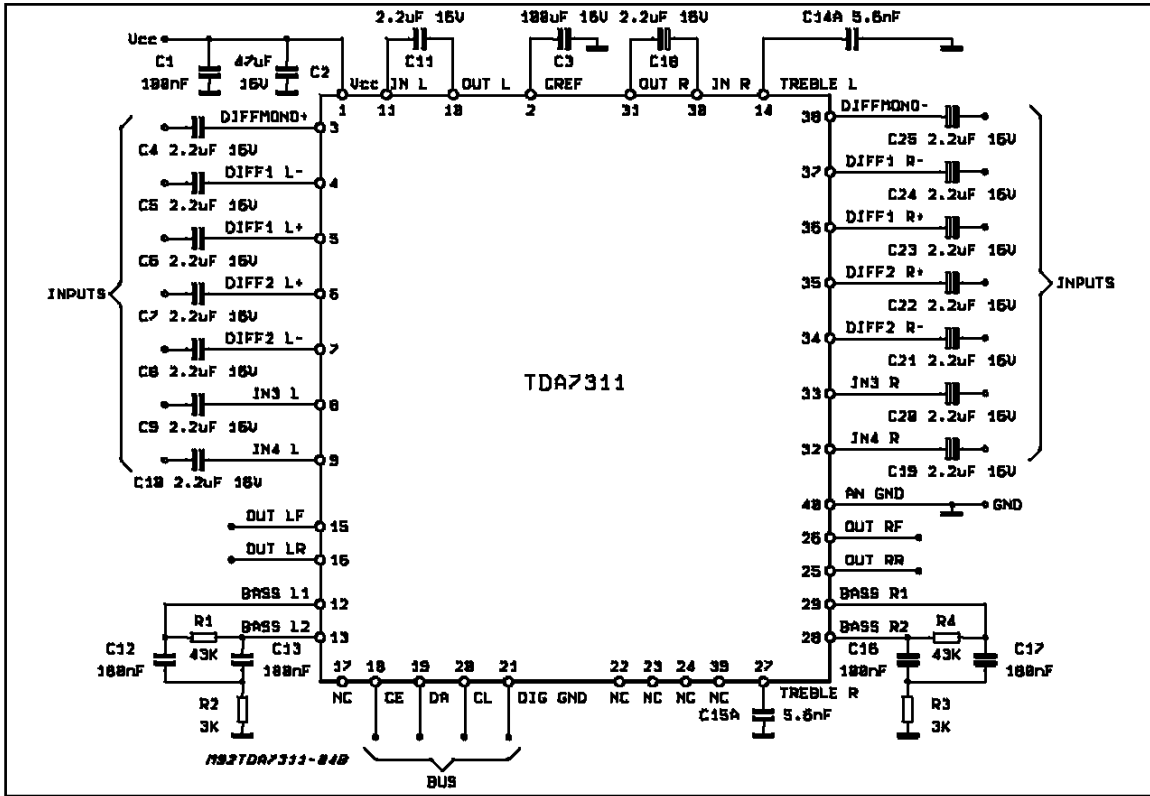
DESCRIPTION

The TDA7311 is a volume, tone (bass and treble) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

PIN CONNECTION (Top view)



TEST CIRCUIT



THERMAL DATA

Symbol	Description	Value	Unit
R _{th j-pins}	Thermal Resistance Junction-pins	max 85	°C/W

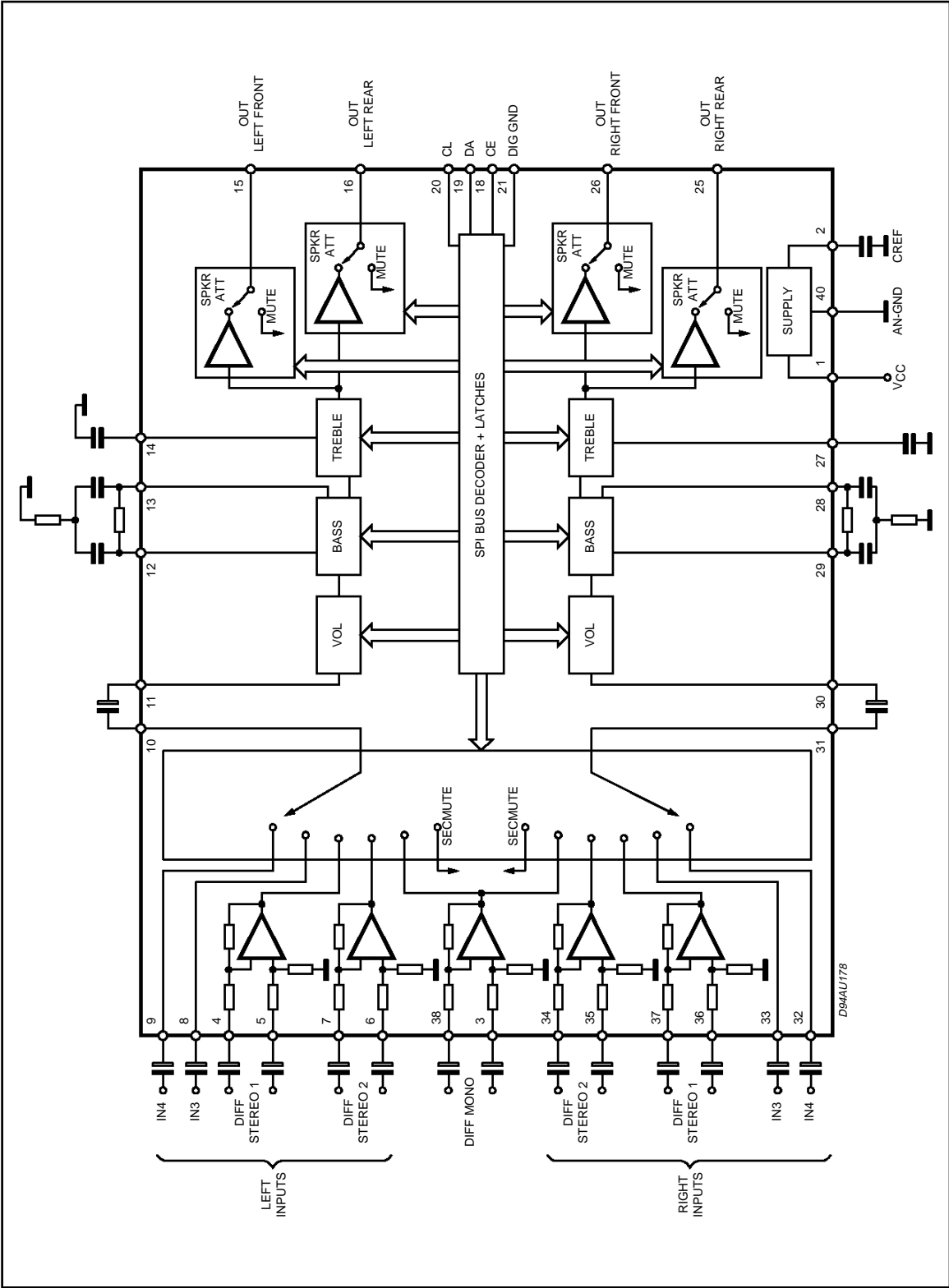
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Operating Supply Voltage	11.2	V
T _{op}	Operating Temperature Range	-40 to 85	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _S	Supply Voltage	8	10	11	V
V _{CL}	Max. input signal handling	2.3			V _{rms}
THD	Total Harmonic Distortion V = 1V _{rms} f = 1KHz		0.01		%
S/N	Signal to Noise Ratio		106		dB
S _C	Channel Separation f = 1KHz		35		dB
BR _{SS}	Volume Control 1.25dB step	-78.75		+11.25	dB
	Treble Control 2dB step	-14		+14	dB
	Bass Control 2dB step	-20		+20	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Mute Attenuation		92		dB

BLOCK DIAGRAM



TDA7311

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 10\text{V}$, $R_L = 10\text{K}\Omega$, $R_G = 600\Omega$, $G_V = 0\text{dB}$, $f = 1\text{KHz}$ unless otherwise specified) (refer to the test circuit)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

SUPPLY

V_S	Supply Voltage		8	10	11	V
I_S	Supply Current			15	20	mA
SVR	Ripple Rejection		55	80		dB

INPUT SELECTORS

R_{II}	Input Resistance	Single Ended inputs	30	50	70	$\text{K}\Omega$
		Differential Inputs	10	20		$\text{K}\Omega$
V_{CL}	Clipping Level	Single Ended Inputs	2.3	2.8		V_{rms}
		Differential Inputs	4.6	5.6		V_{rms}
CMRR	Common Mode Rejection	Differential Inputs		65		dB
INS	Input Separation (2)		70	90		dB
R_L	Output Load resistance		2			$\text{K}\Omega$
C_L	Output Load capacitance				1	nF
R_O	Output Impedance			15	50	Ω
G_{IN}	Input Gain	Single Ended Inputs	-1	0	1	dB
		differential Inputs	-7	-6	-5	dB

VOLUME CONTROL

R_{IN}	Input Resistance		15	30		$\text{k}\Omega$
G_R	Control Range	Max. Attenuation		-75		dB
		Max. Gain		+11.25		dB
A_{STEP}	Step Resolution			1.25		dB
E_A	Attenuation Set Error	$A_V = +11.25$ to -20dB	-1.25	0	1.25	dB
		$A_V = -20$ to -60dB	-3		2	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps		0	3.0	mV
		From 0dB to A_{Vmax}		1	10.0	mV
V_{imax}	Max. Input Voltage		2.3	2.8		V_{rms}

SPEAKER ATTENUATORS

A_R	Control Range			37.5		dB
A_{step}	Step Resolution			1.25		dB
E_A	Attenuation set error				1.5	dB
V_{DC}	DC Steps	adjacent att. steps		0		mV
		from 0 to mute		1		mV

BASS CONTROL (1)

	Control Range			± 20		dB
	Step Resolution			2		dB
	Attenuation / Gain set error		-2.0		2.0	dB

TREBLE CONTROL (1)

	Control Range			± 14		dB
	Step Resolution			2.0		dB
	Attenuation / Gain set error		-1.0	0	1.0	dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

AUDIO OUTPUTS

	Output Voltage	d = 0.3%	2.3	2.8		Vrms
	Output Load Resistance		2			K Ω
	Output Load Capacitance				10	nF
	Output resistance			25	75	Ω
	DC Voltage Level		4.6	5.0	5.4	V

GENERAL

e _{NO}	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB Single Ended all gains = 0dB Diff. Inputs		4 5 10	15 30	μ V μ V μ V
S/N	Signal to Noise Ratio	all gains = 0dB; V _O = 1Vrms Single Ended Differential Inputs		106 100		dB dB
d	Distortion	V _{IN} = 1Vrms		0.01		%
Sc	Channel Separation left/right		70	95		dB
	Total Tracking error	A _V = 0 to -20dB A _V = -20 to -60 dB A _V = 0dB to 11.25dB		0 0 0	1 2 1	dB dB dB
	Output Attenuation	Mute Condition (3)	80	90		dB

BUS INPUTS

V _{IL}	Input Low Voltage				1	V
V _{IH}	Input High Voltage		3			V

Notes:

- (1) Bass and Treble response see attached diagram (fig.17). The center frequency and quality of the resonance behaviour can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network
- (2) The selected input is grounded thru the 2.2 μ F capacitor.
- (3) Condition obtained programming: mute on speaker attenuators (1X111111) followed by selection of SECMUTE (1XXXX111).

APPLICATION INFORMATION

SERIAL BUS INTERFACE

The serial bus interface is compatible to SPI bus systems.

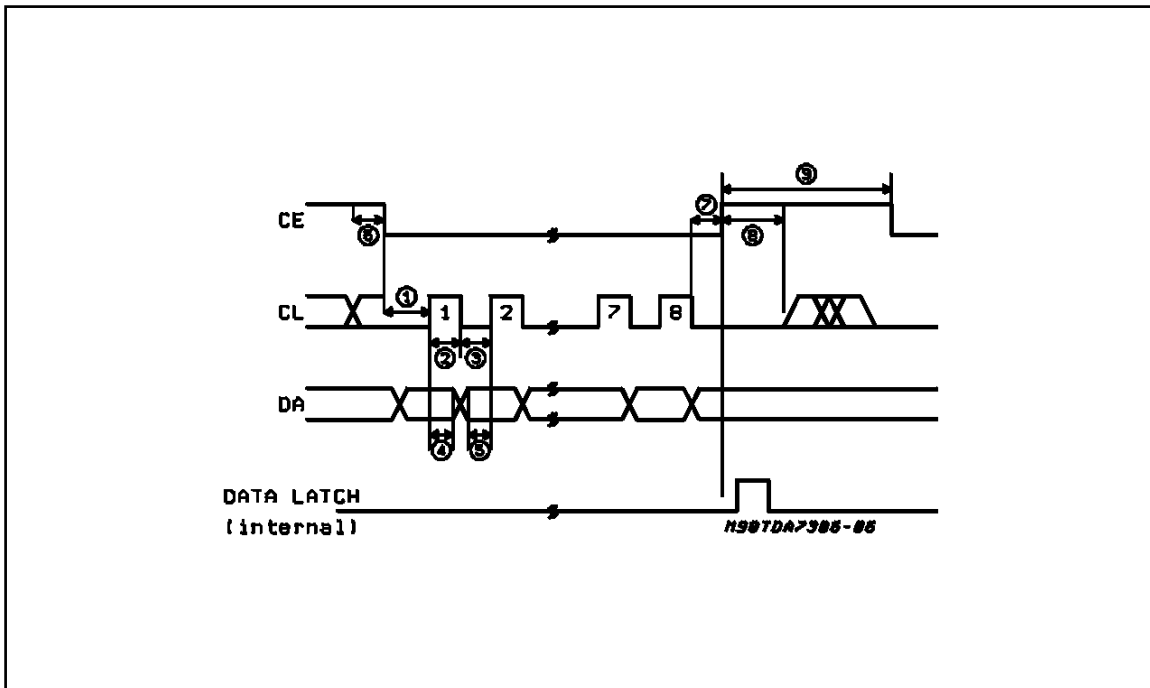
During the LOW state of the chip enable signal (CE) the data on pin DA are clocked into the shift register at the LOW to HIGH transition of the clock signal CL.

At the LOW to HIGH transition of the CE signal the content of the internal shift register is stored into the addressed latches.

The transmission is separated into bytes with 8 bit according to the data specification of the audio-processor. After every byte a positive slope of the CE signal has to be generated in order to store the data byte.

A special clock counter enables the latch of the data byte only, if exactly 8 clocks were present during the LOW state of the CE signal. This results in a high immunity against spikes on the clock line and avoids a storage of wrong databytes.

Figure 1: BUS Timing



Nr.	Parameter	Min.	Max.	Units
	Clock Frequency		250	KHz
1	CE Lead time	4		μs
2	Clock High Time	2		μs
3	Clock Low Time	2		μs
4	Data Hold Time	1.8		μs
5	Data Setup Time	1.8		μs
6	Clock Setup Time	0		μs
7	CE lagtime	0		μs
8	Clock Hold Time	6		μs
9	CE High Time	6		μs

STATUS AFTER POWER-ON RESET

Volume	-78.75dB
Speaker	Mute
Audio Switch	Mute
Bass	-20dB
Treble	-14dB

SOFTWARE SPECIFICATION

Data Bytes

FIRST BYTE

MSB							LSB	Function
0	0	0	0	X	X	X	X	VOL ATTENUATION
0	1	0	0	X	X	X	X	VOL GAIN
0	0	1	0	X	X	X	X	BASS
0	1	1	0	X	X	X	X	TREBLE
0	0	0	1	X	X	X	X	ATT RF (speaker)
0	1	0	1	X	X	X	X	ATT RR (speaker)
0	0	1	1	X	X	X	X	ATT LF (speaker)
0	1	1	1	0	X	X	X	ATT LR (speaker)
0	1	1	1	1	X	X	X	AUDIO SWITCH

SECOND BYTE

VOLUME ATTENUATION

MSB					LSB			
1	X	B2	B1	B0	A2	A1	A0	Volume 1.25dB Steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5.00
					1	0	1	-6.25
					1	1	0	-7.50
					1	1	1	-8.75
1	X	B2	B1	B0				Volume 10dB Steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SOFTWARE SPECIFICATION (continued)
VOLUME GAIN

MSB					LSB			1.25dB STEPS
1	X	X	X	0	0	0	0	0.00
1	X	X	X	0	0	0	1	1.25
1	X	X	X	0	0	1	0	2.50
1	X	X	X	0	0	1	1	3.75
1	X	X	X	0	1	0	0	5.00
1	X	X	X	0	1	0	1	6.25
1	X	X	X	0	1	1	0	7.50
1	X	X	X	0	1	1	1	8.75
1	X	X	X	1	0	0	0	10.00
1	X	X	X	1	0	0	1	11.25

SPEAKER ATTENUATION

MSB					LSB			1.25dB STEPS
1				0	0	0	0	0
1				0	0	1		-1.25
1				0	1	0		-2.50
1				0	1	1		-3.75
1				1	0	0		-5.00
1				1	0	1		-6.25
1				1	1	0		-7.50
1				1	1	1		-8.75
								10dB STEPS
1	X	0	0	0				0
1	X	0	0	1				-10
1	X	0	1	0				-20
1	X	0	1	1				-30
1	X	1	1	1	1	1	1	MUTE

AUDIO SWITCH

MSB					LSB			INPUT
1	X	X	X	X	0	0	0	MONO
1	X	X	X	X	0	0	1	DIFF1
1	X	X	X	X	0	1	0	DIFF2
1	X	X	X	X	0	1	1	IN3
1	X	X	X	X	1	0	0	IN4
1	X	X	X	X	1	1	1	SECMUTE

SOFTWARE SPECIFICATION (continued)
TREBLE

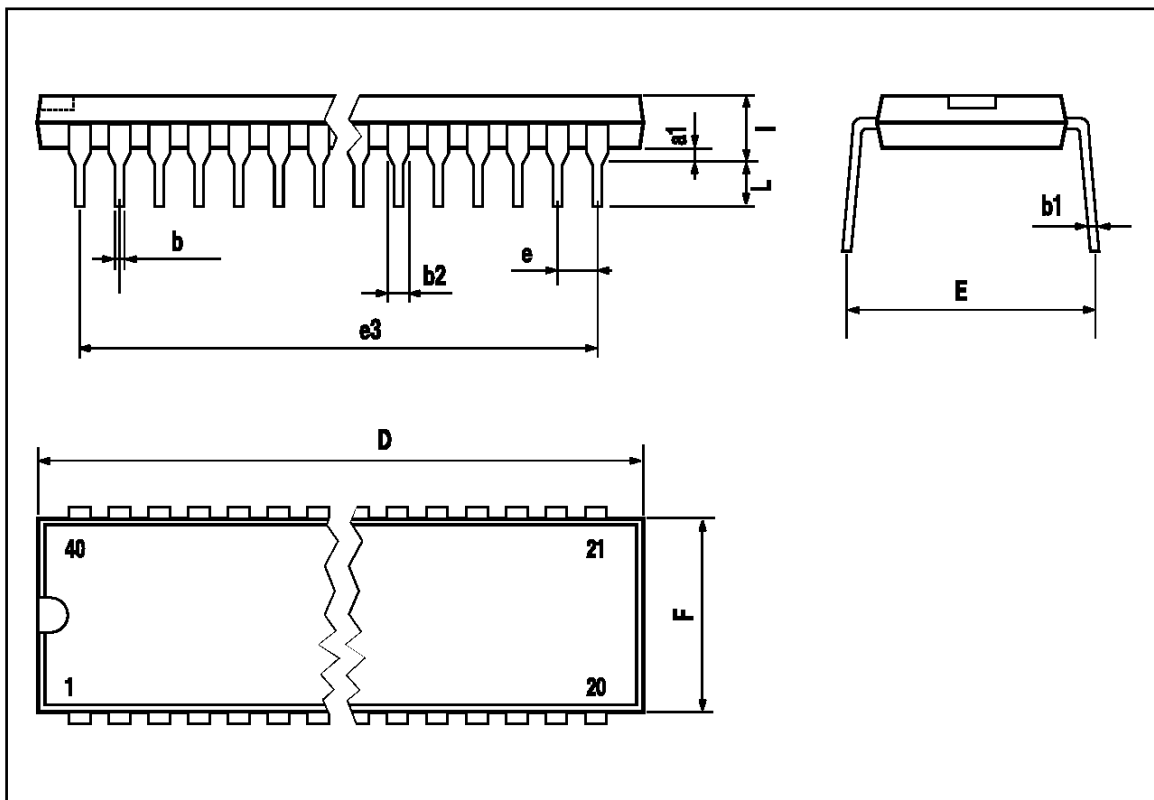
MSB				LSB				2dB STEPS
1	X	X	X	0	1	1	1	14
1	X	X	X	0	1	1	0	12
1	X	X	X	0	1	0	1	10
1	X	X	X	0	1	0	0	8
1	X	X	X	0	0	1	1	6
1	X	X	X	0	0	1	0	4
1	X	X	X	0	0	0	1	2
1	X	X	X	0	0	0	0	0
1	X	X	X	1	0	0	0	-0
1	X	X	X	1	0	0	1	-2
1	X	X	X	1	0	1	0	-4
1	X	X	X	1	0	1	1	-6
1	X	X	X	1	1	0	0	-8
1	X	X	X	1	1	0	1	-10
1	X	X	X	1	1	1	0	-12
1	X	X	X	1	1	1	1	-14

BASS

MSB				LSB				2dB STEPS
1	X	X	1	1	1	1	1	-20
1	X	X	1	1	0	0	1	-18
1	X	X	1	1	0	0	0	-16
1	X	X	1	0	1	1	1	-14
1	X	X	1	0	1	1	0	-12
1	X	X	1	0	1	0	1	-10
1	X	X	1	0	1	0	0	-8
1	X	X	1	0	0	1	1	-6
1	X	X	1	0	0	1	0	-4
1	X	X	1	0	0	0	1	-2
1	X	X	1	0	0	0	0	0
1	X	X	0	0	0	0	0	0
1	X	X	0	0	0	0	1	2
1	X	X	0	0	0	1	0	4
1	X	X	0	0	0	1	1	6
1	X	X	0	0	1	0	0	8
1	X	X	0	0	1	0	1	10
1	X	X	0	0	1	1	0	12
1	X	X	0	0	1	1	1	14
1	X	X	0	1	0	0	0	16
1	X	X	0	1	0	0	1	18
1	X	X	0	1	1	1	1	20

DIP40 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1993 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.