

TDC1020

High-Speed Monolithic A/D Converter

10-Bit, 20 Msps

Features

- 10-bit resolution
- 20 Msps conversion rate
- Overflow flag
- Sample-and-hold circuit not required
- TTL digital interface
- Selectable output format

Applications

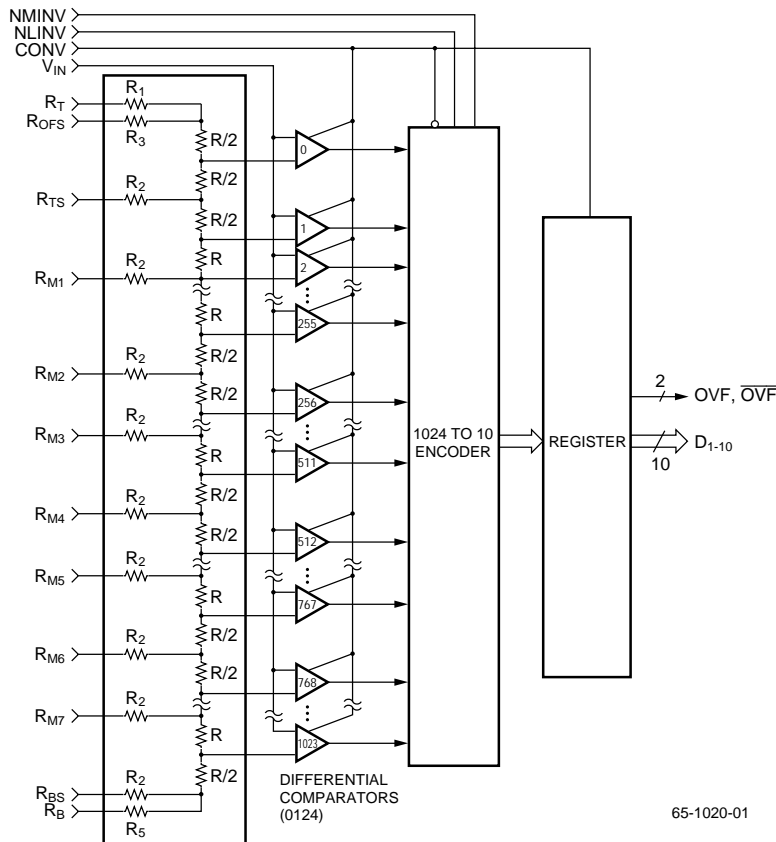
- Medical imaging systems
- Video data conversion
- Radar data conversion
- High-speed data acquisition
- Process control

Description

The TDC1020 is a 20 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting a video signal into a stream of 10-bit digital words.

All outputs of the device are TTL compatible, and will provide the conversion in unsigned magnitude, or two's complement format, and either inverted or noninverted. An output signal indicating overflow condition is also provided for added flexibility. All digital inputs to the device are TTL compatible.

Block Diagram



65-1020-01

Functional Description

General Information

The TDC1020 is a flash analog-to-digital (A/D) converter in which each of the 1024 comparators has one input biased at one of the transition points of the transfer function and all of the other comparator inputs are connected to the analog input signal. The output of the comparator array is sometimes referred to as a “thermometer” code as all of comparators biased at voltages more positive than the input voltage will be off and the rest will be on. The thermometer code from the comparator array is encoded into an 11-bit code (10 data bits plus an overflow bit). The format of the code that is encoded is determined by the format controls NMINV and NLINV so that the data presented to the output latches is in binary, two’s complement or inverted data format.

Power and Thermal Management

The TDC1020 operates from two supply voltages, +5.0V and -5.2V. The bulk of the current drawn by the positive supply is returned through the negative supply, however, the positive supply should be referenced to digital ground (DGND) and the negative supply to analog ground (AGND). All power and ground pins must be connected. The maximum power is drawn at the lower limit of the operating temperature range. When the device is being operated at elevated temperatures, the power dissipation drops, however, thermal management will then be a consideration. The TDC1020 is rated for operation in a 70°C ambient temperature in still air.

The power dissipation decreases with increasing temperature. Fairchild specifies the absolute maximum I_{EE} and I_{CC} specifications in the Electrical Characteristics Table. The worst case conditions are $V_{CC} = 5.25V$, $V_{EE} = -5.5V$ and the case temperature equal to 0°C. The case temperature of 0°C is, however, a transient condition since the device immediately warms up and decreases its power dissipation, upon power up. For typical steady state power dissipation as a function of ambient temperature, please see Figure 7.

It is possible to relax the temperature requirements of the device by providing adequate heat sinking.

Reference

The bias voltages for the comparator array are provided by use of a serial chain of 1024 equal-valued resistors across which the reference voltage is applied. Seven equally separated mid-point adjustment taps are provided to allow the user to optimize the integral linearity of the device. In addition, there are sense leads on the top and bottom of the resistor chain which allow the user to minimize the offset and gain errors of the device. It is recommended that the user drive RM2, RM4 and RM6 in order to obtain optimal device performance. One method for driving the references is

shown in Figure 7. The reference top and reference bottom sources must be able to source or sink the reference current and since noise on these leads will lead to inaccurate conversions, they should be bypassed with a capacitor to AGND. There are in addition 4 more reference taps, the use of which is not required to obtain 0.1 % integral linearity. It is recommended that these pins be left open (no connection).

Format Control

There are two inputs provided on the TDC1020 which control the output format of the device. When NMINV is connected to a logic LOW, the MSB is inverted. When NLINV is connected to a logic LOW D2 through D10 will be inverted. By using various combinations of these commands the user can select any of the following output data formats: binary, inverted binary, two’s complement, inverted two’s complement. The Output Coding Table shows the output formats generated for each of the control states.

Convert

The analog input to the TDC1020 is sampled at a time t_{STO} after the rising edge of the CONV signal. The output data from the 1024 comparators is encoded into the proper format and the final result is transferred to the output latches on the next rising edge. This timing is shown in the Timing Diagram (Figure 1). Note that there are minimum LOW and HIGH requirements of the CONV signal (t_{PWH} , t_{PWL}) which must be met for proper device operation. In addition, the performance is generally improved if the CONV signal is LOW for as long as possible. A circuit which provides an optimized waveshape CONV signal to the TDC1020 is shown on Figure 7.

Analog Input

The analog input to the TDC1020 has an equivalent circuit shown in Figure 2. It should be noted that the major component of the input impedance is capacitance, and the input range is 4Vp-p. A low-impedance driving circuit is recommended for the TDC1020 to obtain good dynamic performance. All analog inputs to the TDC1020 must be connected to insure proper operation of the A/D converter.

Outputs

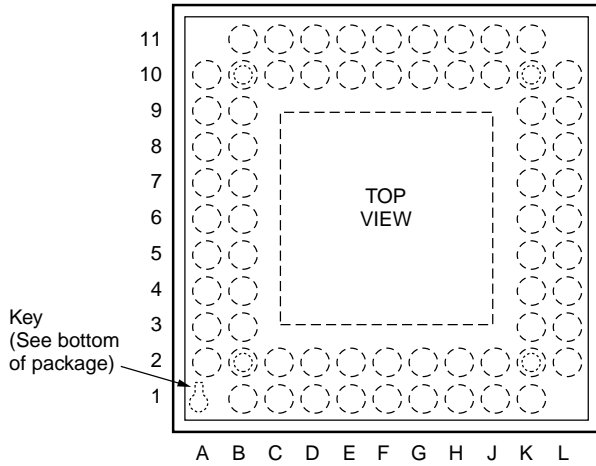
The data and overflow outputs of the TDC1020 are TTL compatible, capable of driving four low power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CONV signal. New data becomes valid after a maximum delay time. t_D .

No Connects

There are several pins labelled No Connect (NC) which have no electrical connection to the chip. These pins should be connected to AGND for best noise performance.

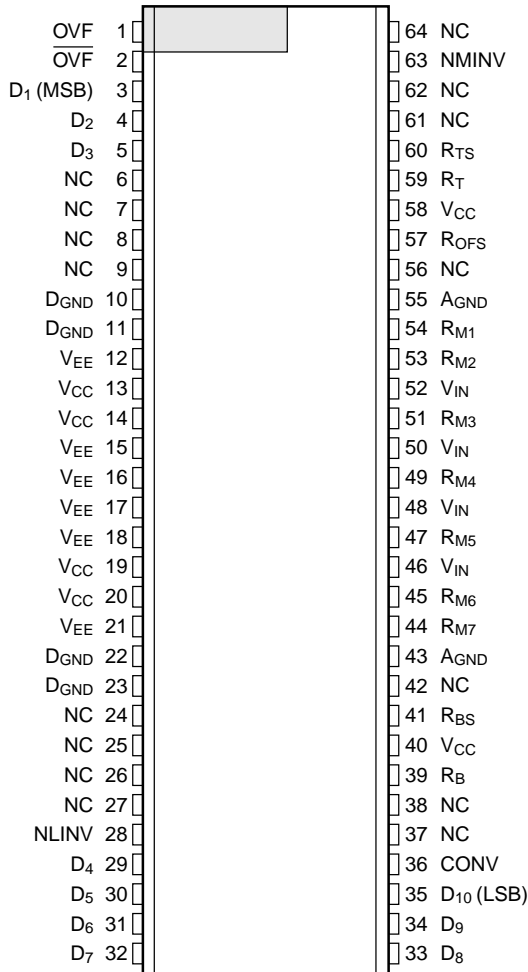
Pin Assignments

68 Pin Grid Array



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	R _{M7}	F10	D ₇	K4	V _{CC}
A3	AGND	B10	NC	F11	D ₈	K5	V _{CC}
A4	R _{M2}	B11	R _{BS}	G1	D ₃	K6	V _{EE}
A5	R _{M3}	C1	R _{TS}	G2	D ₂	K7	V _{EE}
A6	NC	C2	R _T	G10	NC	K8	V _{CC}
A7	NC	C10	R _B	G11	D ₆	K9	NC
A8	R _{M5}	C11	V _{CC}	H1	NC	K10	D _{GND}
A9	R _{M6}	D1	NC	H2	NC	K11	NC
A10	AGND	D2	NC	H10	D ₄	L2	D _{GND}
B1	V _{CC}	D10	D ₁₀ LSB	H11	D ₅	L3	V _{EE}
B2	R _{OFS}	D11	CONV	J1	NC	L4	NC
B3	R _{M1}	E1	OVF	J2	NC	L5	V _{EE}
B4	V _{IN}	E2	NMINV	J10	NC	L6	V _{EE}
B5	V _{IN}	E10	NC	J11	NLINV	L7	V _{CC}
B6	R _{M4}	E11	D ₉	K1	NC	L8	V _{EE}
B7	V _{IN}	F1	D ₁ MSB	K2	NC	L9	NC
B8	V _{IN}	F2	OVF	K3	D _{GND}	L10	D _{GND}

64 Pin Hermetic Ceramic DIP



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Pin Descriptions

Pin Name	Ceramic DIP	Pin Grid Array	Type/ Value	Pin Function Description
Power				
VCC	13, 14, 19, 20, 40, 58	K4, K5, L7, K8, C11, B1	5.0V	Positive Supply Voltage
VEE	12, 15, 16, 17, 18, 21	L3, L5, K6, L6, K7, L8	-5.2V	Negative Supply Voltage
DGND	10, 11, 22, 23	L2, K3, L10, K10	0.0V	Digital Ground
AGND	43, 55	A10, A3	0.0V	Analog Ground
Reference				
RT	59	C2	2.0V	Reference Resistor, Top
ROFS	57	B2	2.0V	Overflow Sense
RTS	60	C1	2.0V	Reference Resistor, Top Sense
RM1	54	B3	1.5V ¹	Reference Resistor, 1/8 Tap
RM2	53	A4	1.0V ¹	Reference Resistor, 2/8 Tap
RM3	51	A5	0.5V ¹	Reference Resistor, 3/8 Tap
RM4	49	B6	0.0V ¹	Reference Resistor, 4/8 Tap
RM5	47	A8	-0.5V ¹	Reference Resistor, 5/8 Tap
RM6	45	A9	-1.0V ¹	Reference Resistor, 6/8 Tap
RM7	44	B9	-1.5V ¹	Reference Resistor, 7/8 Tap
RB	39	C10	-2.0V	Reference Resistor, Bottom
RBS	41	B11	-2.0V	Reference Resistor, Bottom Sense
Format Control				
NMINV	63	E2	TTL	Not MSB Invert
NLINV	28	J11	TTL	Not LSB Invert
Convert				
CONV	36	D 11	TTL	Convert
Analog Input				
VIN	46, 48, 50, 52	B8, B7, B5, B4	+2 to -2V	Analog Signal Input
Outputs				
OVF	1	E1	TTL	Overflow
$\overline{\text{OVF}}$	2	F2	TTL	Overflow Complement
D ₁ MSB	3	F1	TTL	Most Significant Bit
D ₂ –D ₉	4–5, 29–34	G2, G1, H10, H11, G11, F10, F11, E11	TTL	
D ₁₀ LSB	35	D10	TTL	Least Significant Bit
No Connects				
NC	6, 7, 8, 9, 24, 25, 26, 27, 37, 38, 42, 56, 61, 62, 64	H2, H1, J2, J1, K1, K2, L4, K9, L9, K11, J10, G10, E10, B10, A7, A6, A2, O2, D1	Open	No Connection

Note:

1. Measured values

Output Coding Table

Input	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1, NLINV = 1	NMINV = 0, NLINV = 0	NMINV = 0, NLINV = 1	NMINV = 1, NLINV = 0
	MSB- LSB IOV			
>2.000V	000000000(1)	111111111(1)	100000000(1)	011111111(1)
>2.000V	000000000(0)	111111111(0)	100000000(0)	011111111(0)
1.996V	000000001(0)	111111110(0)	100000001(0)	011111110(0)
⋮	⋮	⋮	⋮	⋮
0.004V	011111111(0)	100000000(0)	111111111(0)	000000000(0)
0.000V	100000000(0)	011111111(0)	000000000(0)	111111111(0)
-0.004V	100000001(0)	011111110(0)	000000001(0)	111111110(0)
⋮	⋮	⋮	⋮	⋮
-1.996V	111111110(0)	000000001(0)	011111110(0)	100000001(0)
-2.000V	111111111(0)	000000000(0)	011111111(0)	100000000(0)

Note:

1. Input voltages are at code centers.

Timing Diagrams

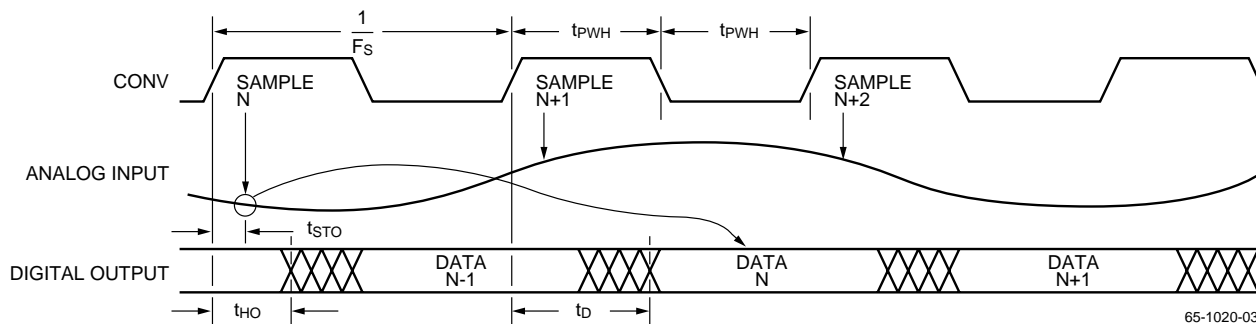


Figure 1. Timing Diagram

Equivalent Circuits

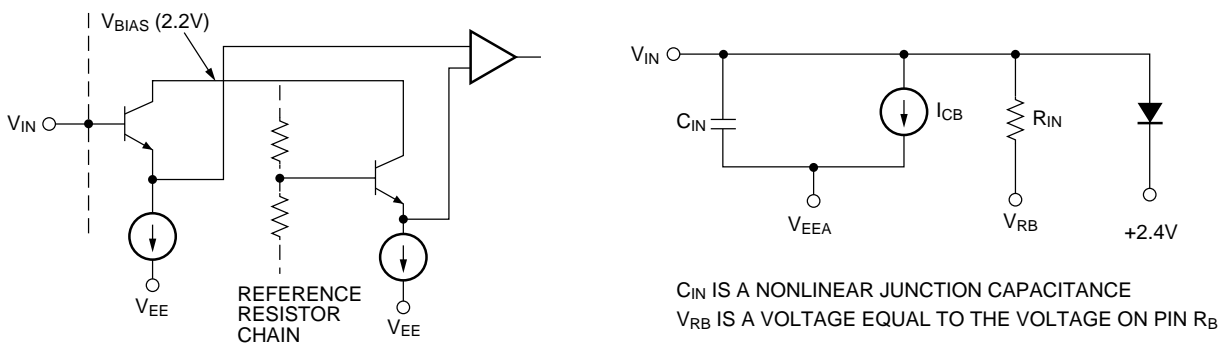


Figure 2. Simplified Analog Input Equivalent Circuits

Equivalent Circuits (continued)

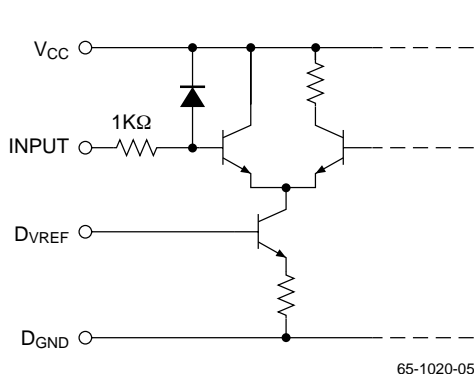


Figure 3. Equivalent Input Circuits
Convert, NMINV, and NLINV

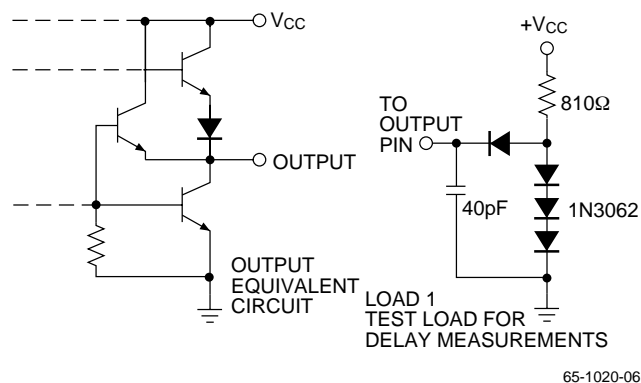


Figure 4. Output Circuits

Absolute Maximum Ratings

(beyond which the device may be damaged)¹

Supply Voltages		Min.	Max.	Unit
VCC (measured to DGND)		-0.5	+6.0	V
VEE (measured to AGND)		+5.0	-6.0	V
AGND (measured to DGND)		-1.0	+1.0	V
Input Voltages				
CONV, NMINV, NLINV (measured to DGND)		-0.5	+5.5	V
VIN (measured to AGND)		VCC	VEE	V
Any reference (measured to AGND)		VCC	VEE	V
VRT (measured to VRB)		-1.0	+4.4	V
Output				
Applied voltage measured to DGND ²		-0.5	+5.5	V
Applied current, externally forced ^{3,4}		-1.0	+6.0	mA
Short-circuit duration (single output in HIGH state to ground)			1	S
Sense lead current		-1.0	1.0	mA
Temperature				
Operating	Ambient	-55	+90	°C
	Junction		+175	°C
Lead, soldering (10 seconds)			+300	°C
Storage		-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Commercial			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
VCC	Positive Supply Voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
VEE	Negative Power Supply Voltage	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
VAGND	Analog Ground Voltage (measured to DGND)	-0.1	0.0	0.1	-0.1	0.0	0.1	V
tPWL	CONV Pulse Width, LOW	22			22			ns
tPWH	CONV Pulse Width, HIGH	18			20			ns
VIL	Input Voltage, Logic LOW			0.8			0.8	V
VIH	Input Voltage, Logic HIGH	2.0			2.0			V
IOL	Output Current, Logic LOW			4.0			4.0	mA
IOH	Output Current, Logic HIGH			-400			-400	μA
VRM2	Reference Tap, 1/4-Scale	0.8	1.0	1.2	0.8	1.0	1.2	V
VRM4	Reference Tap, 1/2-Scale	-0.2	0.0	0.2	-0.2	0.0	0.2	V
VRM6	Reference Tap, 3/4-Scale	-0.8	-1.0	-1.2	-0.8	-1.0	-1.2	V
VRT	Most Positive Reference Voltage	1.8	2.0	2.2	1.8	2.0	2.2	V
VRB	Most Negative Reference Voltage	-1.8	-2.0	-2.2	-1.8	-2.0	-2.2	V
VRT-VRB	Reference Voltage Differential	3.6	4.0	4.4	3.6	4.0	4.4	V
VIN	Input Voltage Range	VRB	±2.0	VRT	VRB	±2.0	VRT	V
TA	Ambient Temperature, C-Grade	0		70				°C
TC	Case Temperature, V-Grade				-55		125	°C

DC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Extended		
			Min.	Max.	Min.	Max.	
ICC	Total Positive Supply Current	VCC = VEE = Max		850		850	mA
IEE	Total Negative Supply Current	VEE = Max		-500		-500	mA
IREF	Reference Current	VRT, VRB = Nom		50		50	mA
RREF	Reference Chain Resistance	VRT, VRB = Nom	80		80		Ohms
RIN	Analog Input Resistance	VRT, VRB = Nom, VIN = VRB	3000		2000		Ohms
CIN	Analog Input Capacitance	VRT, VRB = Nom, VIN = VRB		300		300	pF
ICB	Input Constant Bias	VEE = Max		2		3	mA
IL	Input Current, Logic LOW	VCC = Max, VI = 0.5V		50		50	μA
I _{IH}	Input Current, Logic HIGH	VCC = Max, VI = 2.4V		100		100	μA
I _I	Input Current, Maximum	VCC = Max, VI = 5.25V		100		100	μA
VOL	Output Voltage, Logic LOW	VCC = Min, IOL = Max		0.5		0.5	V
VOH	Output Voltage, Logic HIGH	VCC = Min, IOL = Max	2.4		2.4		V
IOS	Short-Circuit Output Current	VCC = Max, output HIGH, one pin to ground, one second duration max.		-35		-35	mA
CI	Digital Input Capacitance	TA = 25°C, f = 1 MHz		15		15	pF

AC Electrical Characteristics

Parameter		Test Conditions	Temper				Units
			Commercial		Extended		
			Min	Max	Min	Max	
F _S	Maximum Conversion Rate	V _{EE} = Min, V _{CC} = Min	20		20		MSPS
t _{STO}	To Sampling Time Offset	V _{EE} = Max, V _{CC} = Max	3	17	3	17	ns
t _D	Output Delay	V _{EE} = Max, V _{CC} = Max		37		43	ns
t _{HO}	Output Hold Time	V _{EE} = Max, V _{CC} = Max	5		5		ns

Performance Characteristics

Parameter		Test Conditions	Typ.	Temperature Range				Units
				Commercial		Extended		
				Min.	Max.	Min.	Max.	
ELI	Linearity Error, Integral	Reference Taps Open	±0.1		±0.2		±0.2	%
ELI	Linearity Error, Integral	Reference Taps Adjusted	±0.05		±0.1		±0.1	%
ELD	Linearity Error, Differential	Reference Taps Open	±0.05		±0.1		±0.1	%
CS	Code Size			5	225	5	225	% Nominal
EOT	Offset Error, Top				25		30	mV
EOB	Offset Error, Bottom				-30		-35	mV
TCO	Offset Error Tempco				±10		±20	µA/°C
t _{TR}	Transient Response	Full-Scale Input Step, Settling to ±32 LSBs	20		30		30	ns
BW	Full-Power Bandwidth	Full-Scale Input	10	5				MHz
SNR ¹	Signal-to-Noise Ratio	F _{IN} = 1.0 MHz	60	58		58		dB
		F _{IN} = 2.0 MHz	59	56		56		dB
		F _{IN} = 5.0 MHz	56	52		52		dB
		F _{IN} = 8.0 MHz	54	47				dB
		F _{IN} = 10.0 MHz	52	43				dB
SINAD ¹	Signal-to-Noise and Distortion	F _{IN} = 1.0 MHz	59	55		52		dB
		F _{IN} = 2.0 MHz	58	52		52		dB
		F _{IN} = 5.0 MHz	54	48		45		dB
		F _{IN} = 8.0 MHz	48	41				dB
		F _{IN} = 10.0 MHz	43	39				dB
THD ¹	Total Harmonic Distortion	F _{IN} = 1.0 MHz	-66	-58		-53		dBc
		F _{IN} = 2.0 MHz	-64	-56		-53		dBc
		F _{IN} = 5.0 MHz	-58	-52		-46		dBc
		F _{IN} = 8.0 MHz	-50	-43				dBc
		F _{IN} = 10.0 MHz	-44	-41				dBc

Performance Characteristics (continued)

Parameter	Test Conditions	Typ.	Temperature Range				Units	
			Commercial		Extended			
			Min.	Max.	Min.	Max.		
SFDR ¹	Spurious-Free Dynamic Range	$F_{IN} = 1.0 \text{ MHz}$	70	53		53		dB
		$F_{IN} = 2.0 \text{ MHz}$	68	54		54		dB
		$F_{IN} = 5.0 \text{ MHz}$	63	48		48		dB
		$F_{IN} = 8.0 \text{ MHz}$	55	40				dB
		$F_{IN} = 10.0 \text{ MHz}$	48	35				dB
EAP	Aperture Error				50		50	ps
DP	Differential Phase	$F_S = 4 \times \text{NTSC Subcarrier}$, Reference Taps Adjusted	0.3		0.5			Degree
DG	Differential Gain	$F_S = 4 \times \text{NTSC Subcarrier}$, Reference Taps Adjusted	0.8		1.0			%

Note:

1. $F_S = 20\text{Mpsps}$ Reference Taps Adjusted, $V_{CC} = V_{EE} = \text{Nom}$, $T_A = 25^\circ\text{C}$

Typical Performance Curves

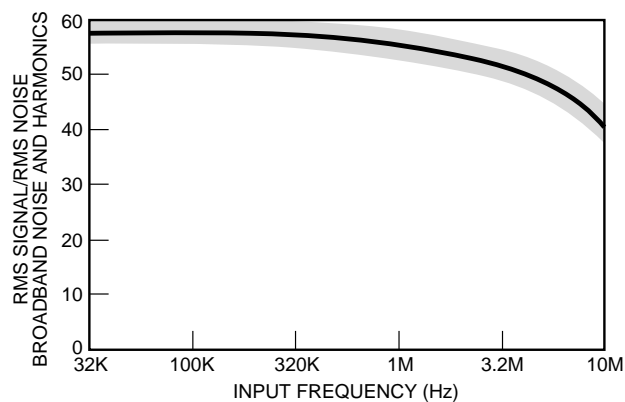
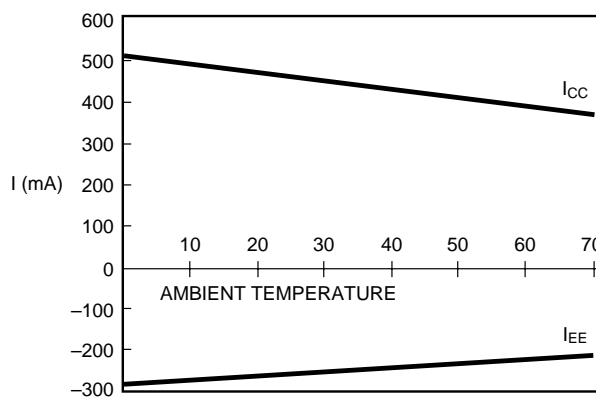


Figure 5. Typical SNR vs. Input Frequency



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Figure 6. Typical Supply Current vs. Temperature

Applications Discussion

Calibration

Calibration of the TDC1020 consists of adjusting the reference taps so that the converters integral linearity, gain and offset errors are minimized. To minimize the offset errors the sense leads must be used properly. The sense leads are not designed to carry very much current (<1mA) and should therefore be used in a feedback loop to a high-impedance input such as that shown in Figure 7. When a circuit similar to that in Figure 7 is used for generating the reference voltages, calibration can be achieved with the following procedure:

1. Apply an input to the input amplifier which is 1/2 LSB less than full-scale (A/D input = 1.998V) and adjust the gain so that the output of the A/D is toggling between full-scale and one LSB below full-scale (1111111111 and 1111111110 for binary conversions).
2. Apply an input to the input amplifier which is 1/2 LSB greater than zero-scale (A/D input = 1.998V) and adjust V_{RB} via the V_{RG} pot so that the output of the A/D is toggling between 0 and 1 (0000000000 and 0000000001 for binary conversions).

The A/D converter will now be calibrated to provide accurate conversions throughout its input range. To optimize the integral linearity of the device set up the “Subtractive Ramp Test” described in the TRW Applications Note TP-30, *Understanding Flash A/D Converter Terminology*, then adjust the mid-point taps to minimize the bow in the error curve.

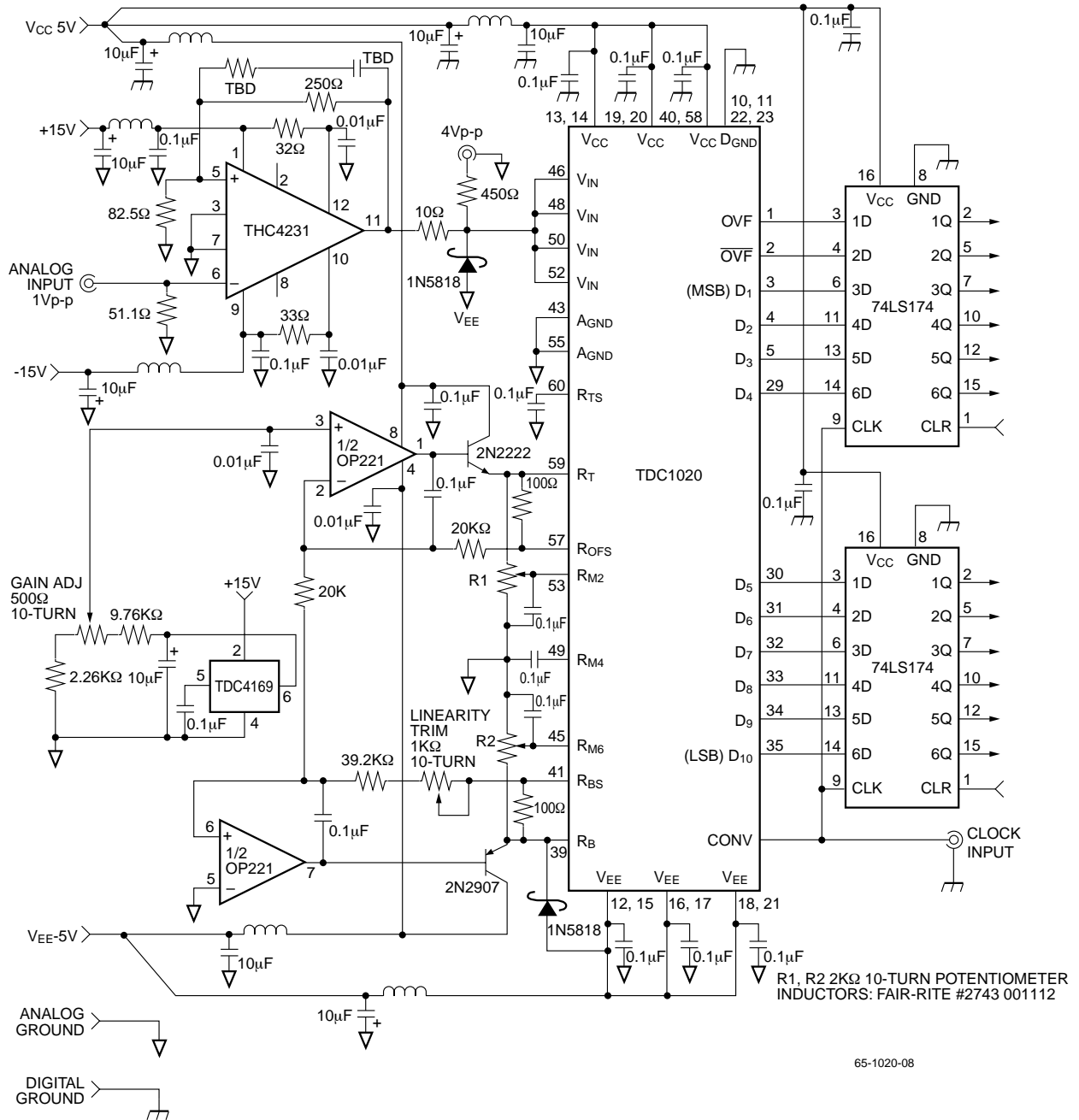
Typical Interface

A Typical Interface Circuit is shown of the TDC1020 in Figure 7. The analog input amplifier, a THC4231, is used to directly drive the A/D converter. This amplifier is set up to have a gain of four and will provide the recommended +2 to -2V input signal to the TDC1020 when it has a 1Vp-p input signal. All four analog input pins are connected in parallel to decrease the parasitic inductance. An LM313 is used to provide a stable reference voltage which is buffered by a dual op-amp, generating V_{RT} and V_{RB} . Both op-amps have their outputs buffered by an emitter follower to decrease the output impedance seen by the reference resistor chain. To minimize noise coupling into the reference resistor chain, bypass capacitors have been added, bypassing the reference taps to ground.

Since capacitive coupling from the digital signals to the analog input will adversely affect the converter performance, careful attention to board layout is recommended.

As is true with most bipolar integrated circuits, the substrate of the TDC1020 (V_{EE}); must be the most negative potential applied. This rule applies for all conditions of temperature, signal level and power supply sequencing. In many systems, the voltage reference generators and input driving amplifier are powered from voltages greater than the +5 and -5.2V of the TDC1020. Whenever this situation occurs, it is always possible for the V_{EE} inputs of the TDC1020 to be positive with respect to the V_{IN} or V_{RG} inputs when power supplies are cycled ON and OFF.

To protect the TDC1020 from latch-up due to substrate bias, Fairchild recommends the use of a 1N5818 Schottky diode connected between V_{EE} and V_{IN} and another between V_{EE} and V_{RG} with the anode of each diode connected to V_{EE} . The diodes prevent V_{IN} and V_{RT} from going more than 0.4V more negative than V_{EE} . This protection circuit is shown in Figure 7.



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Figure 7. Typical Interface Circuit

Notes:

Notes:

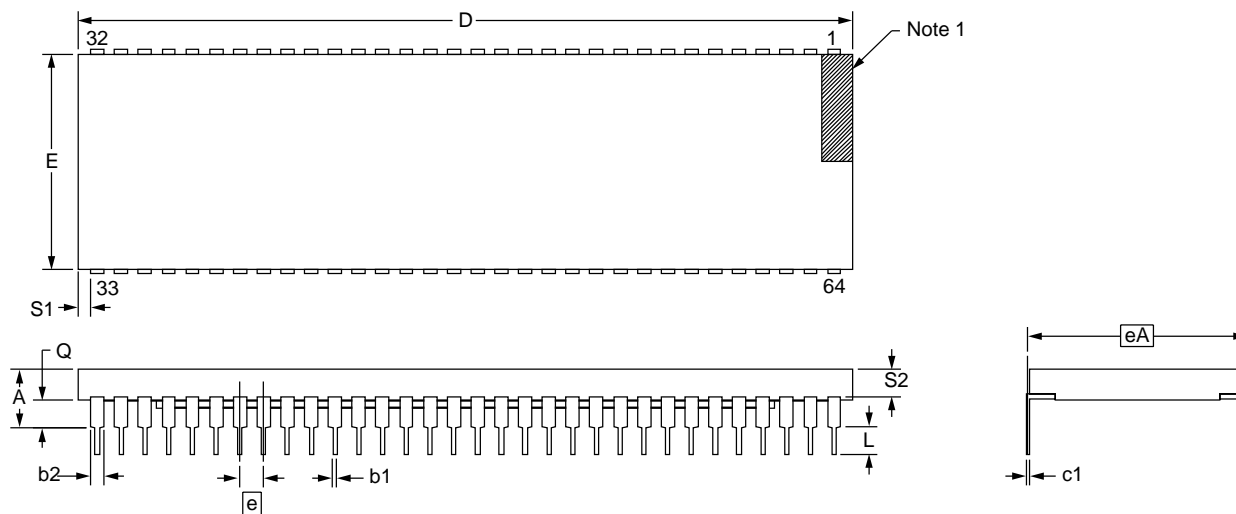
Mechanical Dimensions

64 Lead Bottombraze Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.125	.200	3.18	5.08	
B1	.015	.023	.38	.58	7
B2	.040	.065	1.02	1.65	2
C1	.008	.015	.20	.38	7
D	3.110	3.240	80.00	82.30	
E	.790	.810	20.07	20.57	
e	.100 BSC		2.54 BSC		4, 8
eA	.900 BSC		22.86 BSC		6
L	.125	.175	3.18	4.45	
Q	.050	.100	1.27	2.54	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 32, 33, and 64 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within $\pm .010$ (.25mm) of its exact longitudinal position relative to pins 1 and 64.
5. Applies to all four corners (leads number 1, 32, 33, and 64).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Sixty-two spaces.



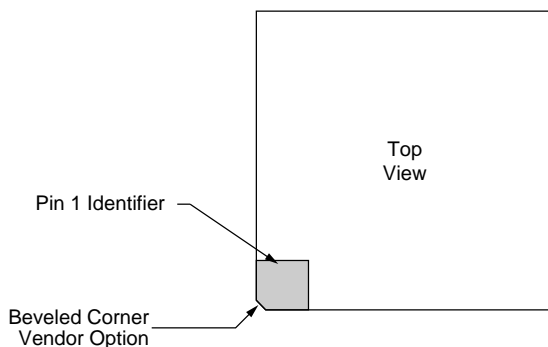
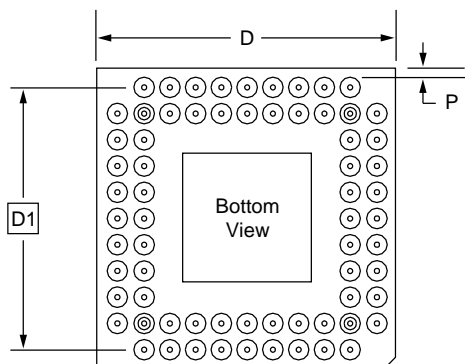
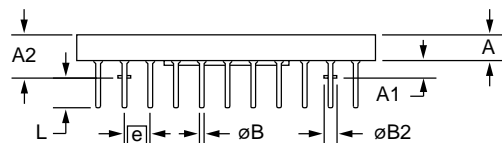
Mechanical Dimensions (continued)

68 Pin PGA

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.025	.060	0.64	1.52	
A2	.105	.180	2.67	4.57	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1020J1C	STD-T _A = 0°C to 70°C	Commercial	64 Lead Bottombraze Ceramic DIP	1020J1C
TDC1020J1V	EXT-T _C = -55°C to 125°C	Military	64 Lead Bottombraze Ceramic DIP	1020J1V
TDC1020G0C	STD-T _A = 0°C to 70°C	Commercial	68 Pin PGA	1020G0C
TDC1020G0V	EXT-T _C = -55°C to 125°C	Military	68 Pin PGA	1020G0V

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.