

TMC1103

Triple Video A/D Converter with Clamps

8-Bit, 50MSPS

Features

- 8-bit resolution
- 50 MspS conversion rate
- Low power: 100mW per channel @ 20 MspS
- Integral track/hold
- Independent Input Clamps
- Independent clock inputs
- Integral and differential linearity error 0.5 LSB
- Differential phase 0.7 degree
- Differential gain 1.8%
- Single +5V power supply
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing (composite and Y-C)
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

Description

Incorporated into the TMC1103 are three analog-to-digital (A/D) converters, each with an independent clock, reference voltage and input clamp. Analog signals are converted to Triple 8-bit digital words at sample rates up to 50 MspS (Megasamples per second) per channel.

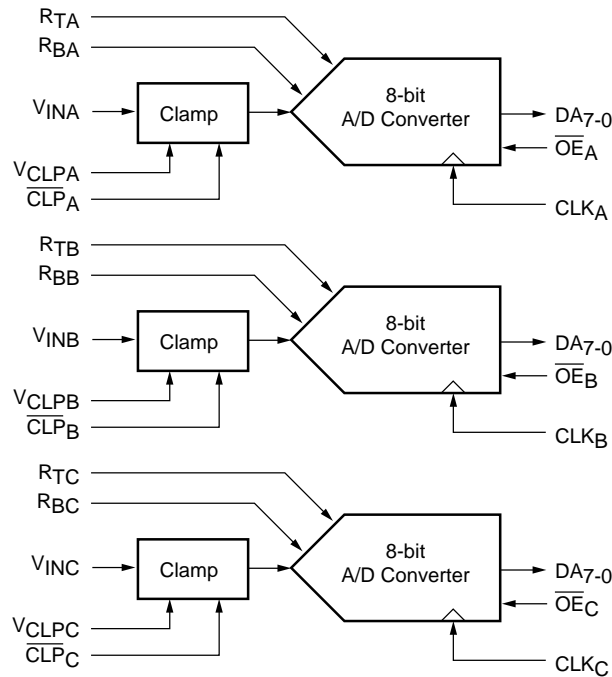
Integral Track/Hold circuits deliver excellent performance on signals with full-scale spectral components up to 12 MHz. Innovative two-step conversion architecture and

submicron CMOS technology reduce typical power dissipation to 100 mW per converter.

Power is derived from a single +5 Volt power supply. Outputs are three-state outputs and TTL/CMOS-compatible.

TMC1103 package is a 80-lead Metric Quad Flat Pack (MQFP). Performance specifications are guaranteed from 0°C to 70°C.

Block Diagram



65-1103-01

Circuit Function

Within the TMC1103 are three 8-bit A/D converters, each employing two-step architecture to convert an analog input to a digital output at rates up to 50 Msps. Input signals are held in integral track/hold stages during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CLK_X cycle.

Each of the three converters function identically. In the following descriptions 'X' refers to a generic input/output or clock where 'X' is equivalent to A, B or C.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

Analog Input and Voltage References

Each A/D accepts analog signals in the range R_{BX} to R_{TX} into digital data. Input signals outside this range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range AGND to V_{DDA} .

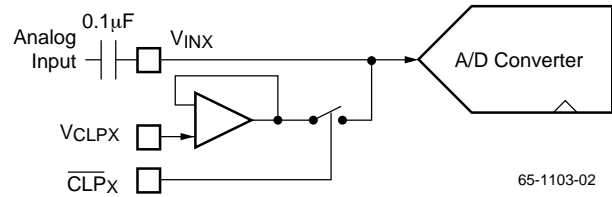
Input range is very flexible and extends from the +5 Volt power supply to ground. Nominal input range is 2 Volts, extending from 0.6V to 2.6V. Characterization and performance is specified over this range. However, the part will function with a full-scale range from 1.0V to 5.0V. A smaller input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance.

External voltage reference sources are connected to the RTX and RBX pins. RBX can be grounded. Within each A/D converter is a reference resistor ladder comprising 255 resistors that are accessed by the TMC1103 comparators. RTX is connected to the top of the ladder, RBX to the bottom. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Input Clamps

A clamp circuit is connected to the input pin V_{INX} of each of the three A/D converters. With \overline{CLPX} LOW, the input pin is clamped to the voltage at V_{CLPX} . If \overline{CLPX} is HIGH, the input pin is high impedance. Clamping adds an offset voltage to an AC coupled signal to adjust this signal's amplitude to the A/D converter input voltage range.

The analog input is corrected through a $0.1\mu F$ capacitor to V_{INX} . The source impedance of the analog source should be less than 50 Ohms. Current pulses through the capacitor over several clamp cycles until the voltage across the capacitor equals the difference between V_{CLPX} and the voltage at the analog source during the clamping period. When the switch is open, the voltage on the coupling capacitor is added to the analog input, producing a DC offset input signal.



Input Clamp Circuit

Digital Inputs and Outputs

Sampling of the applied input signal occurs on the falling edge of the CLK_X signal (Figure 1). Output data is delayed by $2\frac{1}{2} CLK_X$ cycles and is valid following the rising edge of CLK_X . Previous output data remains valid for t_{HO} (Output Hold Time). New data becomes valid t_D (Output Delay Time) after this rising edge of CLK_X .

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, the output limits at 00h or FFh, as appropriate.

Table 1. A/D Output Coding

Input Voltage	Output
$RTX + 1 \text{ LSB}$	FF
RTX	FF
$RTX - 1 \text{ LSB}$	FE
...	...
$RBX + 128 \text{ LSB}$	80
$RBX + 127 \text{ LSB}$	7F
...	...
$RBX + 1 \text{ LSB}$	01
RBX	00
$RBX - 1 \text{ LSB}$	00

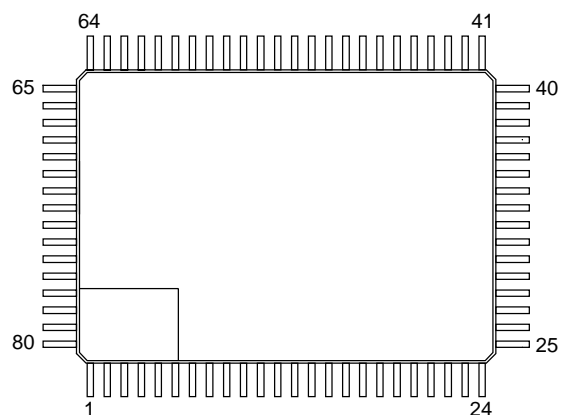
Note: $1 \text{ LSB} = (RTX - RBX) / 255$

The outputs of the TMC1103 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL loads. An Output Enable control, \overline{OE}_X , places the A/D outputs in a high-impedance state when HIGH. The outputs are enabled when \overline{OE}_X is LOW.

Power and Ground

The TMC1103 operates from a single +5 Volt power supply. For optimum performance, an analog ground plane should be placed under the TMC1103 the AGND and DGND pins should be connected to the system analog ground plane.

Pin Assignments

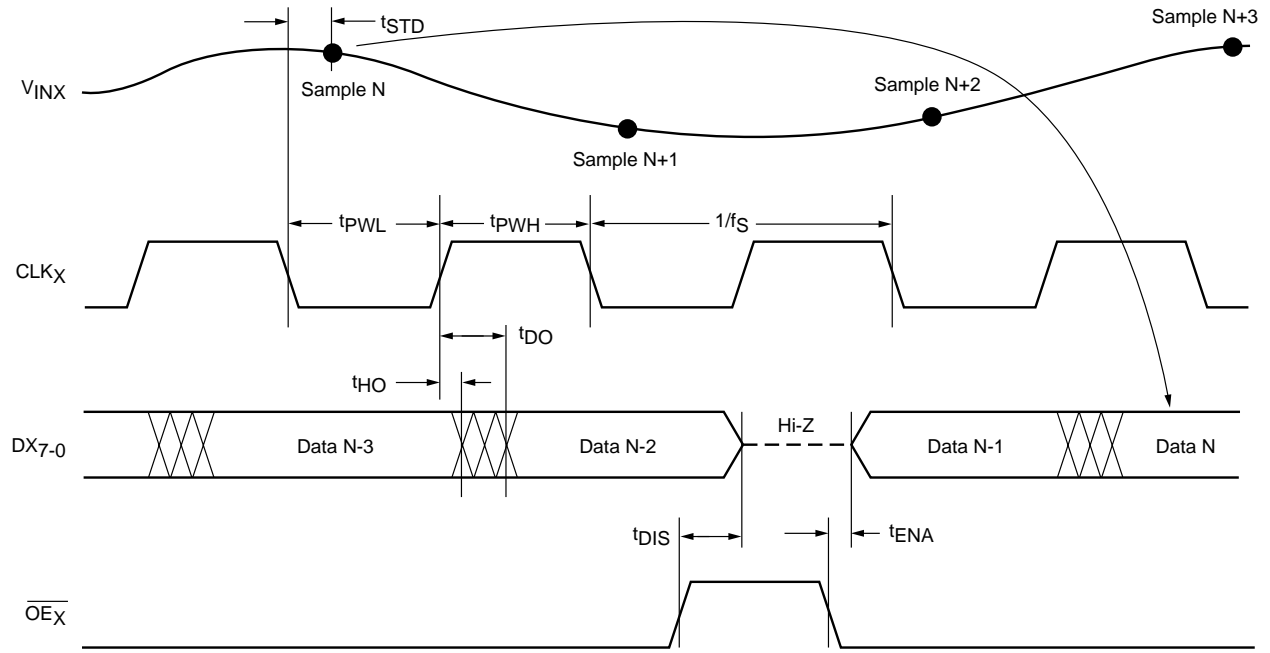


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Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	21	DGND	41	DC7	61	VDD
2	DA5	22	DGND	42	OE _C	62	OE _B
3	DA6	23	NC	43	VDD	63	DB7
4	DA7	24	NC	44	VDD	64	DB6
5	OE _A	25	DGND	45	CLK _C	65	DB5
6	VDD	26	DGND	46	NC	66	DB4
7	VDD	27	VDD	47	VDDA	67	DB3
8	NC	28	CLP _A	48	VINC	68	DB2
9	CLK _A	29	CLP _B	49	AGND	69	DB1
10	NC	30	CLP _C	50	RTC	70	DB0
11	VDDA	31	NC	51	RBC	71	DGND
12	VINA	32	DGND	52	RBB	72	DGND
13	AGND	33	DGND	53	RTB	73	NC
14	RTA	34	DC0	54	AGND	74	DGND
15	RBA	35	DC1	55	VINB	75	DGND
16	VCLPA	36	DC2	56	VDDA	76	DA0
17	VCLPB	37	DC3	57	NC	77	DA1
18	VCLPC	38	DC4	58	CLK _B	78	DA2
19	DGND	39	DC5	59	NC	79	DA3
20	DGND	40	DC6	60	VDD	80	DA4

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
A/D Converters			
VINA, VINB, VINC	12, 55, 48	RTX to RBX	Analog Inputs. The input voltage conversion range lies between the voltage applied to the RTX and RBX pins.
RTA, RTB, RTC	14, 53, 50	2.6V	Reference Voltage, Top Inputs. DC voltages applied to RTA, RTB and RTC define highest value of VINX.
RBA, RBB, RBC	15, 52, 51	0.6V	Reference Voltage, Bottom Inputs. DC voltages applied to RBA, RBB and RBC define lowest value of VINX.
CLKA, CLKB, CLKC	9, 58, 45	CMOS	Clock Inputs. CMOS-compatible. VINX is sampled on the falling edge of CLKX.
DA7-0	4, 3, 2, 80, 79, 78, 77, 76	CMOS/TTL	Data outputs, Converter A (D7 = MSB). Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
DB7-0	63, 64, 65, 66, 67, 68, 69, 70	CMOS/TTL	Data outputs, Converter B (D7 = MSB). Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
DC7-0	41, 40, 39, 38, 37, 36, 35, 34	CMOS/TTL	Data outputs, Converter C (D7 = MSB). Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
$\overline{OE}A, \overline{OE}B, \overline{OE}C$	5, 62, 42	CMOS	Output Enable Inputs. CMOS-compatible. When LOW, the A/D output is enabled. When HIGH, the output is in a high-impedance state.
Clamps			
VCLPA, VCLPB, VCLPB	16, 17, 18	RTX to RBX	Clamp Reference Voltage. One reference for each clamp. A VINX input is clamped to VCLPX when $\overline{CLP}X$ is low.
$\overline{CLP}A, \overline{CLP}B, \overline{CLP}C$	28, 29, 30	CMOS	Clamp Pulse Inputs. One input for each A/D clamp. When $\overline{CLP}X$ is low, the VINX input is clamped to the VCLPX clamp voltage.
Power			
VDDA	11, 47, 56	+5V	Analog Supply Voltage. +5 Volt power inputs. These should come from the same power source and be decoupled to AGND.
VDD	6, 7, 27, 28, 29, 30, 43, 44, 60, 61	+5V	Digital Supply Voltage. +5 Volt power inputs. These should come from the same power source and be decoupled to AGND.
AGND	13, 49, 54	0.0V	Analog Ground. Ground connections. These pins should be connected to the system analog ground plane.
DGND	16, 17, 18, 19, 20, 21, 22, 25, 26, 32, 33, 71, 72, 74, 75	0.0V	Digital Ground. Ground connections. These pins should be connected to the system analog ground plane.
No Connect			
N/C	1, 8, 10, 23, 24, 31, 46, 57, 59, 73	open	Not Connected.



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Figure 1. Timing

Equivalent Circuits and Threshold Levels

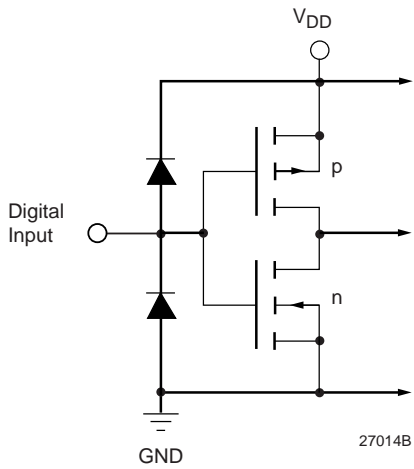


Figure 2. Equivalent Digital Input Circuit

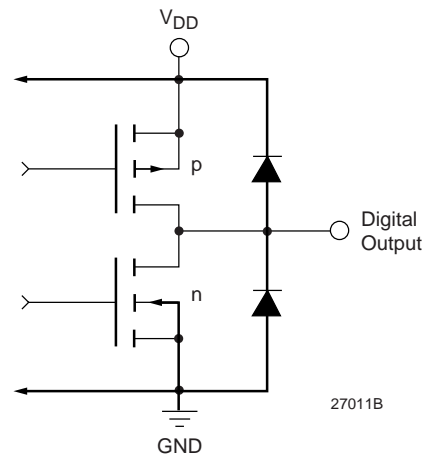


Figure 3. Equivalent Digital Output Circuit

Equivalent Circuits and Threshold Levels (continued)

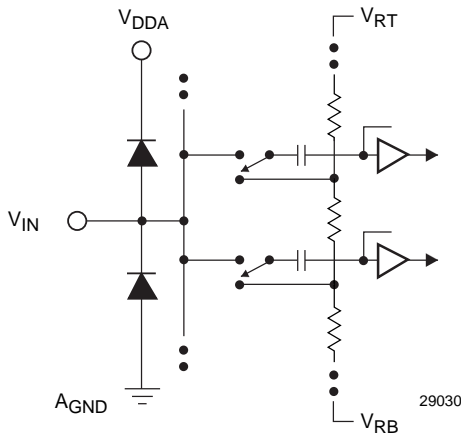


Figure 4. Equivalent Analog Input Circuit

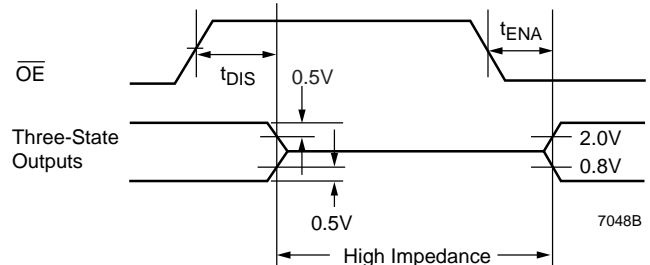


Figure 5. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltages					
VDDA	Measured to AGND	-0.5		+7.0	V
VDD	Measured to DGND	-0.5		+7.0	V
VDDA	Measured to VDD	-0.5		+0.5	V
AGND	Measured to DGND	-0.5		+0.5	V
Digital Inputs					
Applied Voltage	Measured to DGND	-0.5		VDD + 0.5	V
Forced current		-10.0		+10.0	mA
Analog Inputs					
Applied Voltage	Measured to AGND	-0.5		VDDA+0.5	V
Forced current		-10.0		+10.0	mA
Digital Outputs					
Applied voltage	Measured to DGND	-0.5		VDD + 0.5	V
Forced current		-6.0		+6.0	mA
Short circuit duration	Single output in HIGH state to ground)			1 second	
Temperature					
Operating, ambient		-20		110	°C
Junction				+150	°C
Lead, soldering	10 seconds			+300	°C
Vapor Phase soldering	1 minute			+220	°C
Storage		-65		+150	°C
Electrostatic Discharge	EIAJ test method			±150	V

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
VDD, VDDA	Power Supply Voltage	4.75	5.0	5.25	V
AGND	Analog Ground (Measured to DGND)	-0.1	0	0.1	V
VRTX	Reference Voltage, Top		2.6	VDDA	V
VRBX	Reference Voltage, Bottom	0	0.6		V
VRTX-VRBX	Reference Voltage Differential	1.0	2.0	5.0	V
VINX	Analog Input Range	VRB		VRT	V
VCLPX	Clamp Reference Voltage, 50Ω max source	0			V
VIH	Input Voltage, Logic HIGH	0.7 VDD		VDD	V
VIL	Input Voltage, Logic LOW	GND		0.3 VDD	V
IOH	Output Current, Logic HIGH			-4.0	mA
IOL	Output Current, Logic LOW			4.0	mA
TA	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ ¹	Max.	Units
IDD	Power Supply Current ¹	CLOAD = 35pF, fCK = fs (3 A/Ds)				
		fs = 20 Msps		70	90	mA
		fs = 40 Msps		94	120	mA
		fs = 50 Msps		105	135	mA
IDDQ	Power Supply Current, Quiescent	VDD = VDDA = Max.				
		CLKX = LOW		29	55	mA
		CLKX = HIGH		45	65	mA
PD	Total Power Dissipation ¹	CLOAD = 35pF, fCK = fs (3 A/Ds)				
		fs = 20 Msps		300	470	mW
		fs = 40 Msps		425	630	mW
		fs = 50 Msps		490	710	mW
CAI	Input Capacitance, Analog	CLKX = LOW		4		pF
		CLKX = HIGH		12		pF
RIN	Input Resistance		500			kΩ
RREF	Reference Resistance		200	270	340	Ω
ICB	Input Current, Analog				±5	μA
IiH	Input Current, HIGH	VDD = Max., VIN = VDD			±5	μA
IiL	Input Current, LOW	VDD = Max., VIN = 0V			±5	μA
IOZH	Hi-Z Output Leakage Current, Output HIGH	VDD = Max., VIN = VDD			±5	μA
IOZL	Hi-Z Output Leakage Current, Output LOW	VDD = Max., VIN = VDD			±5	μA
IOS	Short-Circuit Current				35	mA

Electrical Characteristics (continued)

Parameter		Conditions	Min.	Typ ¹	Max.	Units
VOH	Output Voltage, HIGH	I _{OH} = -2.5mA	3.5			V
		I _{OH} = Max.	2.4			V
VOL	Output Voltage, LOW	I _{OL} = Max.			0.4	V
CDI	Digital Input Capacitance			4	10	pF
CDO	Digital Output Capacitance			10		pF

Note:

1. Typical values with V_{DD} = V_{DDA} = Nom and T_A = Nom, Maximum values with V_{DD} = V_{DDA} = Max. and T_A = Min.

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
fS	Conversion Rate	TMC1103-20			20	MSPS
		TMC1103-40			40	MSPS
		TMC1103-50			50	MSPS
tPWH	CLKX Pulsewidth, HIGH	TMC1103-20	14			ns
		TMC1103-40	14			ns
		TMC1103-50	13			ns
tPWL	CLKX Pulsewidth, LOW	TMC1103-20	8			ns
		TMC1103-40	8			ns
		TMC1103-50	7			ns
EAP	Aperture Error		30		ps	
tSTO	Sampling Time Offset	1	2	5	ns	
tSTS	Sampling Time Skew		150	400	ps	
tCPW	Clamp Pulse Width ¹	+20 < T _A < +70°C	2			μS
tCDLY	Clamp Delay Time		100	300	ns	
tHO	Output Hold Time	CLOAD = 15pF	9			ns
tDO	Output Delay Time			14		ns
tENA	Output Enable Time			27		ns
tDIS	Output Disable Time			42		ns

System Performance Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
ELI	Integral Linearity Error, Independent	$V_{RT} = 2.6V$		± 0.5		LSB
ELD	Differential Linearity Error	$V_{RB} = 0.6V$		± 0.5		LSB
BW	Bandwidth ¹	TMC1203-20			10	MHz
		TMC1203-40			12	MHz
		TMC1203-50			12	MHz
EOT	Offset Voltage, Top ($R_T - V_{IN}$ for most positive code transition)	$V_{RT} = 2.6V, V_{RB} = 0.6V$	-40		80	mV
EOB	Offset Voltage, Bottom ($R_B - V_{IN}$ for most negative code transition)	$V_{RT} = 2.6V, V_{RB} = 0.6V$	-95		-30	mV
OFFCL	Offset Voltage, Clamp				± 20	mV
dg	Differential Gain	$f_S = 14.3\text{Msp}$ s NTSC 40 IRE Mod Ramp $V_{DDA} = +5.0V, T_A = 25^\circ\text{C}$ $V_{RT} = 2.6V, V_{RB} = 0.6V$		1.8		%
dp	Differential Phase	$f_S = 14.3\text{Msp}$ s NTSC 40 IRE Mod Ramp $V_{DDA} = +5.0V, T_A = 25^\circ\text{C}$ $V_{RT} = 2.6V, V_{RB} = 0.6V$		0.7		deg
XTALK	Channel Crosstalk	$f_N = 5.0\text{MHz}$		45		dB
SNR	Signal-to-Noise Ratio	$f_S = 20\text{Msp}$ s, $V_{RT} = 2.6V, V_{RB} = 0.6V$				
		$f_N = 1.24\text{MHz}$		46		dB
		$f_N = 2.48\text{MHz}$		46		dB
		$f_N = 6.98\text{MHz}$		45		dB
		$f_N = 10.0\text{MHz}$		45		dB
		$f_S = 40\text{Msp}$ s, $V_{RT} = 2.6V, V_{RB} = 0.6V$				
		$f_N = 1.24\text{MHz}$		42		dB
		$f_N = 6.98\text{MHz}$		41		dB
		$f_N = 12.0\text{MHz}$		40		dB
		$f_S = 50\text{Msp}$ s, $V_{RT} = 2.6V, V_{RB} = 0.6V$				
		$f_N = 1.24\text{MHz}$		40		dB
		$f_N = 6.98\text{MHz}$		40		dB
		$f_N = 12.0\text{MHz}$		40		dB

System Performance Characteristics (continued)

Parameter		Conditions	Min.	Typ.	Max.	Units
SFDR	Spurious-Free Dynamic Range	f _S = 20Msps, V _{IN} = 2V p-p				
		f _N = 1.24MHz		53		dB
		f _N = 2.48MHz		48		dB
		f _N = 6.98MHz		44		dB
		f _N = 10.0MHz		40		dB
		f _S = 40Msps, V _{IN} = 2V p-p				
		f _N = 1.24MHz		49		dB
		f _N = 6.98MHz		44		dB
		f _N = 12.0MHz		38		dB
		f _S = 50Msps, V _{IN} = 2V p-p				
		f _N = 1.24MHz		46		dB
		f _N = 6.98MHz		40		dB
		f _N = 12.0MHz		37		dB

Notes:

1. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.
2. Values shown in Typ. column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25°C.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
5. Characteristics specified for V_{RT} = 2.6V, V_{RB} = 0.6V.

Typical Performance Characteristics

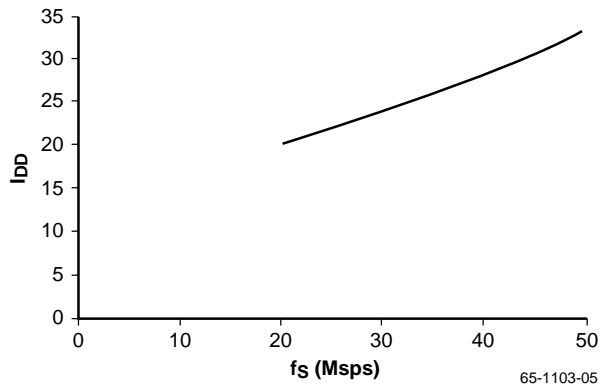


Figure 6. Typical IDD vs fs (Single A/D)

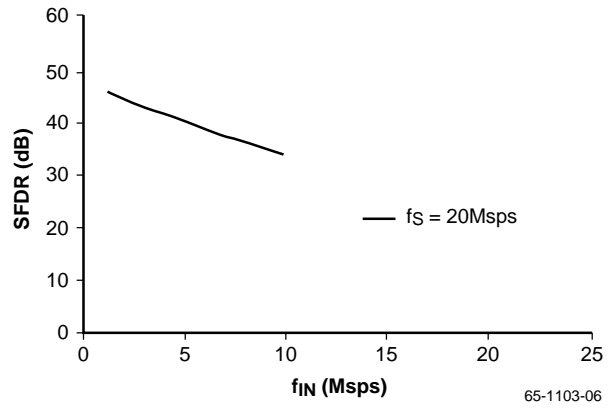


Figure 7. Typical SFDR vs fIN

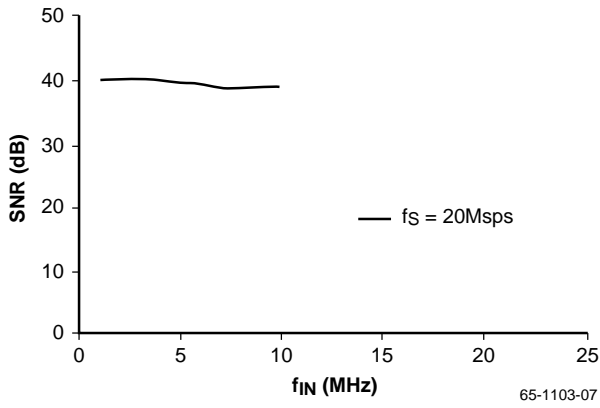


Figure 8. Typical SNR vs fIN

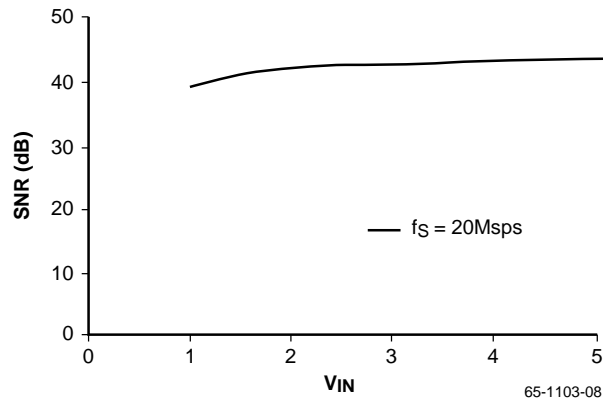


Figure 9. Typical SNR vs Full Scale Input Range

Application Notes

The circuit in Figure 10 employs a band-gap reference to generate a variable R_{TX} reference voltages for the TMC1103 as well as a bias voltage to offset the wideband input amplifiers to mid-range. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_{TX} can be adjusted from 0.0 to 2.4 volts while R_{BX} is grounded. Schottky diodes can be used at V_{INX} to restrict the wideband amplifier output to between $-0.3V$ and $V_{DD} + 0.3V$. Diode protection is good practice to limit the analog input voltage at V_{INX} to the safe operating range.

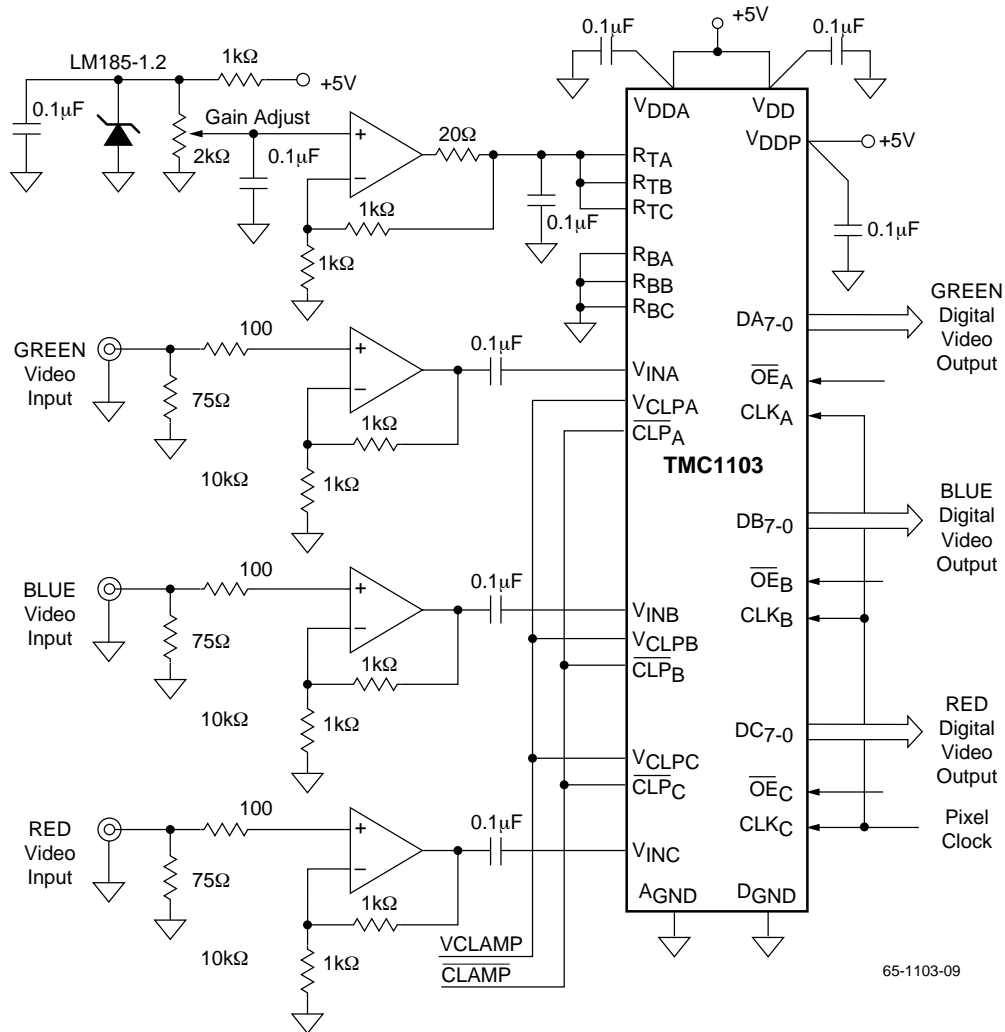


Figure 10. Typical Interface Circuit – High Performance

Grounding

The TMC1103 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DD} and V_{DDA}) come from the same source, and that ground connections ($DGND$ and $AGND$) be made to the analog ground plane, and as close as possible to the device pins. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1103 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_N , R_{TX} , R_{BX}) as short as possible and as far as possible from all digital signals. The TMC1103 should be located close to the analog input connectors.

2. Segregate traces:

- A/D analog
- D/A analog
- Clocks
- Digital

Treat analog inputs as transmission lines. Cleanly route traces over the ground plane bearing in mind that the return currents will flow through the ground plane beneath the traces. Do not route digital traces nearby. A few inches of digital trace less than a few line widths from an analog trace will cross-couple noise into adjacent analog circuits.

3. The power plane for the TMC1103 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the VDD pins. If the power supply for the TMC1103 is the same as that of the system's digital circuitry, power to the TMC1103 should be decoupled with ferrite beads and 0.1 μ F capacitors to reduce noise.
4. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

5. Decoupling capacitors should be applied liberally to VDD pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1 μ F ceramic capacitors. Lead lengths should be minimized.
6. CLK_X should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line, if needed, to eliminate overshoot and ringing.

Related Products

- TMC1175A, TMC1275 8-Bit Video A/D Converters
- TMC1173A, TMC1273 3V, Low-Power 8-Bit Video A/D Converters
- TMC1203 Triple 8-bit A/D Converter
- TMC3003/TMC3503 Triple Video D/A Converters
- TMC2242B/TMC2243/TMC2246A Digital Filters

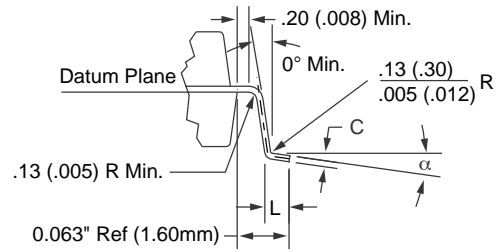
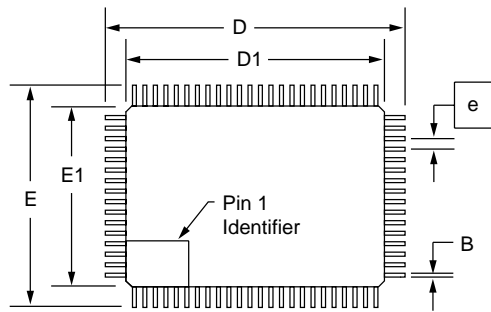
Notes:

Mechanical Dimensions – 80-Lead MQFP Package

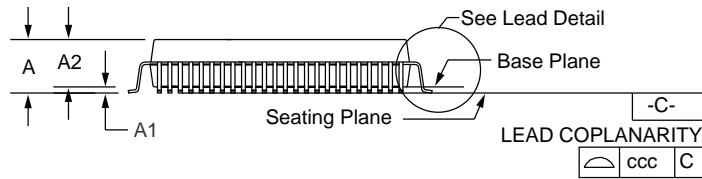
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0315 BSC		.80 BSC		
L	.025	.041	.65	1.03	4
N	80		80		
ND	24		24		
NE	16		16		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Lead Detail



Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1103KLC20	20 Msps	T _A = 0°C to 70°C	Commercial	80-Lead MQFP	1103KLC20
TMC1103KLC40	40 Msps	T _A = 0°C to 70°C	Commercial	80-Lead MQFP	1103KLC40
TMC1103KLC50	50 Msps	T _A = 0°C to 70°C	Commercial	80-Lead MQFP	1103KLC50

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.