

# TMC1203

## Triple Video A/D Converter

### 8-Bit, 50MSPs

#### Features

- 8-bit resolution
- 50 Msps conversion rate
- Low power: 100mW per channel @ 20 Msps
- Integral track/hold
- Independent clock inputs
- Integral and differential linearity error 0.5 LSB
- Differential phase 0.7 degree
- Differential gain 1.8%
- Single +5V power supply
- Three-state TTL/CMOS-compatible outputs
- Low cost

#### Applications

- Video digitizing (composite and Y-C)
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion
- Digital communications

#### Description

Incorporated into the TMC1203 are three analog-to-digital (A/D) converters, each with independent clocks and reference voltages. Analog signals are converted to Triple 8-bit digital words at sample rates up to 50 Msps (Megasamples per second) per channel.

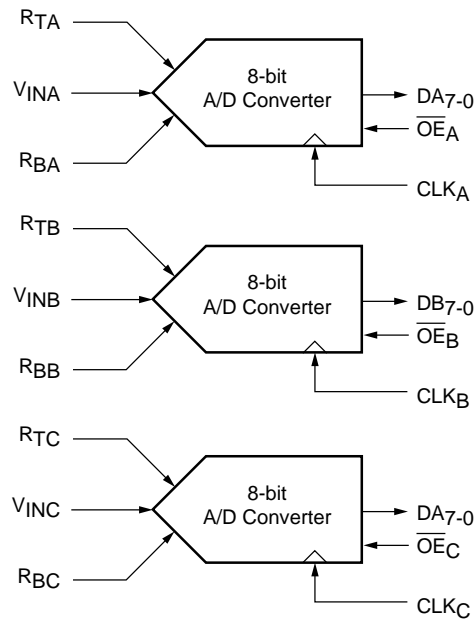
Integral Track/Hold circuits deliver excellent performance on signals with full-scale spectral components up to 12 MHz. Innovative two-step architecture conversion

architecture and submicron CMOS technology reduce typical power dissipation to 100 mW per converter.

Power is derived from a single +5 Volt power supply. Outputs are three-state outputs and TTL/CMOS-compatible.

TMC1203 package is a 80-lead Metric Quad Flat Pack (MQFP). Performance specifications are guaranteed from 0°C to 70°C.

#### Block Diagram



65-3720-01

## Circuit Function

Within the TMC1203 are three 8-bit A/D converters, each employing two-step architecture to convert an analog input to a digital output at rates up to 50 Msps. Input signals are held in integral track/hold stages during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CLKX cycle.

Each of the three converters function identically. In the following descriptions 'X' refers to a generic input/output or clock where 'X' is equivalent to A, B or C.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

### Analog Input and Voltage References

Each A/D accepts analog signals in the range  $R_{BX}$  to  $R_{TX}$  into digital data. Input signals outside this range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range AGND to VDDA.

Input range is very flexible and extends from the +5 Volt power supply to ground. Nominal input range is 2 Volts, extending from 0.6V to 2.6V. Characterization and performance is specified over this range. However, the part will function with a full-scale range from 1.0V to 5.0V. A smaller input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance.

External voltage reference sources are connected to the RTX and RBX pins. RBX can be grounded. Within each A/D converter is a reference resistor ladder comprising 255 resistors that are accessed by the TMC1203 comparators. RTX is connected to the top of the ladder, RBX to the bottom. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

## Digital Inputs and Outputs

Sampling of the applied input signal occurs on the "falling" edge of the CLKX signal (Figure 1). Output data is delayed by  $2\frac{1}{2}$  CLKX cycles and is valid following the "rising" edge of CLKX. Previous output data remains valid for  $t_{HO}$  (Output Hold Time), satisfying any hold time requirement of the receiving circuit. New data becomes valid  $t_D$  (Output Delay Time) after this rising edge of CLKX.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, the output limits at 00h or FFh, as appropriate.

**Table 1. A/D Output Coding**

Input Voltage	Output
RTX + 1 LSB	FF
RTX	FF
RTX - 1 LSB	FE
...	...
RBX + 128 LSB	80
RBX + 127 LSB	7F
...	...
RBX + 1 LSB	01
RBX	00
RBX - 1 LSB	00

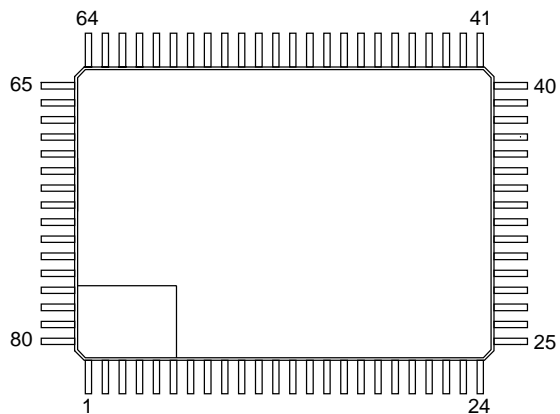
**Note:**  $1 \text{ LSB} = (R_{TX} - R_{BX}) / 255$

The outputs of the TMC1203 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL loads. An Output Enable control,  $\overline{OEX}$ , places the A/D outputs in a high-impedance state when HIGH. The outputs are enabled when  $\overline{OEX}$  is LOW.

### Power and Ground

The TMC1203 operates from a single +5 Volt power supply. For optimum performance, it is recommended that AGND and DGND pins of the TMC1203 be connected to the system analog ground plane.

# Pin Assignments



65-3720-08

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	21	DGND	41	DC7	61	VDD
2	DA5	22	DGND	42	OE $\bar{C}$	62	OE $\bar{B}$
3	DA6	23	NC	43	VDD	63	DB7
4	DA7	24	NC	44	VDD	64	DB6
5	OE $\bar{A}$	25	DGND	45	CLK $\bar{C}$	65	DB5
6	VDD	26	DGND	46	NC	66	DB4
7	VDD	27	VDD	47	VDDA	67	DB3
8	NC	28	VDD	48	VINC	68	DB2
9	CLK $\bar{A}$	29	VDD	49	AGND	69	DB1
10	NC	30	VDD	50	RTC	70	DB0
11	VDDA	31	NC	51	RBC	71	DGND
12	VINA	32	DGND	52	RBB	72	DGND
13	AGND	33	DGND	53	RTB	73	NC
14	RTA	34	DC0	54	AGND	74	DGND
15	RBA	35	DC1	55	VINB	75	DGND
16	DGND	36	DC2	56	VDDA	76	DA0
17	DGND	37	DC3	57	NC	77	DA1
18	DGND	38	DC4	58	CLK $\bar{B}$	78	DA2
19	DGND	39	DC5	59	NC	79	DA3
20	DGND	40	DC6	60	VDD	80	DA4

## Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
<b>A/D Converters</b>			
VINA, VINB, VINC	12, 55, 48	RTX to RBX	<b>Analog Inputs.</b> The input voltage conversion range lies between the voltage applied to the RTX and RBX pins. RTX, RBX.
RTA, RTB, RTC	14, 53, 50	2.6V	<b>Reference Voltage, Top Inputs.</b> DC voltages applied to RTA, RTB and RTC define highest value of VINX.
RBA, RBB, RBC	15, 52, 51	0.6V	<b>Reference Voltage, Bottom Inputs.</b> DC voltages applied to RBA, RBB and RBC define highest value of VINX.
CLKA, CLKB, CLKC	9, 58, 45	CMOS	<b>Convert (Clock) Inputs.</b> A/D converter clock inputs. CMOS-compatible. VINX is sampled on the falling edge of CLKX. Clock inputs are separate for the three converters.
DA7-0	4, 3, 2, 80, 79, 78, 77, 76	CMOS/TTL	<b>Data outputs, Converter A (D7 = MSB).</b> Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
DB7-0	63, 64, 65, 66, 67, 68, 69, 70	CMOS/TTL	<b>Data outputs, Converter B (D7 = MSB).</b> Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
DC7-0	41, 40, 39, 38, 37, 36, 35, 34	CMOS/TTL	<b>Data outputs, Converter C (D7 = MSB).</b> Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLKX.
$\overline{OE}A, \overline{OE}B, \overline{OE}C$	5, 62, 42	CMOS	<b>Output Enable Inputs.</b> CMOS-compatible. When LOW, the A/D output is enabled. When HIGH, the output is in a high-impedance state. Output Enables are separate for the three converters.
<b>Power</b>			
VDDA	11, 47, 56	+5V	<b>Analog Supply Voltage.</b> +5 Volt power inputs. These should come from the same power source and be decoupled to AGND.
VDD	6, 7, 27, 28, 29, 30, 43, 44, 60, 61	+5V	<b>Digital Supply Voltage.</b> +5 Volt power inputs. These should come from the same power source and be decoupled to AGND.
AGND	13, 49, 54	0.0V	<b>Analog Ground.</b> Ground connections. These pins should be connected to the system analog ground plane.
DGND	16, 17, 18, 19, 20, 21, 22, 25, 26, 32, 33, 71, 72, 74, 75	0.0V	<b>Digital Ground.</b> Ground connections. These pins should be connected to the system analog ground plane.
<b>No Connect</b>			
N/C	1, 8, 10, 23, 24, 31, 46, 57, 59, 73	open	<b>Not Connected.</b>

# Specification Notes

## Bandwidth

Bandwidth specification of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: sampling and quantizing. Sampling is *grabbing* a snapshot of the input signal and holding it steady for quantizing. The quantizing process is approximating the analog input to its nearest numerical value within the conversion range. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process relates to the dynamic characteristics of an A/D converter.

Sampling involves an aperture time, the time needed for the track/hold circuit to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the A/D aperture (or faster the shutter) the less the signal (or picture) will be blurred, and the less uncertainty there will be in the quantized value. This is not to be confused with the camera lens opening (aperture), which is entirely different.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of  $2\pi fA$  at zero crossing, or 62.8V/ms. With an 8-bit A/D converter,  $q$  (the quantiza-

tion step size) =  $2V/255 = 7.8mV$ . The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to aperture effects to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Notice that the slew rate is directly proportional to signal amplitude, A. A/Ds will handle lower-amplitude signals of higher bandwidth, but other distortion effects will be worsened.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to sample on these stable pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and bandwidth considerations are less important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1203 is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

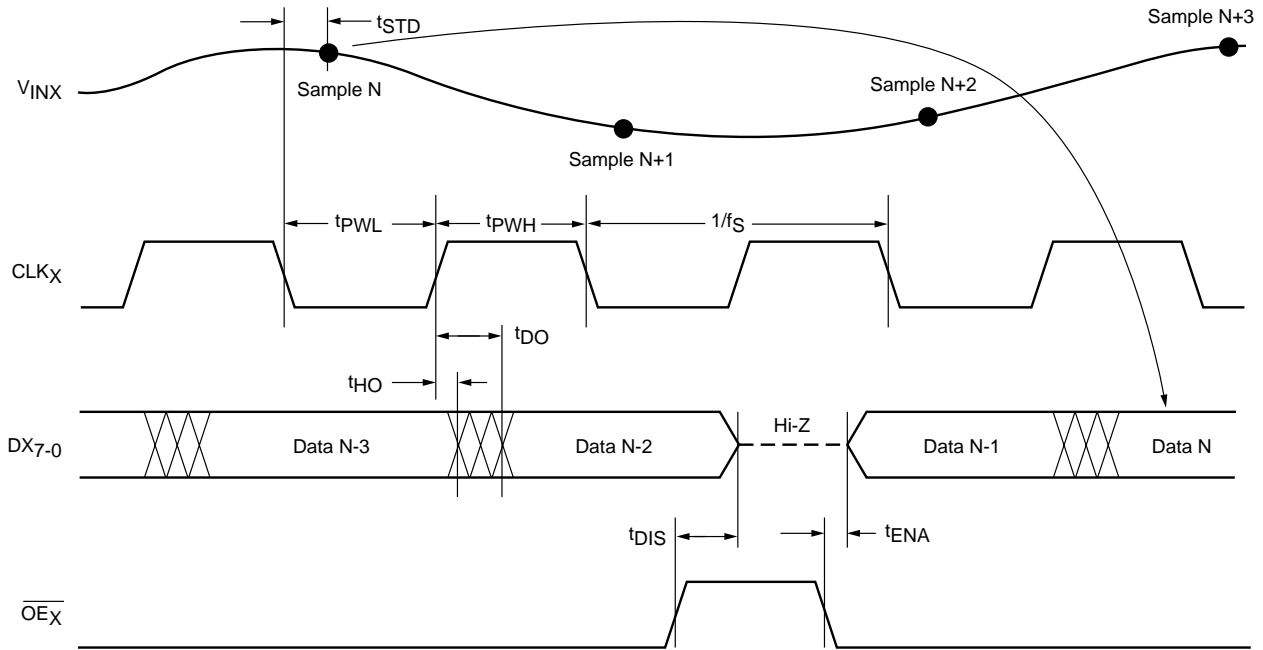


Figure 1. Timing

65-3720-02

## Equivalent Circuits

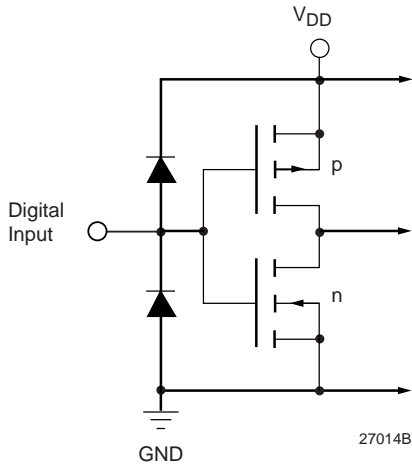


Figure 2. Equivalent Digital Input Circuit

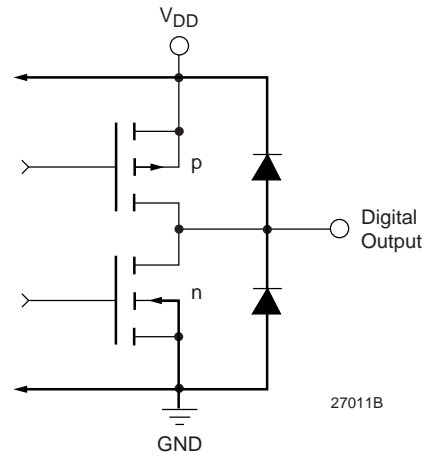


Figure 3. Equivalent Digital Output Circuit

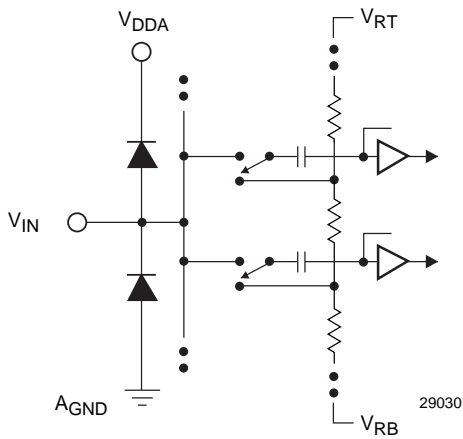


Figure 4. Equivalent Analog Input Circuit

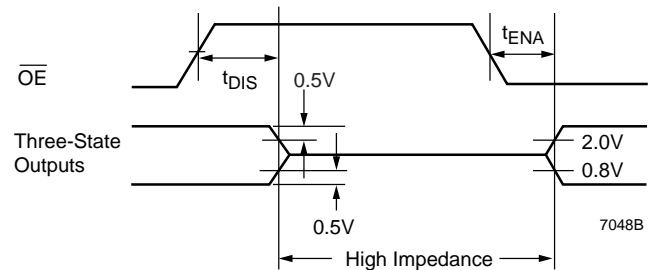


Figure 5. Threshold Levels for Three-State Measurements

## Absolute Maximum Ratings

(beyond which the device may be damaged)<sup>1</sup>

Parameter	Condition	Min	Typ	Max	Unit
<b>Power Supply Voltages</b>					
VDDA	Measured to AGND	-0.5		+7.0	V
VDDP	Measured to DGND	-0.5		+7.0	V
VDD	Measured to DGND	-0.5		+7.0	V
VDDA	Measured to VDD	-0.5		+0.5	V
VDDP	Measured to VDD	-0.5		+0.5	V
AGND	Measured to DGND	-0.5		+0.5	V
<b>Digital Inputs</b>					
Applied Voltage	Measured to DGND <sup>2</sup>	-0.5		VDD + 0.5	V
Forced current <sup>3, 4</sup>		-10.0		+10.0	mA

## Absolute Maximum Ratings (continued)

(beyond which the device may be damaged)<sup>1</sup>

Parameter	Condition	Min	Typ	Max	Unit
<b>Analog Inputs</b>					
Applied Voltage	Measured to AGND <sup>2</sup>	-0.5		V <sub>DDA</sub> +0.5	V
Forced current <sup>3, 4</sup>		-10.0		+10.0	mA
<b>Digital Outputs</b>					
Applied voltage	Measured to DGND2	-0.5		V <sub>DD</sub> + 0.5	V
Forced current <sup>3, 4</sup>		-6.0		+6.0	mA
Short circuit duration	Single output in HIGH state to ground)			1 second	
<b>Temperature</b>					
Operating, ambient		-20		110	°C
Junction				+150	°C
Lead, soldering	10 seconds			+300	°C
Vapor Phase soldering	1 minute			+220	°C
Storage		-65		+150	°C
<b>Electrostatic Discharge<sup>5</sup></b>				±150	V

### Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

## Operating Conditions

Parameter		Min.	Nom	Max.	Units
V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDP</sub>	Power Supply Voltage	4.75	5.0	5.25	V
AGND	Analog Ground (Measured to DGND)	-0.1	0	0.1	V
V <sub>RTX</sub>	Reference Voltage, Top		2.6	V <sub>DDA</sub>	V
V <sub>RBX</sub>	Reference Voltage, Bottom	0	0.6		V
V <sub>RTX</sub> -V <sub>RBX</sub>	Reference Voltage Differential	1.0	2.0	5.0	V
V <sub>INX</sub>	Analog Input Range	V <sub>RB</sub>		V <sub>RT</sub>	V
V <sub>IH</sub>	Input Voltage, Logic HIGH	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub>	Input Voltage, Logic LOW	GND		0.3 V <sub>DD</sub>	V
I <sub>OH</sub>	Output Current, Logic HIGH			-4.0	mA
I <sub>OL</sub>	Output Current, Logic LOW			4.0	mA
T <sub>A</sub>	Ambient Temperature, Still Air	0		70	°C

## Electrical Characteristics

Parameter		Conditions	Min.	Typ <sup>1</sup>	Max.	Units
IDD	Power Supply Current <sup>1</sup>	VDD = VDDA = VDDP = Max., CLOAD = 35pF, fCK = fS (3 A/Ds)				
		fS = 20 Msps		70	90	mA
		fS = 40 Msps		94	120	mA
		fS = 50 Msps		105	135	mA
IDDQ	Power Supply Current, Quiescent	VDD = VDDA = Max.				
		CLKX = LOW		29	55	mA
		CLKX = HIGH		45	65	mA
PD	Total Power Dissipation	VDD = VDDA = VDDP = Max., CLOAD = 35pF, fCK = fS (3 A/Ds)				
		fS = 20 Msps		300	470	mW
		fS = 40 Msps		425	630	mW
		fS = 50 Msps		490	710	mW
CAI	Input Capacitance, Analog	CLKX = LOW		4		pF
		CLKX = HIGH		12		pF
RIN	Input Resistance		500			kΩ
RREF	Reference Resistance		200	270	340	Ω
ICB	Input Current, Analog				±1	μA
I <sub>IH</sub>	Input Current, HIGH	VDD = Max., VIN = VDD			±5	μA
I <sub>IL</sub>	Input Current, LOW	VDD = Max., VIN = 0V			±5	μA
IOZH	Hi-Z Output Leakage Current, Output HIGH	VDD = Max., VIN = VDD			±5	μA
IOZL	Hi-Z Output Leakage Current, Output LOW	VDD = Max., VIN = VDD			±5	μA
I <sub>OS</sub>	Short-Circuit Current				-35	mA
VOH	Output Voltage, HIGH	I <sub>OH</sub> = -100mA	VDD-0.3			V
		I <sub>OH</sub> = -2.5mA	3.5			V
		I <sub>OH</sub> = Max.	2.4			V
VOL	Output Voltage, LOW	I <sub>OL</sub> = Max.			0.4	V
CDI	Digital Input Capacitance			4	10	pF
CDO	Digital Output Capacitance			10		pF

### Note:

1. Typical values with VDD = VDDA = Nom and TA = Nom, Minimum/Maximum values with VDD = VDDA = Max. and TA = Min..

## Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
fs	Conversion Rate	TMC1203-20			20	Msps
		TMC1203-40			40	Msps
		TMC1203-50			50	Msps
tPWH	CLKX Pulsewidth, HIGH	TMC1203-20	14			ns
		TMC1203-40	14			ns
		TMC1203-50	12			ns
tPWL	CLKX Pulsewidth, LOW	TMC1203-20	8			ns
		TMC1203-40	8			ns
		TMC1203-50	7			ns
EAP	Aperture Error		30		ps	
tSTO	Sampling Time Offset		1	2	5	ns
tSTS	Sampling Time Skew			150	400	ps
tHO	Output Hold Time	CLOAD = 15pF	9			ns
tDO	Output Delay Time				14	ns
tENA	Output Enable Time				27	ns
tDIS	Output Disable Time				42	ns

## System Performance Characteristics

Parameter		Conditions	Min. <sup>2</sup>	Typ <sup>1</sup>	Max. <sup>2</sup>	Units
ELI	Integral Linearity Error, Independent	V <sub>RT</sub> = 2.6V		±0.5		LSB
ELD	Differential Linearity Error	V <sub>RB</sub> = 0.6V		±0.5		LSB
BW	Bandwidth <sup>1</sup>	TMC1203-20			10	MHz
		TMC1203-40			12	MHz
		TMC1203-50			12	MHz
EOT	Offset Voltage, Top (R <sub>T</sub> - V <sub>IN</sub> for most positive code transition)	V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V	-40		80	mV
EOB	Offset Voltage, Bottom (R <sub>B</sub> - V <sub>IN</sub> for most negative code transition)	V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V	-95		-30	mV
dg	Differential Gain	f <sub>S</sub> = 14.3Msps NTSC 40 IRE Mod Ramp V <sub>DDA</sub> = +5.0V, T <sub>A</sub> = 25°C V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V		1.8		%
dp	Differential Phase	f <sub>S</sub> = 14.3Msps NTSC 40 IRE Mod Ramp V <sub>DDA</sub> = +5.0V, T <sub>A</sub> = 25°C V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V		0.7		deg
XTALK	Channel Crosstalk	f <sub>N</sub> = 5.0 MHz		45		dB

## System Performance Characteristics (continued)

Parameter	Conditions	Min. <sup>2</sup>	Typ <sup>1</sup>	Max. <sup>2</sup>	Units	
SNR <sup>3</sup>	Signal-to-Noise Ratio	f <sub>S</sub> = 20Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		46		dB
		f <sub>N</sub> = 2.48MHz		46		dB
		f <sub>N</sub> = 6.98MHz		45		dB
		f <sub>N</sub> = 10.0MHz		45		dB
		f <sub>S</sub> = 40Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		42		dB
		f <sub>N</sub> = 6.98MHz		41		dB
		f <sub>N</sub> = 12.0MHz		40		dB
		f <sub>N</sub> = 20.0MHz		38		dB
		f <sub>S</sub> = 50Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		40		dB
		f <sub>N</sub> = 6.98MHz		40		dB
		f <sub>N</sub> = 12.0MHz		40		dB
SFDR <sup>4</sup>	Spurious-Free Dynamic Range	f <sub>S</sub> = 20Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		53		dB
		f <sub>N</sub> = 2.48MHz		48		dB
		f <sub>N</sub> = 6.98MHz		44		dB
		f <sub>N</sub> = 10.0MHz		40		dB
		f <sub>S</sub> = 40Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		49		dB
		f <sub>N</sub> = 6.98MHz		44		dB
		f <sub>N</sub> = 12.0MHz		38		dB
		f <sub>S</sub> = 50Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V				
		f <sub>N</sub> = 1.24MHz		46		dB
		f <sub>N</sub> = 6.98MHz		40		dB
		f <sub>N</sub> = 12.0MHz		37		dB

### Notes:

1. Values shown in Typ. column are typical for V<sub>DD</sub> = V<sub>DDA</sub> = +5V and T<sub>A</sub> = 25°C.
2. Values shown in Min. and Max. columns are for V<sub>DD</sub> = V<sub>DDA</sub> and T<sub>A</sub> over entire range specified under Operating Conditions.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
5. Characteristics specified for V<sub>RT</sub> = 2.6V, V<sub>RB</sub> = 0.6V.
6. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.

### Typical Performance Characteristics

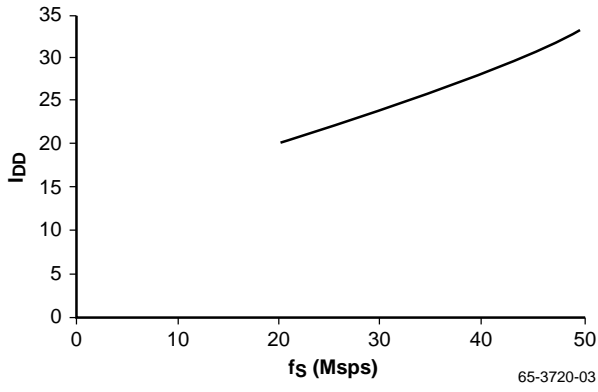


Figure 6. Typical  $I_{DD}$  vs  $f_S$  (Single A/D)

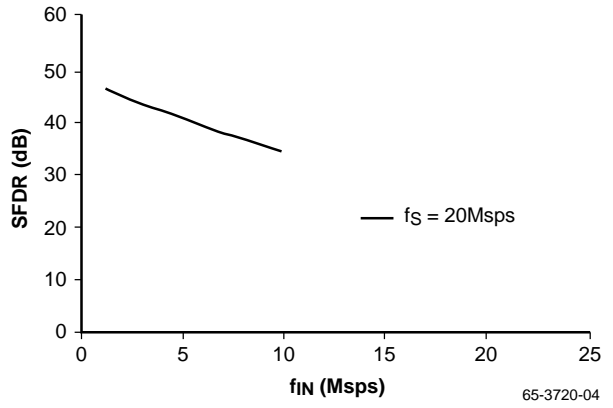


Figure 7. Typical SFDR vs  $f_{IN}$

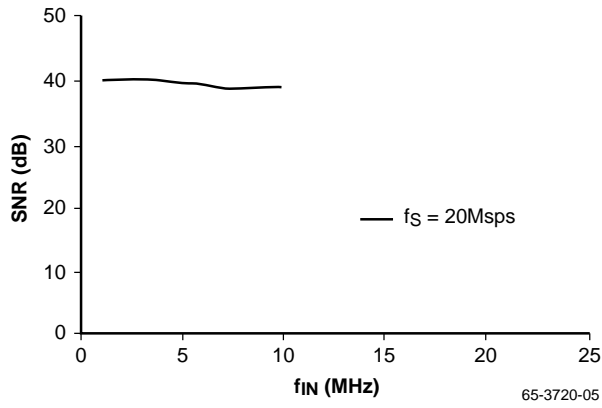


Figure 8. Typical SNR vs  $f_{IN}$

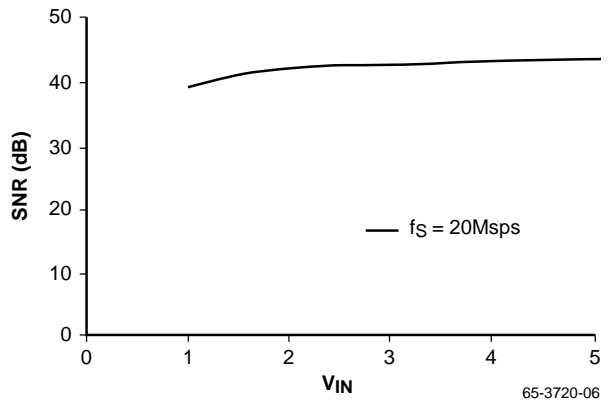


Figure 9. Typical SNR vs Full Scale Input Range

## Application Notes

The circuit in Figure 10 employs a band-gap reference to generate a variable  $R_{TX}$  reference voltages for the TMC1203 as well as a bias voltage to offset the wideband input amplifiers to mid-range. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at  $R_{TX}$  can be adjusted from 0.0 to 2.4 volts while  $R_{BX}$  is grounded. Schottky diodes are used to restrict the wideband amplifier output to between  $-0.3V$  and  $V_{DD} + 0.3V$ . Diode protection is good practice to limit the analog input voltage at  $V_{INX}$  to the safe operating range.

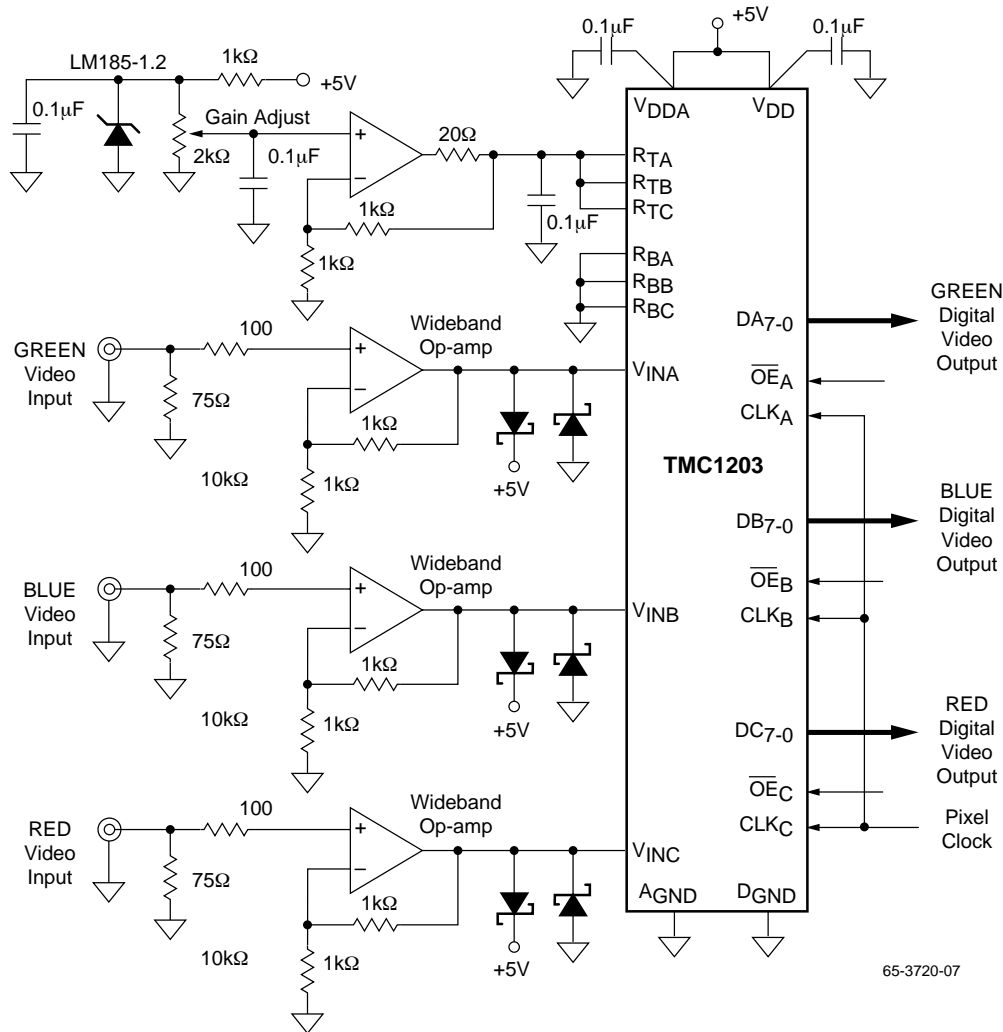


Figure 10. Typical Interface Circuit - High Performance

### Grounding

The TMC1203 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages ( $V_{DD}$  and  $V_{DDA}$ ) come from the same source, and that ground connections ( $DGND$  and  $AGND$ ) be made to the analog ground plane, and as close as possible to the device pins. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1203 should be referred to the system digital ground plane.

### Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces ( $V_N$ ,  $R_{TX}$ ,  $R_{BX}$ ) as short as possible and as far as possible from all digital signals. The TMC1203 should be located close to the analog input connectors.

## 2. Segregate traces:

- A/D analog
- D/A analog
- Clocks
- Digital

Treat analog inputs as transmission lines. Cleanly route traces over the ground plane bearing in mind that the return currents will flow through the ground plane beneath the traces. Do not route digital traces nearby. A few inches of digital trace less than a few line widths from an analog trace will cross-couple noise into adjacent analog circuits.

3. The power plane for the TMC1203 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the VDD pins. If the power supply for the TMC1203 is the same as that of the system's digital circuitry, power to the TMC1203 should be decoupled with ferrite beads and 0.1 $\mu$ F capacitors to reduce noise.
4. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

5. Decoupling capacitors should be applied liberally to VDD pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1 $\mu$ F ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.
6. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1203, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1203 and its related analog circuitry can have an adverse effect on performance.
7. CLK<sub>X</sub> should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line, if needed, to eliminate overshoot and ringing.

## Related Products

- TMC1175A, TMC1275 8-Bit Video A/D Converters
- TMC1173A, TMC1273 3V, Low-Power 8-Bit Video A/D Converters
- TMC1103 Triple 8-bit A/D with Clamps and PLL
- TMC3003/TMC3503 Triple Video D/A Converters
- TMC2242B/TMC2243/TMC2246A Digital Filters

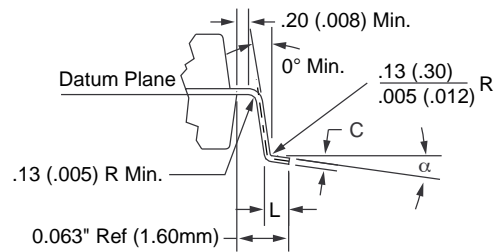
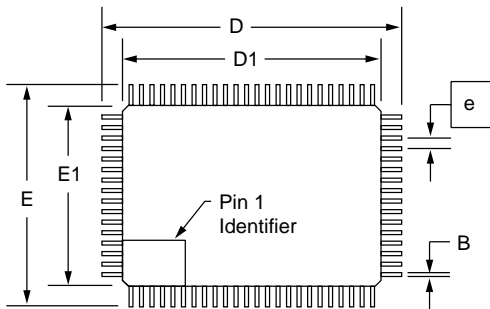
**Notes:**

# Mechanical Dimensions – 80-Lead MQFP Package

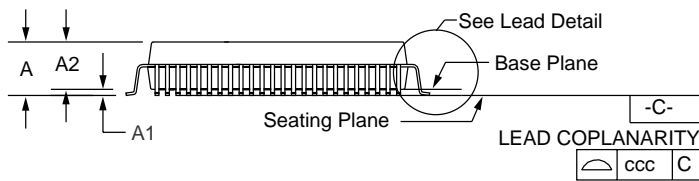
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0315 BSC		.80 BSC		
L	.025	.041	.65	1.03	4
N	80		80		
ND	24		24		
NE	16		16		
$\alpha$	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

**Notes:**

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Lead Detail



## Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1203KLC20	20 Msps	T <sub>A</sub> = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC20
TMC1203KLC40	40 Msps	T <sub>A</sub> = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC40
TMC1203KLC50	50 Msps	T <sub>A</sub> = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC50

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.