TMC2074P7C

Demonstration Board for the TMC2490(1)A

Features

- 8-bit Parallel YCbCr input
- Composite and S-video outputs
- D1 and Master mode operation
- Complete MPEG interface
- Fairchild demo board compatibility

Applications

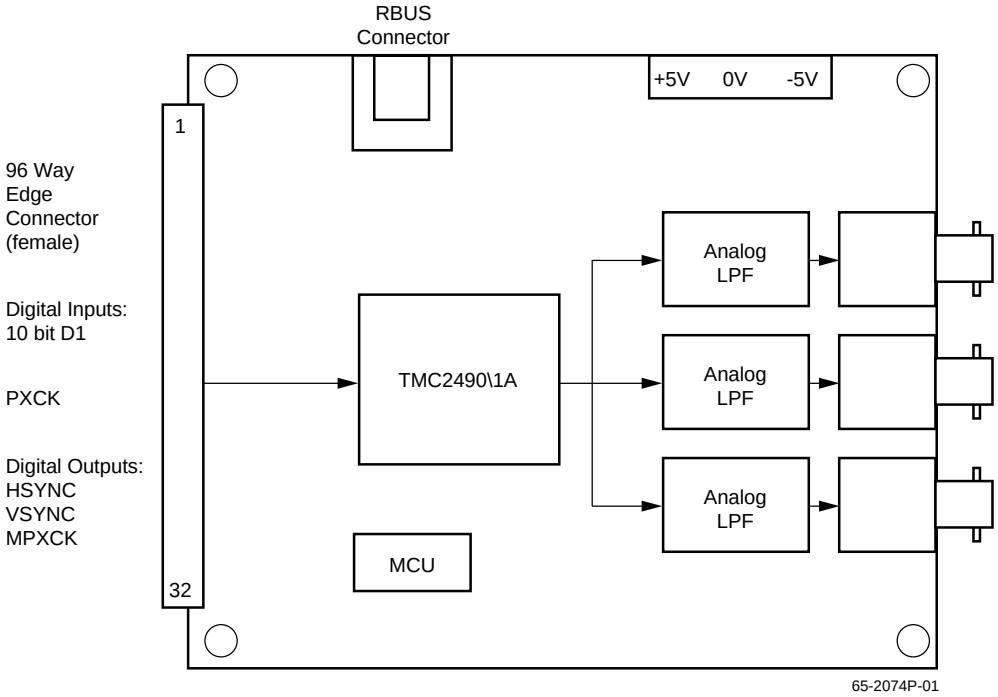
- Evaluation of TMC2490(1)A DENC
- Output for TMC2068P7C Decoder demo board
- System Breadboarding

Description

The TMC2074P7C demonstration board provides a flexible base for evaluating the performance of the TMC2490(1)A Digital Video Encoder (DENC). The board can be driven by D1 source, or it can supply the synchronization signals needed to drive a framestore or any MPEG Decoder.
The board provides high quality analog composite video and analog S-video outputs.

Preliminary Information

Block Diagram



65-2074P-01

Functional Description

The TMC2074P7C is designed to demonstrate the performance of the TMC2490(1)A Digital Video Encoder (DENC). For a complete description of the TMC2490(1)A, please refer to TMC2490(1)A data sheet. The TMC2074P7C is compatible with other Fairchild Demo boards. Typical configurations are the TMC2067P7C, the TMC2068P7C, and the TMC2074P7C or the TMC2071P7C and the TMC2074P7C. The first configuration requires a analog composite or S-video input and supplies a re-encoded analog composite or S-video output. The later requires a parallel D1 input and supplies a encoded analog composite or S-video output.

The TMC2490(1)A can be operated in both D1 and Master mode operation. In the D1 mode the synchronization is derived from the TRS codes embedded in the D1 data stream. In Master mode the synchronization is driven by the TMC2490(1)A, supplying the line ($\overline{\text{HSYNC}}$) and field ($\overline{\text{VSYNC}}$ or BnT) synchronization signals. With the TMC2490(1)A running in Master mode the TMC2074P7C demo board interfaces directly to either a MPEG decoder or a video framestore with no additional glue logic.

The TMC2074P7C has an onboard microcontroller (MCU) to program the TMC2490(1)A. The default register maps are held within the MCU, Table 1, provides a description of each of the default register maps. The control register map is written to the TMC2490(1)A each time the $\overline{\text{MRST}}$ button is pressed. The MCU determines which map to load by the PROG[3-0] (Px) dip switches. The TMC2490(1)A can also be driven by the Raydemo software. The interface is provided by the RBUS connector on the TMC2074P7C and the TMC2070P7C R-Bus interface board. With this setup the user can configure TMC2490(1)A with any IBM compatible PC.

Table 1. Default Control Register Maps

P3	P2	P1	P0	Mode	Format	Source	Synchronization	Comments
0	0	0	0	MASTER	NTSC	Internal Ramp	B/nT, CBSEL, SELC, Hsync	
0	0	0	1	MASTER	NTSC	PD[7:0]	B/nT, CBSEL, SELC, Hsync	
0	0	1	0	MASTER	NTSC	PD[7:0]	Vsync, CBSEL, SELC, Hsync	Macrovision 7.01 if the TMC2491A is fitted.
0	0	1	1	MASTER	NTSC	PD[7:0]	B/nT, PDC, SELC, Hsync	CC encoding
0	1	0	0	MASTER	PAL	Internal Ramp	B/nT, CBSEL, SELC, Hsync	
0	1	0	1	MASTER	PAL	PD[7:0]	B/nT, CBSEL, SELC, Hsync	
0	1	1	0	MASTER	PAL	PD[7:0]	Vsync, CBSEL, SELC, Hsync	Macrovision 7.01 if the TMC2491A is fitted.
0	1	1	1	MASTER	PAL	PD[7:0]	Vsync, PDC, SELC, Hsync	
1	0	0	0	D1	NTSC	Internal Ramp	B/nT, CBSEL, SELC, Hsync	
1	0	0	1	D1	NTSC	PD[7:0]	B/nT, CBSEL, SELC, Hsync	
1	0	1	0	D1	NTSC	PD[7:0]	Vsync, CBSEL, SELC, Hsync	Macrovision 7.01 if the TMC2491A is fitted.
1	0	1	1	D1	NTSC	PD[7:0]	B/nT, PDC, SELC, Hsync	CC encoding
1	1	0	0	D1	PAL	Internal Ramp	B/nT, CBSEL, SELC, Hsync	
1	1	0	1	D1	PAL	PD[7:0]	B/nT, CBSEL, SELC, Hsync	
1	1	1	0	D1	PAL	PD[7:0]	Vsync, CBSEL, SELC, Hsync	Macrovision 7.01 if the TMC2491A is fitted.
1	1	1	1	D1	PAL	PD[7:0]	Vsync, PDC, SELC, Hsync	

Switch, Button, and Jumper Description

Button	Description
$\overline{\text{MRST}}$	Resets the AT89C2051. When the GLOBAL RESET jumper is in place, the reset line on all boards connected to the TMC2074P7C are driven by $\overline{\text{MRST}}$.
Jumpers	**Description**
GLOBAL RESET	When GLOBAL RESET is open, only the TMC2490(1)A and the AT89C2051 receive the reset pluse from $\overline{\text{MRST}}$. When GLOBAL RESET is closed, the reset line on all boards connected to the TMC2074P7C are driven by $\overline{\text{MRST}}$.
RBUSEN	WHEN RBUSEN is open, the RBUS port is disabled. WHEN RBUSEN is closed, the RBUS port is enabled.
JP7, JP8, JP9	When JPx is open, the output video is a single 75 Ohm termination. When JPx is closed, the output video is a double 75 Ohm termination.
Switches	**Description**
SELECT	Clock Selection When EXT. is selected the clock source for the TMC2074P7C is provided from the input edge connector (IXPXCK). When INT. is selected the clock source for the TMC2074P7C is provided by the onboard TTL clock oscillator.
JP1, JP2, JP3	When BUS A is selected the pixel data from the edge connector is supplied to the TM2490(1)A PD port. When DELAYED is selected the pixel data supplied to the PD port of the TMC2490(1)A is supplied by the framestore header.
Dip Switches	**Description**
SA1-0	Configures the bits 2 and 1of the TMC2490(1)A RBUS chip address. When SAx is ON (down), SAx is in a LOW state. When SAx is OFF (up), SAx is in a HIGH state.
CAS	Universal Program Enable When CAS is ON (down), the MCU waits for the PGM_IN to be pulsed low before driving the RBUS. This ensures that no two configuration devices are on the bus at the same time. When CAS is OFF (up), the MCU configures the TMC2490(1)A after reset.
$\overline{\text{ERST}}$	Resets the TMC2490(1)A when LOW.
P3-0	Control Register Programming P3-0 selects which control register map to write to the TMC2490(1)A after reset. Refer to Table 1 Default Control Register Maps for a description.

Setup Procedure

1. Set clock selection to EXT.
2. Provide 100% Color Bar D1 test signal at the input edge connector.
3. Set SA1-0 to ON (down).
4. Set P3-0 to 9h, P3 is OFF (up), P2 is ON (down), P1 is ON (down), and P0 is OFF (up).
5. Plug in power supply connector and apply power. The LED's corresponding to +5 Volts and -5 Volts should be illuminated.
6. Reset board by pressing the MRST button.
7. Adjust R16 until 100% white level is 100 IRE (714mV). Blank is 0 IRE (0mV).

Power Supply Requirements

The TMC2074P7C board requires 1.0 Amp from the +5 Volt power supply. Both the +5 Volt and -5 Volt supplies are connected to the input connector to supply the power requirements of any upstream board. The +5 Volt power supply not only drives TTL logic devices but it also provides the power and voltage references to the D/A's in the TMC2490(1)A. Therefore, it is recommended that a bench power supply be used with the cable lengths kept to a minimum.

Schematics

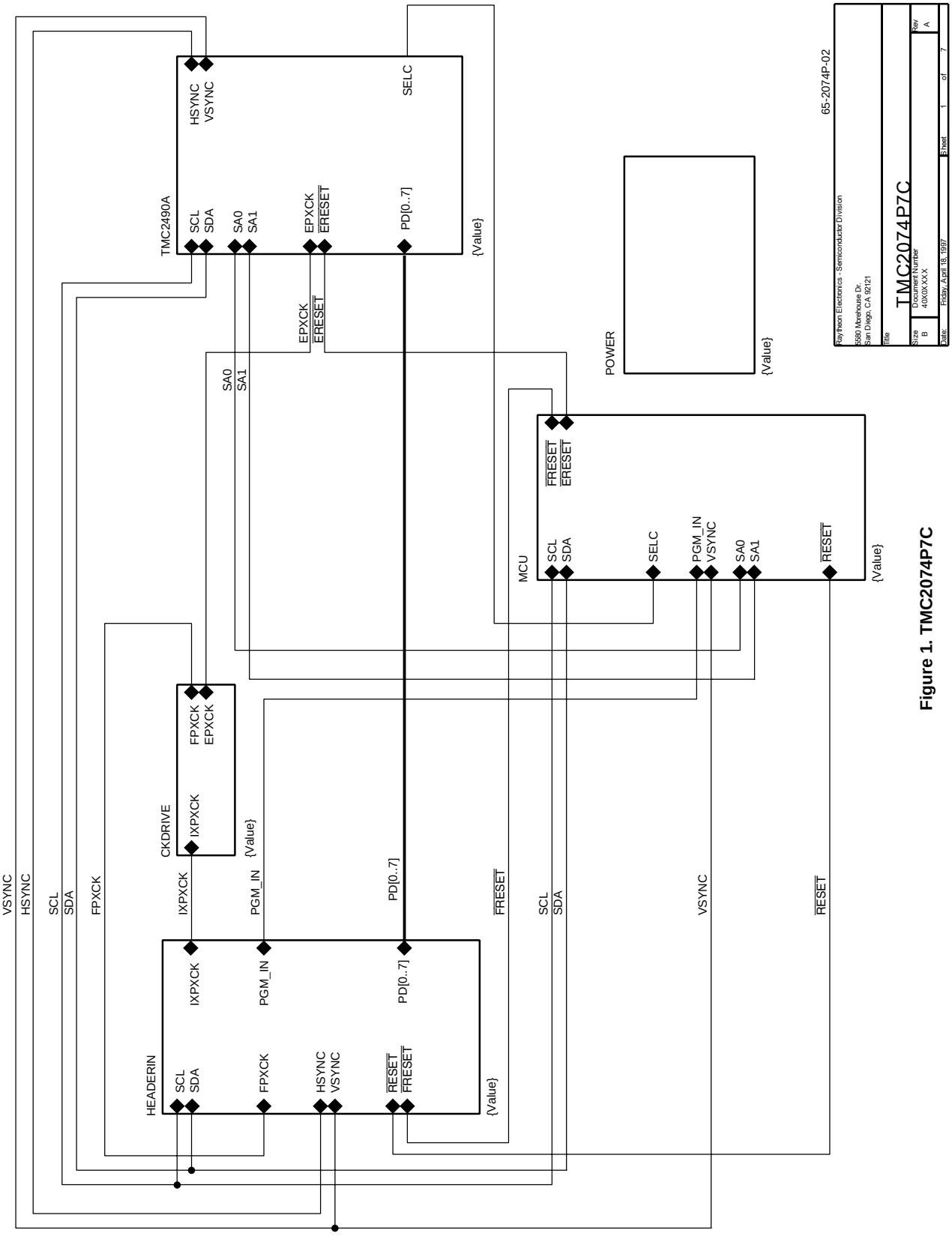


Figure 1. TMC2074P7C

Schematics (continued)

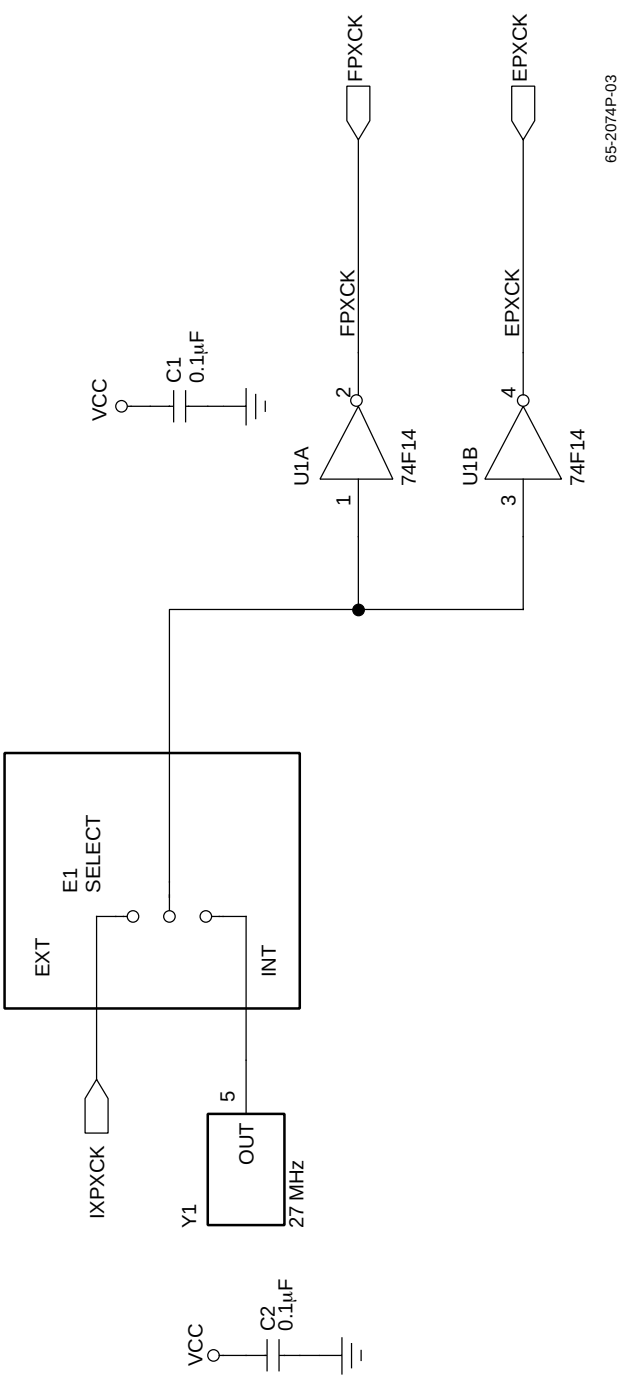


Figure 2. CKDRIVE.SCH

Preliminary Information

Schematics (continued)

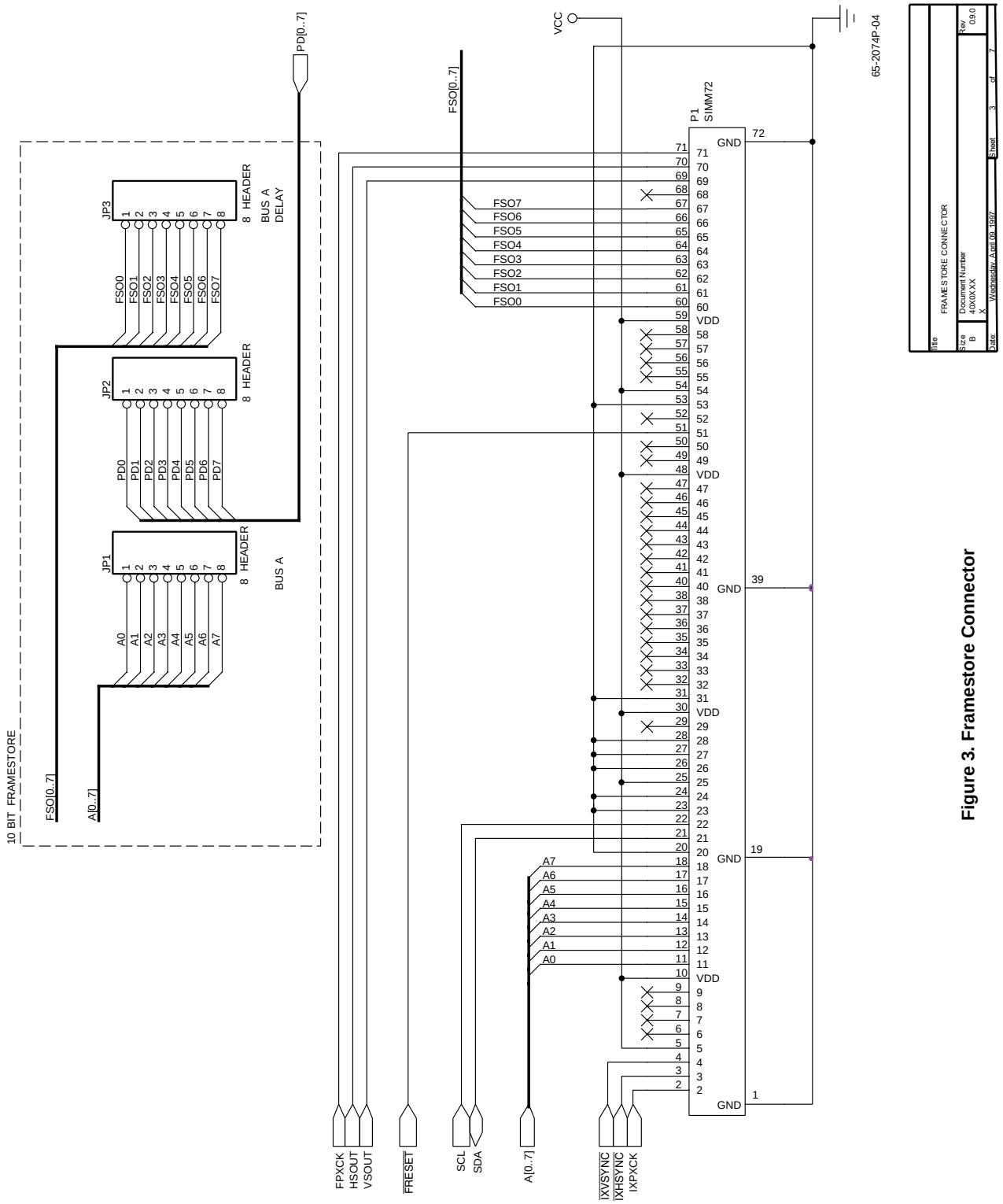


Figure 3. Framestore Connector

Schematics (continued)

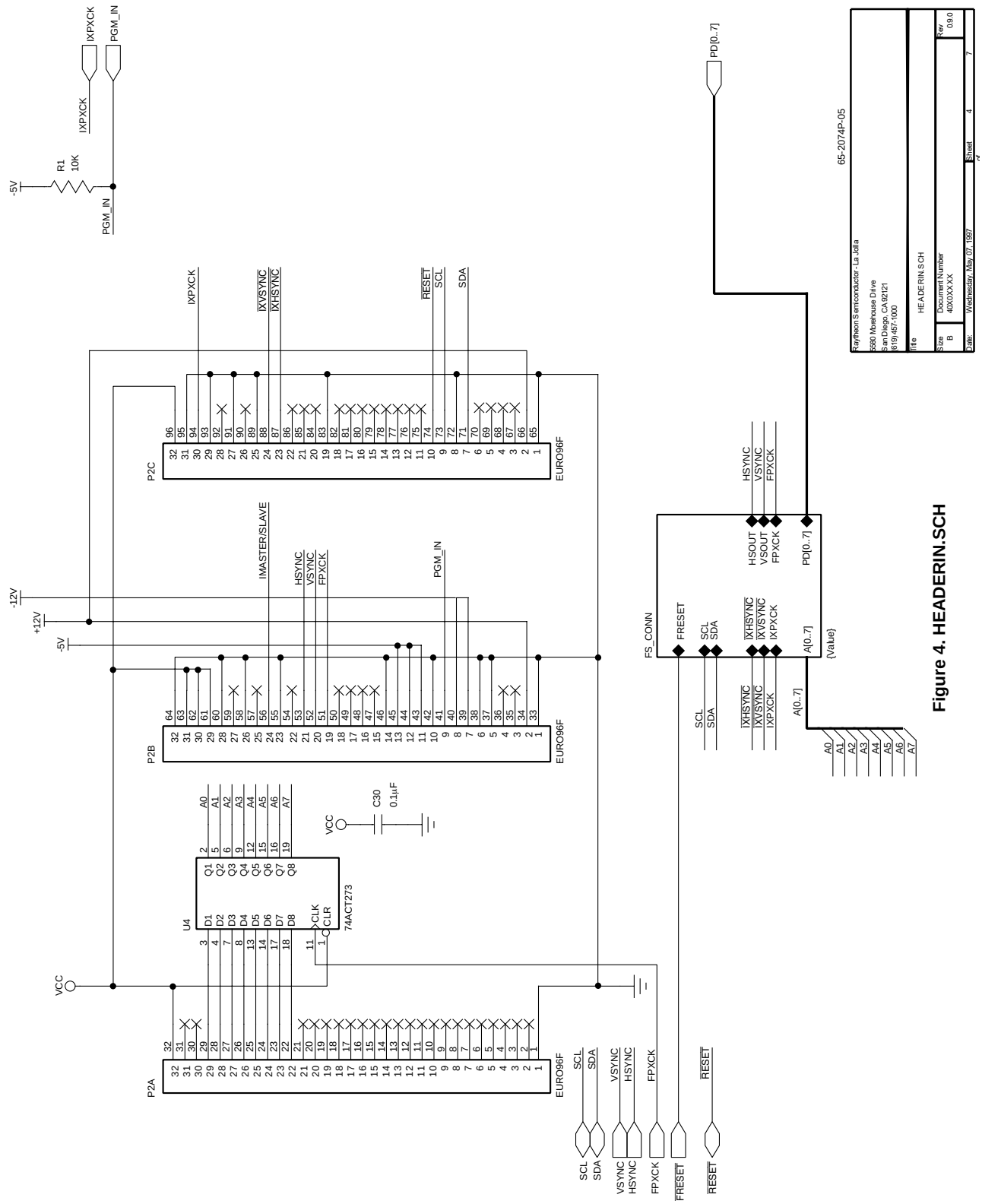


Figure 4. HEADERIN.SCH

Preliminary Information

Schematics (continued)

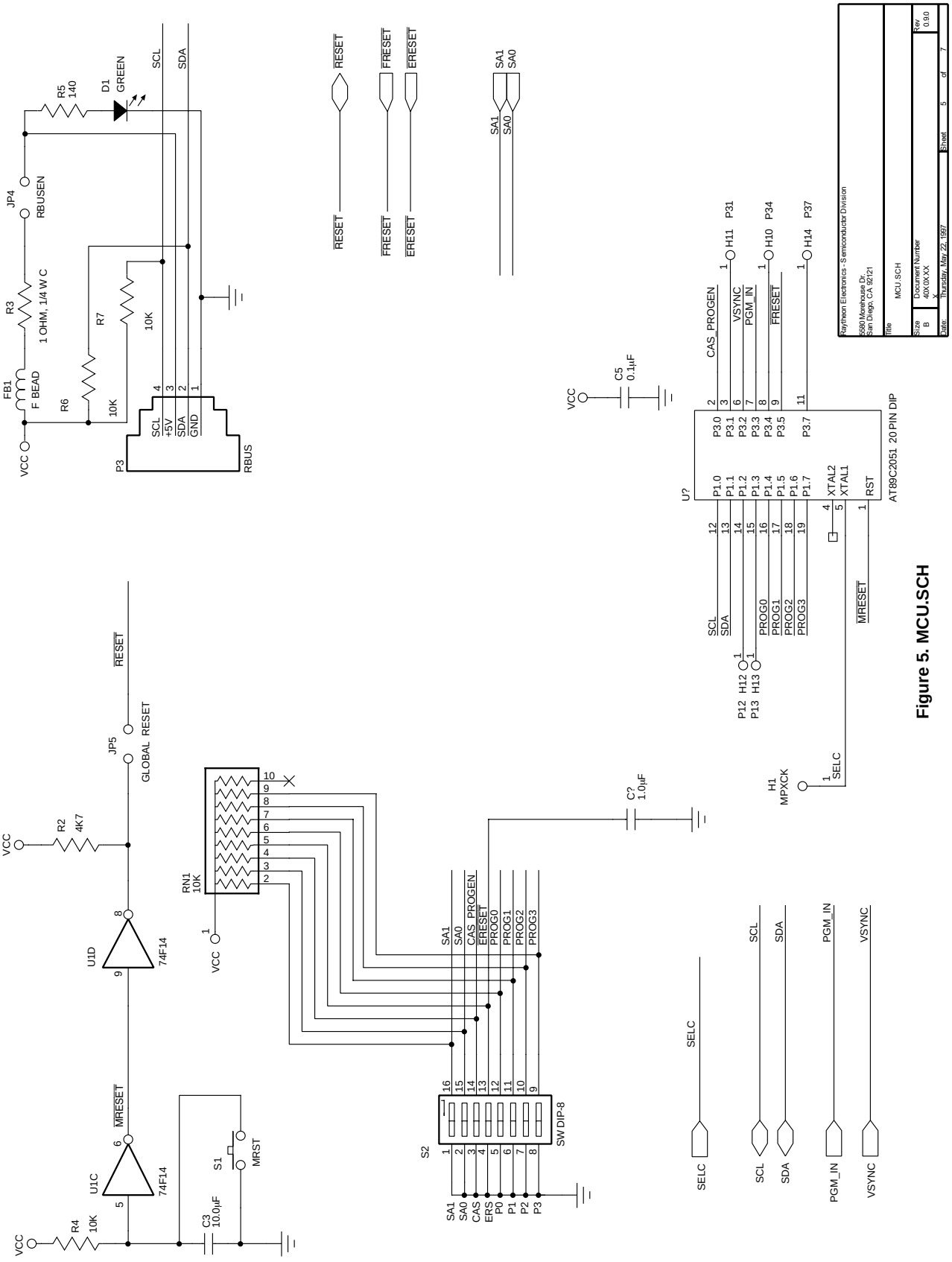


Figure 5. MCU.SCH

Schematics (continued)

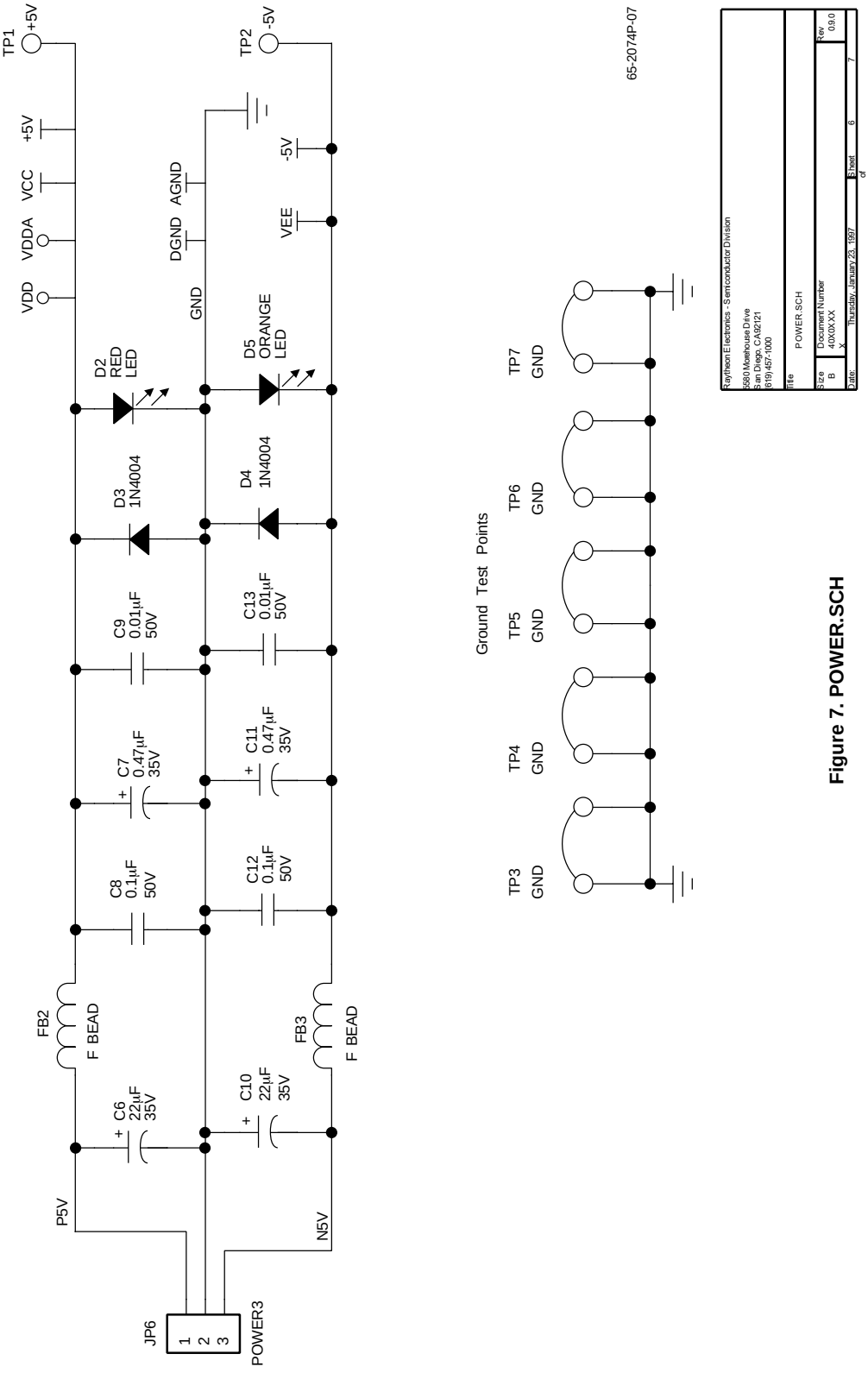


Figure 7. POWER.SCH

Preliminary Information

Schematics (continued)

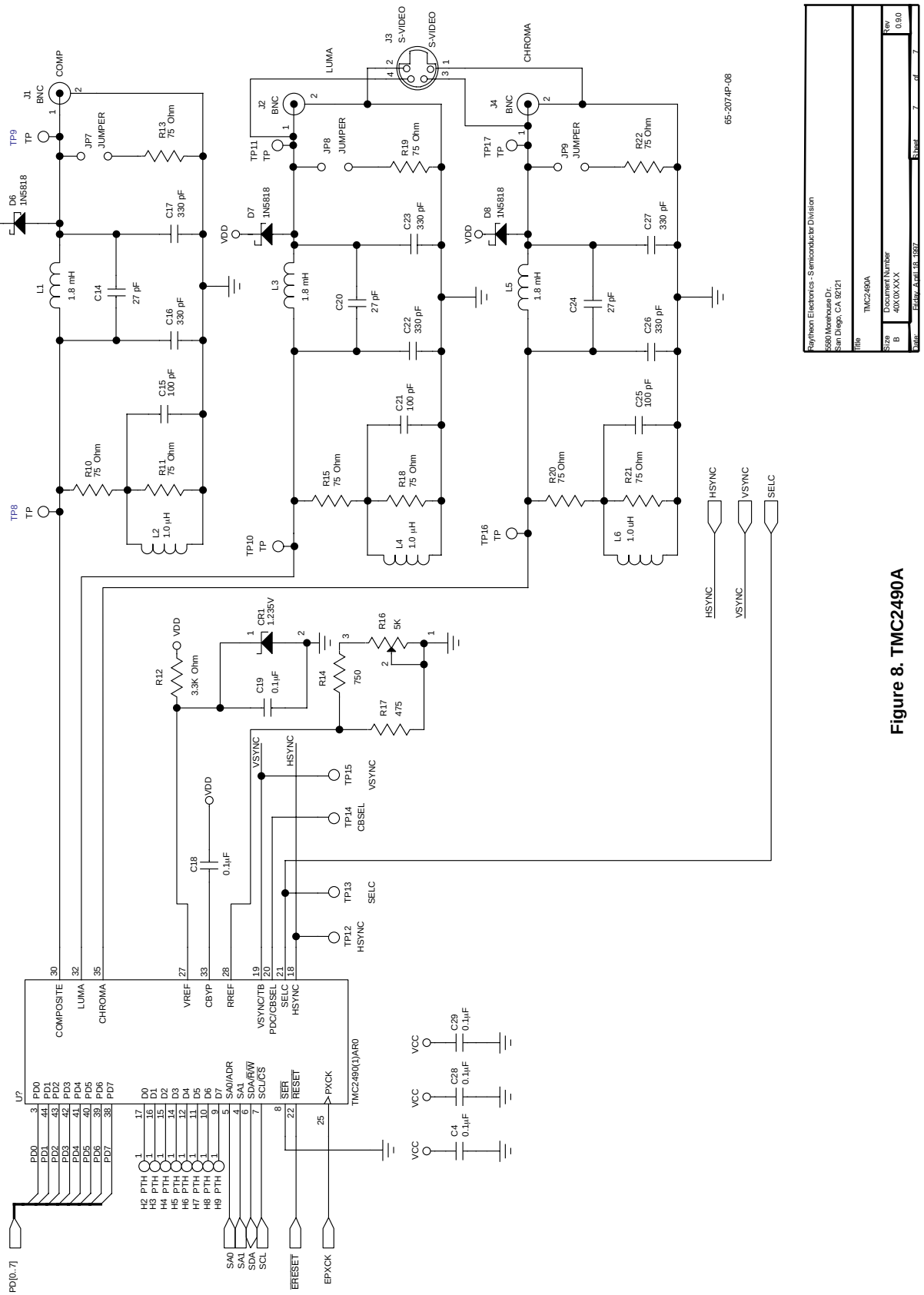


Figure 8. TMC2490A

Table 2. TMC2074P7C Parts List

Item	Qty.	Part Mfr./Number	Reference	Part
1	1	Linear Technology: LT1004CH-1.235	CR1	Diode Zener, 1.2 vref
2	11	MiniReel: 605-611	C1,C2,C4,C5,C8,C12, C18,C19,C28,C29,C30	0.1μF
3	1	MiniReel: 644-810	C3	10.0μF
4	2	MiniReel: 645-823	C6,C10	22μF
5	2	MiniReel: 641-647	C7,C11	0.47μF
6	2	MiniReel: 605-510	C9,C13	0.01μF
7	3	MiniReel: 605-227	C14,C20,C24	27 pF
8	3	MiniReel: 605-310	C15,C21,C25	100 pF
9	6	MiniReel: 605-333	C16,C17,C22,C23, C26,C27	330 pF
10	1	HP: HLMP:DB00 HP: HLMP:DB15	D1	Blue
11	1	Hewlett Pachard: hlmp-1600	D2	Red
12	2	MiniReel: 76-4004	D3,D4	1N4004
13	1	Hewlett Pachard: hlmp-1620	D5	Orange
14	3	MiniReel: 71-5818	D6,D7,D8	1N5818 Schottky
15	1	SECMA: 090320102	E1	Select
16	3	Fair-Rite: 2743019447	FB1,FB2,FB3	F Bead
17	1		H1	MPXCK
18	8		H2,H3,H4,H5,H6,H7, H8,H9	PTH
19	3	AMP: 102972-8 AMP: 103185-8	JP1,JP2,JP3	8 Header
20	1	AMP: 103747-2	JP4	RBUSEN
21	1	AMP: 103747-2	JP5	Global Reset
22	1	AMP: 103747-2	JP6	POWER3
23	3	AMP: 103747-2	JP7,JP8,JP9	Jumper
24	3	Amphenol: 31-5431	J1,J2,J4	BNC
25	1	AMP: 749264-1	J3	S-VIDEO
26	3	MiniReel: 667-118	L1,L3,L5	1.8 mH
27	3	MiniReel: 667-110	L2,L4,L6	1.0 μH
28	1	AMP: 4-103186-0	P1	SIMM72
29	1	AMP: 650461-4	P2	EURO96F
30	1	Molex: 15-83-0064 AMP: 4-943197-1	P3	RBUS
31	1	DALE: CSC10A-01-103	RN1	10K sip
32	4	MiniReel: 615-510	R1,R4,R6,R7	10K
34	1	ROHM: R25XT-68J1R0	R3	1 OHM 1/4W C
35		MiniReel: 615-314	R5	140
36	9	MiniReel: 615-275	R10,R11,R13,R15, R18,R19,R20,R21,R22	75 Ohm
37	1	MiniReel: 615-844	R12	3.3K Ohm

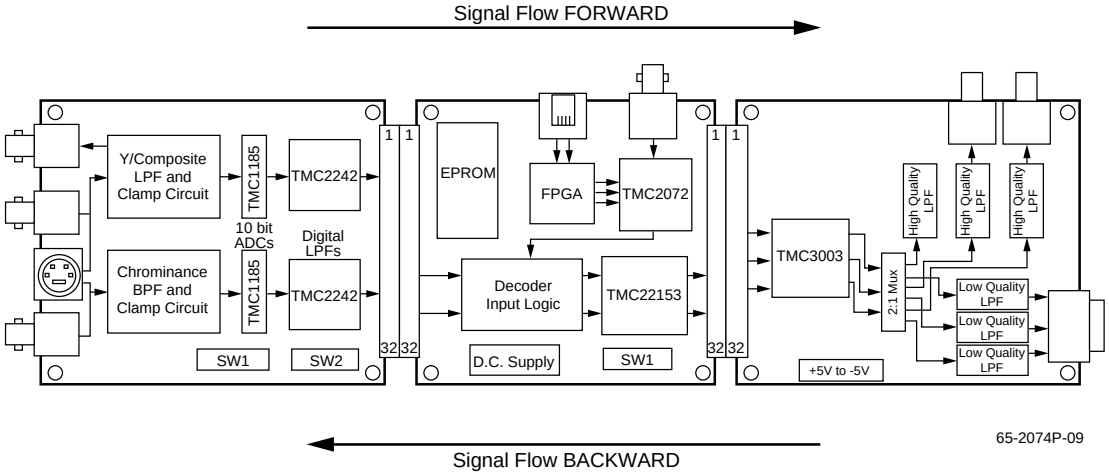
Table 2. TMC2074P7C Parts List (continued)

Item	Qty.	Part Mfr./Number	Reference	Part
38	1	MiniReel: 615-375	R14	750
39	1	MiniReel: 615-449	R16	5K (4.99k)
40	1	MiniReel: 615-347	R17	475
41	1	ITT Canon: KSC221JB	S1	MRST
42	1	ALCOSWITCH: ADP-8	S2	SW DIP-8
43	1	Mouser: ME151-203-100	TP1	+5V
44	1	Mouser: ME151-203-100	TP2	-5V
45	5	Mouser: ME151-203-100	TP3,TP4,TP5,TP6,TP7	GND
46	6	Mouser: ME151-203-100	TP8,TP9,TP10,TP11, TP16,TP17	TP
47	1	Mouser: ME151-203-100	TP12	HSYNC
48	1	Mouser: ME151-203-100	TP13	SELC
49	1	Mouser: ME151-203-100	TP14	CBSEL
50	1	Mouser: ME151-203-100	TP15	VSYNC
51	1	Motorola: MC74F14D	U1	74F14
53	1	R/N: ICE-203-S-TG30	U2	20 Pin Dip Socket
54	1	TMC2490RO	U3	TMC2490
55	1	Motorola: MC74ACT273DW	U4	74ACT273
56	1	ECLIPTEK: ECL1145-27.000M	Y1	27MHz TTL Clock
57	1	Atmel AT89C2051-16PC	U2X	AT89C2051

INPUT 96 Way Connector (Female)

row A		row B		row C	
32	+5v	32	GND	32	+5v
31	D1 or R/V [bit 0]	31	+5V	31	GND
30	D1 or R/V [bit 1]	30	+5V	30	PXCK
29	D1 or R/V [bit 2]	29	+5V	29	GND
28	D1 or R/V [bit 3]	28	GND	28	PCK
27	D1 or R/V [bit 4]	27	Analog Composite/luma	27	GND
26	D1 or R/V [bit 5]	26	GND	26	CREF
25	D1 or R/V [bit 6]	25	Analog chroma	25	GND
24	D1 or R/V [bit 7]	24	XEN	24	$\overline{\text{VSYNC}}$
23	D1 or R/V [bit 8]	23	GND	23	$\overline{\text{HSYNC}}$
22	D1 or R/V [bit 9]	22	XDIR	22	HREF
21	Comp, G/Y, or Luma [bit 0]	21	$\overline{\text{XHSYNC}}$	21	VREF
20	Comp, G/Y, or Luma [bit 1]	20	$\overline{\text{XVSYNC}}$	20	ODD IN
19	Comp, G/Y, or Luma [bit 2]	19	XPXCK	19	GND
18	Comp, G/Y, or Luma [bit 3]	18	XRS [bit 3]	18	NTSC/PAL
17	Comp, G/Y, or Luma [bit 4]	17	XRS [bit 2]	17	CLAMP pulse
16	Comp, G/Y, or Luma [bit 5]	16	XRS [bit 1]	16	RGB
15	Comp, G/Y, or Luma [bit 6]	15	XRS [bit 0]	15	
14	Comp, G/Y, or Luma [bit 7]	14	GND	14	
13	Comp, G/Y, or Luma [bit 8]	13	-5V	13	
12	Comp, G/Y, or Luma [bit 9]	12	-5V	12	LOCK
11	Chroma or B/U [bit 0]	11	-5V	11	D1
10	Chroma or B/U [bit 1]	10	GND	10	$\overline{\text{RESET}}$
9	Chroma or B/U [bit 2]	9	PGM_IN	9	SCL
8	Chroma or B/U [bit 3]	8	-12V	8	GND
7	Chroma or B/U [bit 4]	7	-12V	7	SDA
6	Chroma or B/U [bit 5]	6	IE (input enable)	6	OE (output enable)
5	Chroma or B/U [bit 6]	5	GND	5	$\overline{\text{BLANK}}$ (DAC)
4	Chroma or B/U [bit 7]	4		4	
3	Chroma or B/U [bit 8]	3		3	
2	Chroma or B/U [bit 9]	2	+12V	2	+12V
1	GND	1	GND	1	GND

Input Edge Connector Design Notes



Boards with different revision letters may not be compatible. Damage may occur if they are connected together!

- XPXCK is a two times pixel clock fed BACKWARD.
- XHSYNC and XVSYNC are timing reference signals fed BACKWARD.
- The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD. A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc.
- XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
- PGM_IN is a negative going pulse, logically ANDed with the onboard program start pulse, for initiating the programming sequence for components on that board. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. Minimum width of PGM_IN is 1μS.
- The RESET pin on the input edge connector should be connected directly to the RESET pin on the output connector. A link should be used to connect any pulse to the RESET line.
- The MASTER/SLAVE, XDIR, PGM_IN and RESET pins on the input edge connector should be connected to +5V through a 10k pull up resistor.
- The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

Related Products

- TMC2068P7C Decoder demonstration board
- TMC2067P7C ADC demonstration board
- TMC2070P7C RBUS Interface
- TMC2071P7C Parallel D1 interface board
- RayDemo software

Notes:

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2074P7C	25°C	27 MHz	Commercial	4" by 5" Printed Circuit Board	TMC2074P7C

A schematic database is available in OrCAD™ format. Contact the factory.

The TMC2074P7C Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

FCC Compliance

This device has not been approved by the Federal Communications Commission (FCC). This board is intended for the evaluation of Fairchild products only. This device is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.

Preliminary Information