TMC2601

Digital Video Serial Transmission Encoder 8- or 10-bit Parallel Data Into Serial Format 140–370 MHz Output Frequency

Features

- 0.6 µ CMOS technology
- Single +5 V power supply
- 44 pin PQFP or PLCC
- 0.5 W typical power dissipation
- 140-370 Megabit/s data rate
- Complies with the following digital video interface standards:
  - SMPTE 259MBit-Serial 4:2:2 Component (D1)
  - SMPTE 125MBit-Parallel 4:2:2 Component (D1)
  - SMPTE 244MBit-Parallel 4*f_{SC} NTSC Composite (D2)
- Accepts 8- or 10-bit TTL or CMOS-compatible parallel data
- Outputs differential pseudo-ECL serial data and clock
- Byte sync on Timing Reference Signal (TRS)
- Modulo - 2 division by G(X) = (X^9+X^4+1)*(X+1) scrambler
- Phase-locked loop clock synthesizer
- Transmitter jitter < 500 ps at 270 Mb/s
- Power saving feature on unused clock and data outputs

Applications

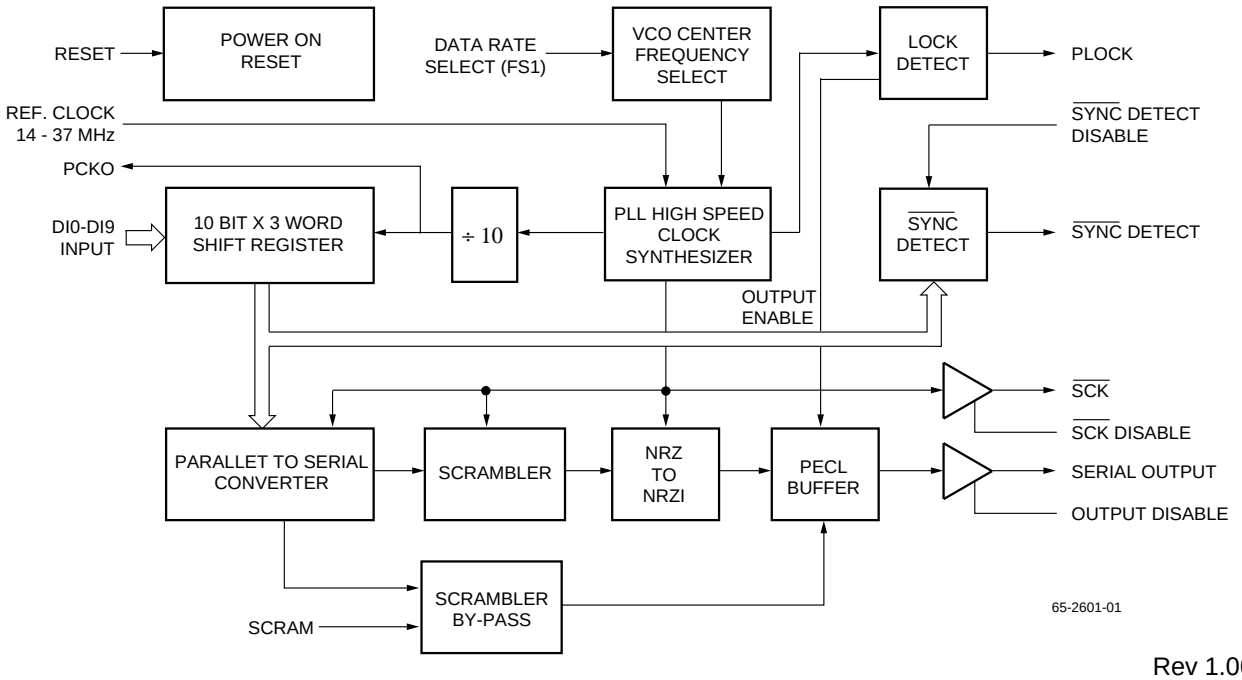
- Encoder for 140 to 370 Mb/s serial data
- Serial transmission interface for:
  - Video cameras 360 Mb/s
  - 4:2:2 signals 270 Mb/s
  - 4*f_{sc} PAL 177 Mb/s
  - 4*f_{sc} NTSC 143 Mb/s

Description

The TMC2601 is a CMOS integrated circuit which can serialize 8- or 10-bit parallel data streams, including SMPTE 125M, CCIR 656, and SMPTE 244M. Fixed functions include parallel-to-serial conversion and 10-fold clock frequency multiplication. The user may also enable sync (TRS word) detection, data scrambling (X^9+X^4+1), and conversion of NRZ serial data into NRZI format (X+1). Using control bis FS_{1-0}, the user may select a nominal operating frequency of 143, 177, 270, or 360MHz.

The TMC2601 provides pseudo-ECL outputs: complementary for the serial data and serial clock, single-ended for the regenerated parallel clock. It requires a single 5-volt supply and consumes less than 1/2 watt while driving 100-ohm loads.

Block Diagram



Rev 1.00

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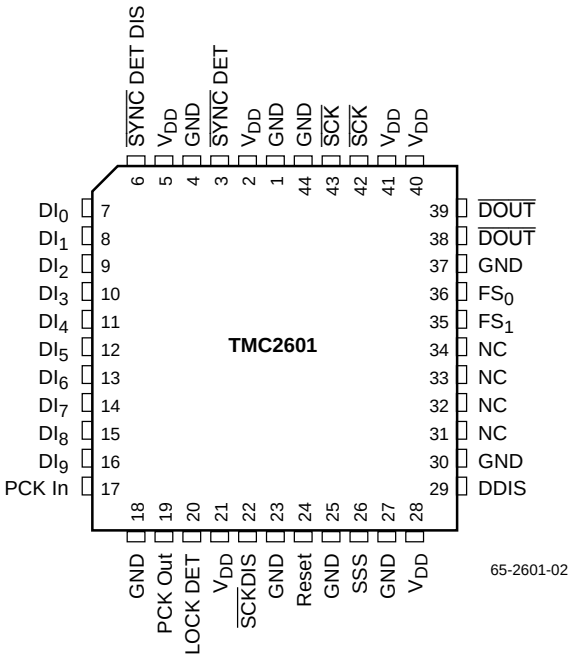
Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
GND	1	Supply	Ground
V_{DD}	2	Supply	+5V supply
$\overline{SYNC}$ DET	3	TTL out	TRS detected flag. If and only if DI_{9-2}=FFh or 00h, flag does low on the following clock cycle.
GND	4	Supply	Ground
V_{DD}	5	Supply	+5V supply
$\overline{SYNC}$ DET DIS	6	TTL in	TRS formatter disable. When low, chip forces DI_{1-0} to 00b if DI_{9-2}=00h and to 11b if DI_{9-2}=FF. When high, passes input data unaltered.
DI_{0-9}	7-16	TTL in	Bit-parallel Input data DI_0 is LSB in 10-Bit mode LSB, DI2 is LSB in 8-Bit mode. DI_9 is MSB in all modes
PCK In	17	TTL in	Parallel clock input. Rising edge strobes DI9-0 into chip.
GND	18	Supply	Ground
PCK Out	19	ECL out	Parallel clock output. This pseudo-ECL signal is derived from the internal VCO and maintains a constant phase relationship with PCKI when the loop is locked.
LOCK DET	20	TTL out	Phase locked flag goes high when the loop is locked.
V_{DD}	21	Supply	+5V supply

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Pin Function Description
$\overline{\text{SCK}}$DIS	22	TTL in	Grounding this pin disables the serial clock output.[1]
GND	23	Supply	Ground
Reset	24	TTL in	When forced high, this pin (which has an internal pull-down) resets the part.
GND	25	Supply	Ground
SSS	26	TTL in	When high, this pin bypasses the scrambler and NRZI conversion blocks, providing direct serialization of the data.
GND	27	Supply	Ground
V_{DD}	28	Supply	+5V supply
DDIS	29	TTL in	Grounding this pin disables the serial data output.[1]
GND	30	Supply	Ground
NC	34:31	NC	May be grounded directly or via a resistor.
FS_{1-0}	35-36	TTL in	Frequency select input. Selects VCO frequency range
GND	37	Supply	Ground
$\overline{\text{DOUT}}$	38	ECL out	Differential pseudo-ECL serial data output requiring an external >100-ohm resistor to $\overline{\text{DOUT}}$.
$\overline{\text{DOUT}}$	39	ECL out	Differential serial data output, compement of $\overline{\text{DOUT}}$.
V_{DD}	40	Supply	+5V supply
V_{DD}	41	Supply	+5V supply
$\overline{\text{SCK}}$	42	ECL out	Differential pseudo-ECL serial clock output, requiring external 100-ohm resistor to $\overline{\text{SCK}}$.
$\overline{\text{SCK}}$	43	ECL out	Differential serial clock output, complement to $\overline{\text{SCK}}$.
GND	44	Supply	Ground

Note

1. These pins may be left open or AC coupled. Do not DC couple to ground unless the corresponding output is to be disabled; logic 1 or high-Z (due to internal pull up) enables the output and 0 disables it.

Functional Description

The TMC2601 serializer is a CMOS integrated circuit which converts parallel data in a format such as SMPTE125M or SMPTE244M into a serial format, such as SMPTE 259M. It encodes 8- or 10-bit TTL-compatible parallel signals into serial differential pseudo-ECL signals at up to 370Mb/s. It operates from a single 5V supply and is packaged in a 44-pin PLCC.

The internal functional blocks include the sync detector, data serializer, polynomial scrambler and NRZ to NRZI converter, and 10-fold clock frequency multiplier.

Sync Detector

On each rising edge of PCKI, the Sync Detector looks for combinations of all 1's or all 0's on pins DI_{9-2}. Whenever it encounters one of these combinations, the Sync Detector drives $\overline{SYNC}$ DET low on the next parallel clock cycle. If control $\overline{SYNC}$ DET DIS is low, it also overrides DI_{1-0} to match DI_{9-2}, such that 000 through 003 (hex) become 000, and 3FC through 3FF become 3FF, to comply with SMPTE259.

Polynomial Scrambler

This feedback shift register pseudorandomizes the incoming data, using the SMPTE-specified fixed polynomial $X^9 + X^4 + 1$, thereby minimizing the DC component in the output stream. A second polynomial operator, cascaded with the first and based on X+1, converts NRZ data into NRZI, turning any long sequences of 1's into series of transitions. When high, control SSS bypasses these two blocks, allowing direct serialization of the incoming data.

Phase-Locked Loop

The PLL, which multiplies the clock frequency by 10, comprises a phase detector, a charge pump, a loop filter, a VCO, and a divide-by-ten counter. On each parallel clock cycle, the loop filter receives a charge proportional to the phase error and perturbs the VCO's frequency appropriately.

VCO Frequency Selector

The chip provides four nominal frequency ranges, selected by FS_{1-0}, as follows:

FS_0	FS_1	Nominal Frequency (MHz)
0	0	270 (D1)
0	1	360
1	0	143 (NTSC D2)
1	1	177 (PAL D2)

The lock detect circuit disables the serial data output when the loop is not locked, at which time the Lock Detect flag will be low.

Complementary serial data emerge on $\overline{SDO}$ and $\overline{SDO}$, whereas the serial clock appears on $\overline{SCK}$ and $\overline{SCK}$. To reduce system noise and to save power, user not needing the serial clock may disable it by grounding LOOPF/$\overline{SCK}$DIS.

The chip also provides a single-ended ECL parallel clock output, PCKO, regenerated from the internal PLL.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Power Supply Voltage, V_{DD}	-0.5		7.0	V
Digital Inputs				
Applied Voltage [2]	-0.5		V_{DD} + 0.5	V
Forced Current [3,4]	-20.0		20.0	mA
Outputs				
Applied Voltage [2]	-0.5		V_{DD} + 0.5	V
Forced Current [3,4]	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH State to GND)				
Temperature				
Operating, Ambient	0		70	°C
Junction			140	°C
Storage	-65		150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	4.75		5.25	V
V_{IH}	Digital inputs, HIGH	2.0			V
V_{IL}	Digital inputs, LOW			0.8	V
t_S	Data setup (to PCKI rising edge)	5			ns
t_H	Data hold (from PCKI rising edge)	0			ns
tPWH	Parallel clock pulse width HIGH (PCKI)	8			ns
tPWL	Parallel clock pulse width LOW (PCKI)	8			ns

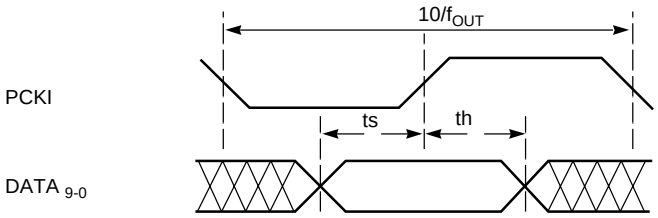
Electrical Characteristics

Parameter		Min.	Typ.	Max.	Units
Power Consumption I_{DD}				800	mW
V_{OHS}	Serial output high logic level, from V_{DD}	-0.875		-0.7	V
V_{OLS}	Serial output low logic level, from V_{DD}	-1.8		-1.5	V
V_{OHP}	TTL output high logic level	2.4			V
V_{OLP}	TTL output low logic level			0.5	V
I_{IH}	TTL input high current	-50		50	
I_{IL}	TTL input low current	-50		50	

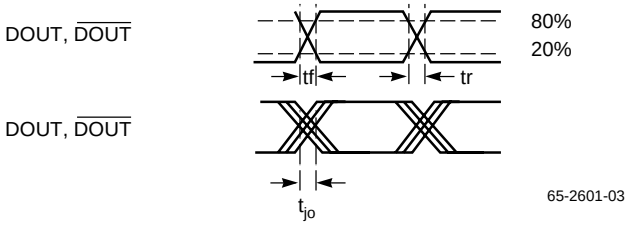
Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output clock & bit rate	R_L=100 ohms	110		400	MHz
V_{SD}	Output data & clock amplitude, p-p		700		850	mV
t_{jo}	Output clock jitter	270Mb/s			700	ps
t_D	Serial clock to data lag			1.4		ns
SDO t_R/t_F	Serial Data Output Rise/Fall time			650		
t_{LOCK}	Lock Time			25		
f_{PCKOUT}	Parallel Clock Output Frequency		11			40
PCKOUT t_R/t_F	Parallel Clock Output Rise/Fall Time			700		
V_{PCKOUT}	Parallel Clock Output Signal Swing			950		
$t_{jPCKOUT}$	Parallel Clock Output Jitter					700

Input Timing



Output Timing



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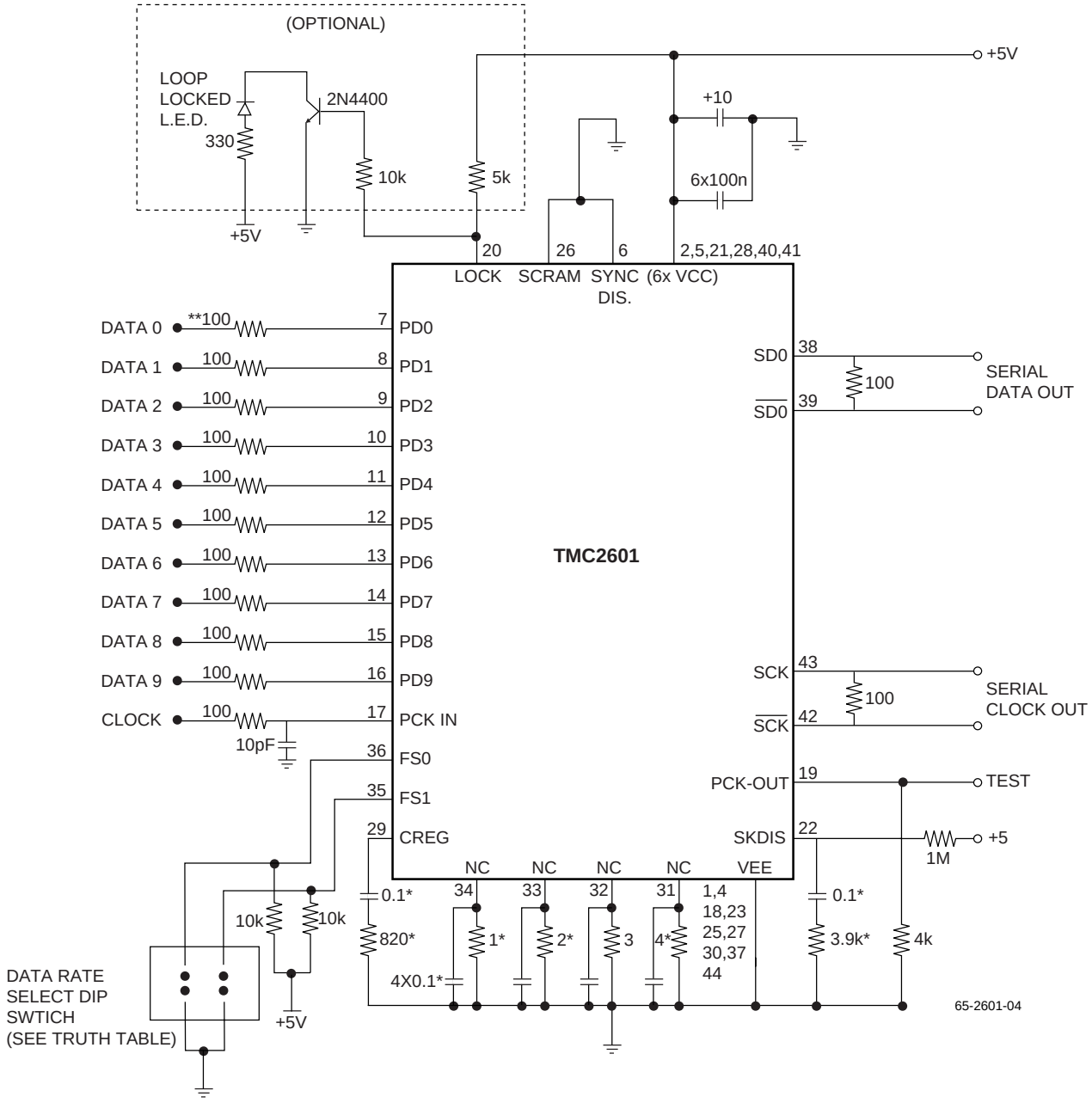
Typical Application Circuit



Notes:

All resistors in ohms, all capacitors in microfarads unless otherwise stated.

*These components may be omitted, without affecting functionality. See Text.

**These resistors slow down fast INPUT edges (≤500ps) and prevent the input signals from ringing.

Equivalent Circuits and Threshold Levels

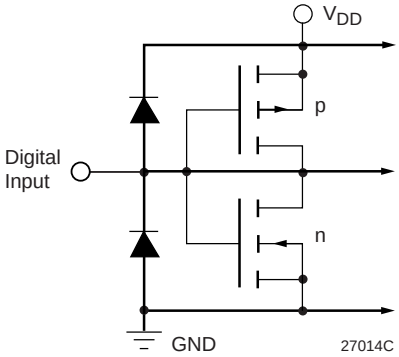


Figure 1. Equivalent Digital Input Circuit

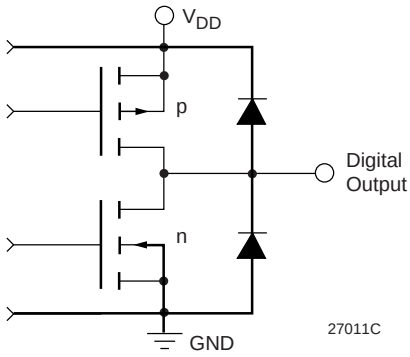


Figure 2. Equivalent Digital Output Circuit

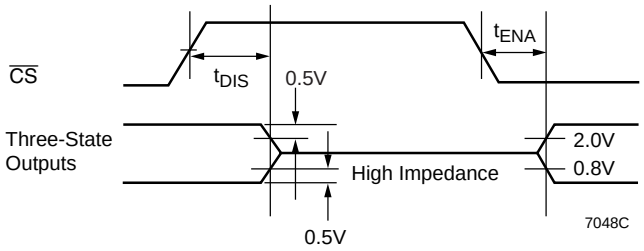


Figure 3. Threshold Levels for Three-State Measurements

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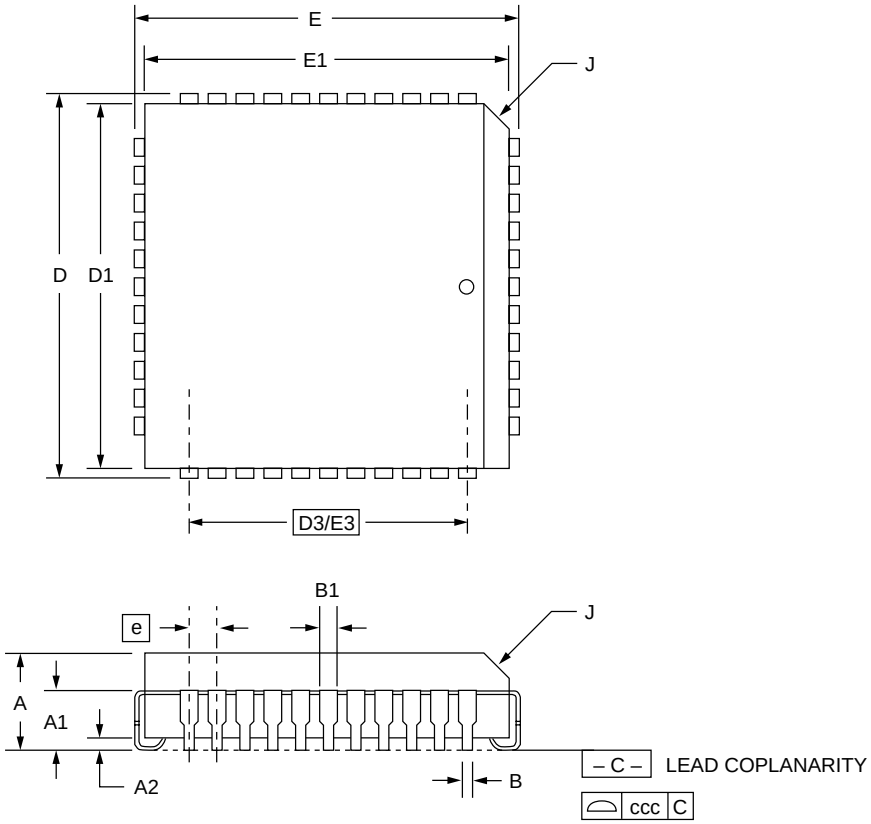
Notes:

Mechanical Dimensions – 44-Pin PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.20	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2601R2C	0°C to 70°C	Commercial	44-Lead PLCC	2601R2C

8/30/99 0.0m 002
Stock#DS30002601