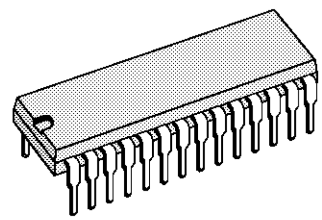
SGS-THOMSON MICROELECTRONICS

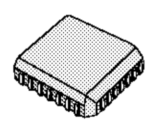
TS68951

MODEM RECEIVE ANALOG INTERFACE

- TWO CHANNEL 12-BIT ANALOG TO DIGITAL CONVERTER FOR RECEPTION OF DIGITAL DATA FROM THE TELEPHONE LINE AND ECHO CANCELLATION (WITH ASYNCHRONOUS MULTIPLEXING OF 2 PLESIOCHRONOUS CHANNELS)
- PROGRAMMABLE SWITCHED CAPACITOR BAND-PASS FILTER
- PROGRAMMABLE GAIN AMPLIFIER FROM 0 TO 46.5dB WITH 1.5dB STEPS
- PROGRAMMABLE BACK CHANNEL REJECTION AND RECONSTRUCTION FILTER
- CARRIER LEVEL DETECTOR WITH PROGRAMMABLE THRESHOLD
- DIRECT INTERFACE WITH STANDARD MPU 8-BIT BUS
- LOW POWER CMOS TECHNOLOGY
- AVAILABLE IN DIL OR SURFACE MOUNT PACKAGE



DIP28
(Plastic Package)



PLCC28
(Plastic Chip Carrier)

DESCRIPTION

The TS68951 is a Receive (Rx) Analog Front-End circuit designed to implement the analog to digital conversion and filtering required by high-speed voice-band modems or speech coding applications using digital signal processing technology.

The TS68951 meets all the CCITT recommendations from V.22 to V.33 including full-duplex recommendations with echo-cancellation (V.32) thanks to its multiplexed 2nd channel.

Used in conjunction with the TS68950 Transmit (Tx) Analog Front-End circuit and the TS68952 clock generator*, it provides a very cheap and efficient interface to digital signal processing functions in high speed modems or telephony applications.

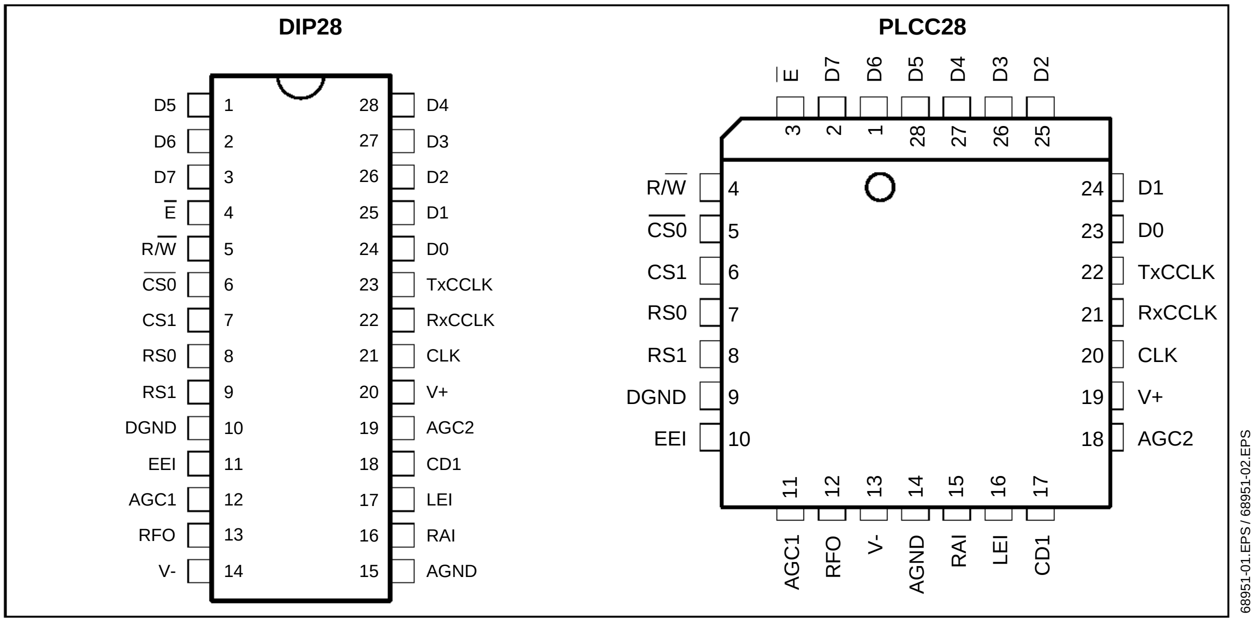
*The interconnection between the 3 chips of the Modem Analog Front End (MAFE) is decribed page 13.

ORDER CODES

Part Number	Temperature Range	Package
TS68951CP	0 to +70°C	DIP28
TS68951CFN	0 to +70°C	PLCC28

68951-01.TBL

PIN CONNECTIONS



PIN DESCRIPTION

Name	Description
D5-D7	Data Bus
$\overline{E}$	Enable Input. Enables Selection Inputs. Active On a Low Level for Read Operation. Active On a Positive Edge for Write Operation.
R/$\overline{W}$	Read/write Selection Input. Read operation is selected on a high level. Write operation is selected on a low level.
$\overline{CS0}$-CS1	Chip Select Inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	Register Select Inputs. Select the register involved in a read or write operation.
DGND	Digital Ground. All digital signals are referenced to this pin.
EEI	Estimated Echo Input. When operating in echo cancelling mode, this signal is added to the reception bandpass filter output.
AGC1	Analog input of the automatic gain control amplifier and of the carrier level detector
RFO	Reception Filter Analog Output. Designed to be connected to AGC1 input through a 1µF non polarised capacitor.
V^-	Negative Power Supply. V^- = -5V ±5%
AGND	Analog Ground. All analog signals are referenced to this pin.
RAI	Receive Analog Input. Analog input tied to the transmission line.
LEI	Local Echo Input. Analog input substracted from the receive anti-aliasing filter output.
CD1	This pin must be connected to the analog ground through a 1µF non polarised capacitor, in order to cancel the offset voltage of the carrier level detector amplifier.
AGC2	This pin must be connected to the analog ground through a 1µF non polarised capacitor, in order to cancel the offset voltage of the AGC amplifier.
V^+	Positive Power Supply V^+ = +5V ±5%
CLK	Master Clock Input. Nominal Frequency 1.44MHz.
RxCCLK	Receive Conversion Clock
TxCCLK	Transmit Conversion Clock
D0-D4	Data Bus

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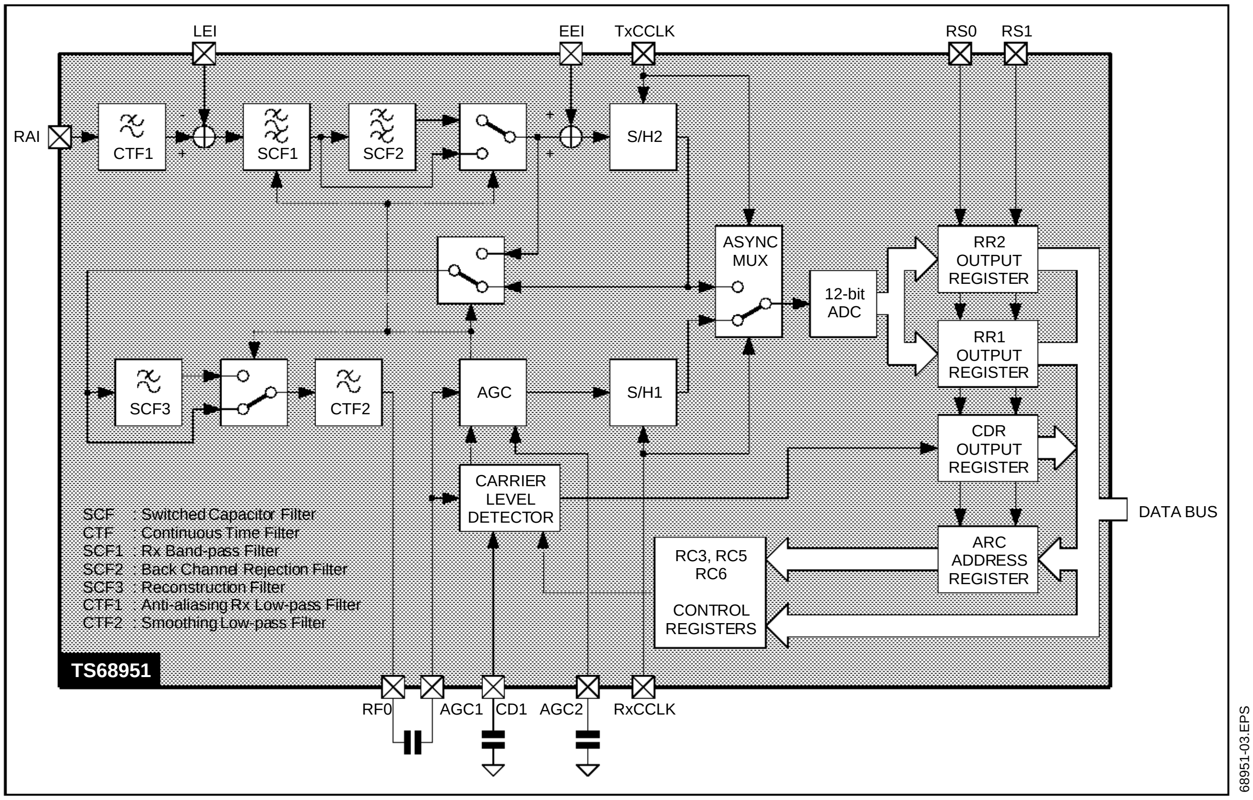
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TS68951 is a received analog interface for voice-band MODEM. It is able to perform the receive interface function for three types of synchronous MODEM :
- Four-wire or two-wire half duplex MODEM.
- Two-wire full duplex band-split MODEM.
- Two-wire full duplex echo cancelling MODEM.

Four/Two Wire Half Duplex Modem Two Wire Band Split Modem

In these modes of operation, EEI input must be tied to the analog ground. The analog signal treatment of receive input is shown in Figure 5.

Programming requirements :
- Band-pass filter cut-off frequencies.
- Back channel rejection filter (presence or absence according to the application).
- SCF1 or SCF2 output as input of CTF2.
- AGC gain.
- Carrier level detector threshold.

The receive samples are coded at RxCCLK rate and can be read from receive register (RR1).

Two Wire Echo Cancelling Modem

This mode of operation uses the full capabilities of the TS68951. The analog treatment of receive input is shown in Figure 6. The echo cancelling operation is achieved by means of subtraction of the LEI signal from the output of CTF1 duplexer and addition of the EEI signal to the output of SC1.
After the local echo reduction by the duplexer the resultant signal consists of the receive signal plus the echo signal generated by the transmission line mismatch : this undesirable signal is then cancelled at the output of the Rx band-pass filter.

Programming requirements :
- Band-pass filter cut-off frequencies.
- SCF1 output as input of S/H2.
- Output of S/H2 as input of SCF3 and output of SCF3 as input of CTF2.
- AGC gain.
- Carrier level detector threshold.

Residual signal samples from S/H2 output are coded at TxCCLK rate and can be read from receive register 2 (RR2), hence the signal processor may correlate them with the transmit samples to update the coefficients of the filter that generates the estimated echo.

The receive signal samples are coded at RxCCLK rate and can be read from receive register 1 (RR1).

FUNCTIONAL SPECIFICATIONS

Bus and Registers Control

For any operation involving bus and registers, the chip select bits CS0 and CS1 must be active ($\overline{CS0}$ = 0 and CS1 = 1).

The seven internal registers are divided into four write only registers and three read-only registers.

Write Operation

There are three control registers (RC3, RC5, RC6) and one address register (ARC) which can be written ; but only ARC can be directly addressed.

The control registers are indirectly addressed by the word contained in ARC according to Table 1.

Table 1

Addressed Control Register	Word Contained in ARC							
	D7	D6	D5	D4	D3	D2	D1	D0
RC3	0	1	0	X	X	X	X	X
RC5	1	0	0	X	X	X	X	X
RC6	1	0	1	X	X	X	X	X

X : don't care

When a write operation is selected (refer to Table 3) the data present on the bus are strobed on a positive edge of $\overline{E}$ and the content of ARC is incremented.

Note : Addresses of RC3 and RC5 are separated by two increments.

Read Operation

There are two 12-bit receive registers (RR1, RR2) and a 1-bit carrier detector register (CDR).

RR2 contains the coded samples of the residual signal and RR1 the coded samples of the receive signal.

The active bit of CDR is D7:D0 to D6 are forced to 0.

When the RMS value of CTF2 output is greater than the programmed threshold, bit 7 of CDR is set. The nominal response time of the carrier detector to a signal settlement or removal is 1.78ms.

When a read operation is selected (refer to Table 3) the data are sent to the bus on a low level of $\overline{E}$; a high level on $\overline{E}$ sets the output bus drivers in a high impedance state.

As the data bus has only 8 bits, the contents of RR1 or RR2 must be read in two cycles. The four less significant bits are transferred in the first cycle and the eight most significant bits are transferred in the second cycle according to the format, Table 2.

Table 2

	D7	D6	D5	D4	D3	D2	D1	D0
First Cycle	RRx3	RRx2	RRx1	RRx0	0	0	0	0
Second Cycle	RRx11	RRx10	RRx9	RRx8	RRx7	RRx6	RRx5	RRx4

Table 3

$R/\overline{W}$	RS0	RS1	Operation
0	1	1	Write Control Register Addressed by ARC
0	1	0	Write Address Register (ARC)
1	0	1	Read Receive Register 2 (RR2) (residual signal sample)
1	0	0	Read Receive Register 1 (RR1) (receive signal sample)
1	1	0	Read Carrier Detector Register (CDR)

An internal latch selects the first or the second byte and is automatically incremented on a positive edge of $\overline{E}$ when one of the receive registers is addressed. This latch is not reset at power-on, so it needs to be reset before the first read operation: reset occurs on any positive edge of $\overline{E}$ for any operation, provided none of the receive registers is addressed ; the first byte is selected when reset.

RR1 and RR2 Output Code

The output code is a 2's complement delivering values from -2048 up to +2047. Since the converter codes voltage between $-V_{REF}$ and $+V_{REF}$, the theoretical decision voltage corresponding to code C can be computed as follows :

$$V_C = \frac{2C+1}{4095} V_{REF}$$

Where V_{REF} is the reference voltage of the A/D converter, V_{REF} nominal value is 2.5V and C is the algebraic value of code C.

Example :
Assume the output code is the hexadecimal value $8B1 ; the algebraic value of this code C = -1871 therefore V_C = -2.283V.

CONTROL REGISTERS DESCRIPTION

Power-on

The control registers are not initialised at power-on ; they must be initialised before reading any word from the output registers.

Register RC3

The contents of RC3 sets the -3dB cut-off frequencies of SCF1 receive band-pass filter, determines the presence or the absence of SCF2 back channel rejection filter and of SCF3 reconstruction filter, and selects receive signal path to the second filtering section ; without echo-cancelling the output of SCF1 or SCF2 is selected ; with echo-cancelling the output of S/H2 is selected.

The band-pass filter consists of a 5th-order elliptic low-pass filter and of a 2nd order high-pass filter whose cut-off frequencies can be programmed by (LP1, LP2) and (HP1, HP2) respectively (refer Table 4).

The rejection filter is present when REJ bit is high.

The reconstruction filter is present when REC bit is high.

S/H2 output is selected when S/A bit is high.

Register RC5 (Table 5)

The content of RC5 sets the gain of the AGC amplifier between 0dB and 46.5dB with 1.5dB steps.

Note : The AGC loop control is performed by the signal processor.

Register RC6

The content of RC6 sets the carrier level detector threshold (Refer to Table 6).

The threshold values are grouped by pair ; values belonging to each pair have 2.5dB separation which allows the signal processor to perform software hysteresis.

Table 4

D7 HP2	D6 HP1	D5 LP2	D4 LP1	D3 REJ	D2 S/A	D1 REC	D0	RC3 Register		
								Low-pass Filter		
								Sampling Frequency Fs (kHz)	**-3dB Cut-off Frequency** (Hz)	
		0 0 1 1	0 1 0 1				x x x x	72 144 288 288	800 1600 3200 3200	
								High-pass Filter		
								Sampling Frequency Fs (kHz)	**-3dB Cut-off Frequency** (Hz)	
0 1 1	x 0 1			0 0 0			x x x	36 72 144	250 500 1600	
								High-pass and Rejection Filter		
								Sampling Frequency (kHz)	**-3dB Cut-off Frequency** (Hz)	**Rejected Band** (Hz)
1 1	0 1			1 1			x x	72 144	800 2200	370-470 800-1600
								S/H2 Selection		
					0 1		x x	Deselected Selected		
								Reconstruction Filter Selection		
						0 1	x x	Deselected Selected	(sampling frequency Fs = 288kHz)	

X : don't care

Table 5

D7	D6	D5	D4	D3	D2	D1	D0	RC5
								AGC Gain (dB)
0	0	0	0	0	x	x	x	0
0	0	0	0	1	x	x	x	1.5
0	0	0	1	0	x	x	x	3
0	0	0	1	1	x	x	x	4.5
0	0	1	0	0	x	x	x	6
0	0	1	0	1	x	x	x	7.5
0	0	1	1	0	x	x	x	9
0	0	1	1	1	x	x	x	10.5
0	1	0	0	0	x	x	x	12
0	1	0	0	1	x	x	x	13.5
0	1	0	1	0	x	x	x	15
0	1	0	1	1	x	x	x	16.5
0	1	1	0	0	x	x	x	18
0	1	1	0	1	x	x	x	19.5
0	1	1	1	0	x	x	x	21
0	1	1	1	1	x	x	x	22.5
1	0	0	0	0	x	x	x	24
1	0	0	0	1	x	x	x	25.5
1	0	0	1	0	x	x	x	27
1	0	0	1	1	x	x	x	28.5
1	0	1	0	0	x	x	x	30
1	0	1	0	1	x	x	x	31.5
1	0	1	1	0	x	x	x	33
1	0	1	1	1	x	x	x	34.5
1	1	0	0	0	x	x	x	36
1	1	0	0	1	x	x	x	37.5
1	1	0	1	0	x	x	x	39
1	1	0	1	1	x	x	x	40.5
1	1	1	0	0	x	x	x	42
1	1	1	0	1	x	x	x	43.5
1	1	1	1	0	x	x	x	45
1	1	1	1	1	x	x	x	46.5

X : don't care

Table 6

D7	D6	D5	D4	D3	D2	D1	D0	RC6
								Threshold (dBm)
0	0	0	x	x	x	x	x	-29.85
0	0	1	x	x	x	x	x	-27.35
0	1	0	x	x	x	x	x	-36.65
0	1	1	x	x	x	x	x	-34.15
1	0	0	x	x	x	x	x	-46.75
1	0	1	x	x	x	x	x	-44.25
1	1	0	x	x	x	x	x	-46.75
1	1	1	x	x	x	x	x	-44.25

X : don't care

Clock

The master clock CLK, the receive conversion clock (RxCCLK) and the transmit conversion clock (TxCCLK) are generated in the TS68952 clock generator. There are three possible frequencies for the conversion clocks : 7.2kHz, 8kHz and 9.6kHz.

The nominal values of the RxCCLK and TxCCLK clocks must be identicals (these clocks are plesiochronous and real values within ±100ppm according to CCITT recommandations).

The frequency of RxCCLK and TxCCLK is controlled by two independant Digital Phase Locked Loops (DPLL). TxCCLK can be synchronised on an external Terminal Clock (TxSCLK) or on the Rx bit rate clock ; in these cases 350ns discrete phase shifts occurs on CLK and TxCCLK synchronously with TxCCLK negative edge with a repetition rate of 600Hz, 800Hz or 1000Hz according to the programmation of RC1 control register in the TS68952.

A/D Conversion

The A/D converter is a 12 bit resolution, 8-bit minimum integral linearity, monotonic converter. The input voltage ranges from – 2.5V to + 2.5V ; and the conversion time is better than 50µs.

Asynchronous Multiplexing

Samples on the output of S/H1 and S/H2 are converted respectively at RxCCLK frequency and TxCCLK frequency.

Since RxCCLK and TxCCLK are plesiochronous, the order of conversion is determined by an asynchronous logic.

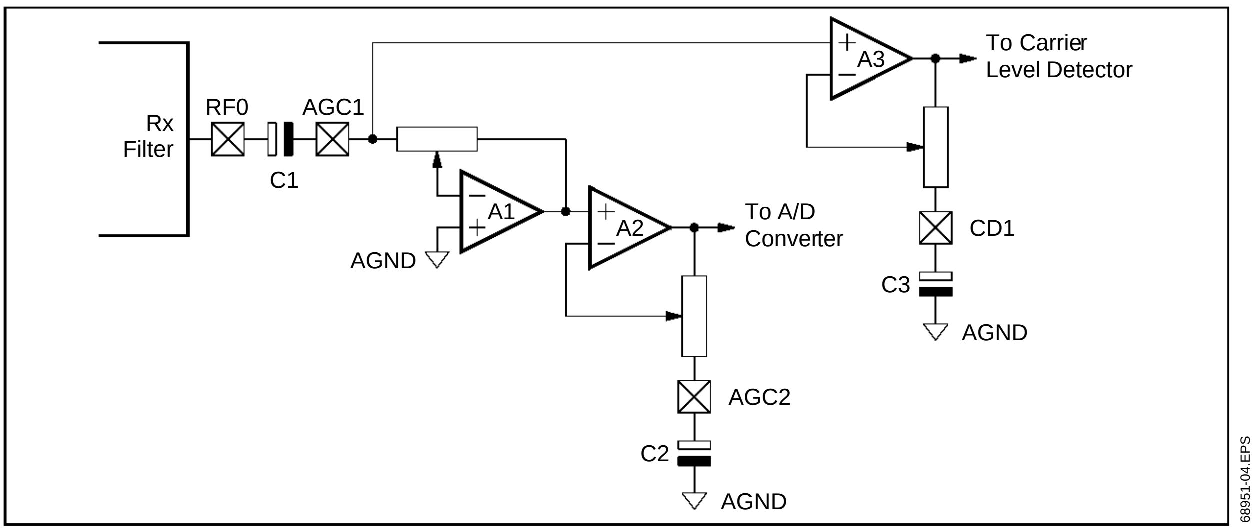
The output register RR1 and RR2 are respectively loaded on the negative edge of RxCCLK and TxCCLK.

AGC and CLD Amplifiers

The AGC consists of two cascaded amplifiers A1 and A2 (see Figure 1) AC coupling is obtained from C1 and C2 external capacitors. C2 can be used as an auxiliary input for performing an analog loop located after echo cancellation.

The carrier level detector (CLD) amplifier A3 also needs an external capacitor C3.

Figure 1 : Rx Amplifiers Schematic



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Supply Voltage between V^+ and AGND or DGND	-0.3, +7	V
	Supply Voltage between V^- and AGND or DGND	-7, +0.3	V
	Voltage between AGND and DGND	-0.3, +0.3	V
	Digital Input Voltage	DGND -0.3, V^+ +0.3	V
	Digital Output Voltage	DGND -0.3, V^+ +0.3	V
	Digital Output Current	-20, +20	mA
	Analog Input Voltage	V^- -0.3, V^+ +0.3	V
	Analog Output Voltage	V^- -0.3, V^+ +0.3	V
	Analog Output Current	-10, +10	mA
P_{tot}	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-65, +150	°C

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ELECTRICAL CHARACTERISTICS

The electrical specifications are given for Operating Temperature range (0°C, 70°C).

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLIES (DGND = AGND = 0V)					
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	-5.25		-4.75	V
I^+	Positive Supply Current (receive signal level 0dBm)			20	mA
I^-	Negative Supply Current (receive signal level 0dBm)	-20			mA
DIGITAL INTERFACE (Control Inputs - Voltages referenced to DGND = 0V)					
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.2			V
V_{IL}	Low Level Input Current (DGND < V_I < 0.8V)	-10		10	µA
V_{IH}	High Level Input Current (2.2V < V_I < V^+)	-10		10	µA
DATA BUS (Voltages referenced to DGND = 0V)					
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.2			V
V_{OL}	Low Level Output Voltage (I_{OL} = 2.5mA)			0.4	V
V_{OH}	High Level Output Voltage (I_{OL} = 2.5mA)	2.4			V
I_{OZ}	High Impedance Output Current (when $\overline{E}$ is high and DGND < V_I < V^+)	-50		50	µA
ANALOG INTERFACE (All voltages referenced to AGND = 0V)					
V_{in}	Input Voltage EEI, LEI, RAI	-2.5		2.5	V
I_{in}	Input Current EEI, LEI, RAI (-2.5V < V_{in} < 2.5V)	-1		1	µA
R_{in}	Input Resistance AGC1, AGC2	1.5			kΩ
R_{in}	Input Resistance CD1	0.7			kΩ
V_{out}	Output Voltage RFO (C_L = 50pF, R_L = 1kΩ)	-2.5		2.5	V
R_{out}	Output Resistance RFO			2	Ω
R_L	Load Resistance RFO	1			kΩ
C_L	Load Capacitance RFO			50	pF

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BUS TIMING CHARACTERISTICS (see Notes 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	320			ns
t_{WEL}	Pulse Width $\overline{E}$ Low Level	180			ns
t_{WEH}	Pulse Width $\overline{E}$ High Level	100			ns
t_r, t_f	Clock Rise and Fall Time			20	ns
t_{HCE}	Control Signal Hold Time	10			ns
t_{SCE}	Control Signal Set-up Time	40			ns
t_{SDI}	Input Data Set-up Time	120			ns
t_{HDI}	Input Data Hold Time	1			ns
t_{SDO}	Output Data Set-up Time (1 TTL load and C_L = 50pF)			150	ns
t_{DZ}	Output High Impedance Delay Time (1 TTL load and C_L = 50pF)			80	ns

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Notes : 1. Voltage levels shown are $V_{IL} < 0.4V$, $V_{IH} > 2.4V$, unless otherwise specified.
2. Measurements points shown are 0.8V and 2.2V, unless otherwise specified.

Figure 2 : Write Operation

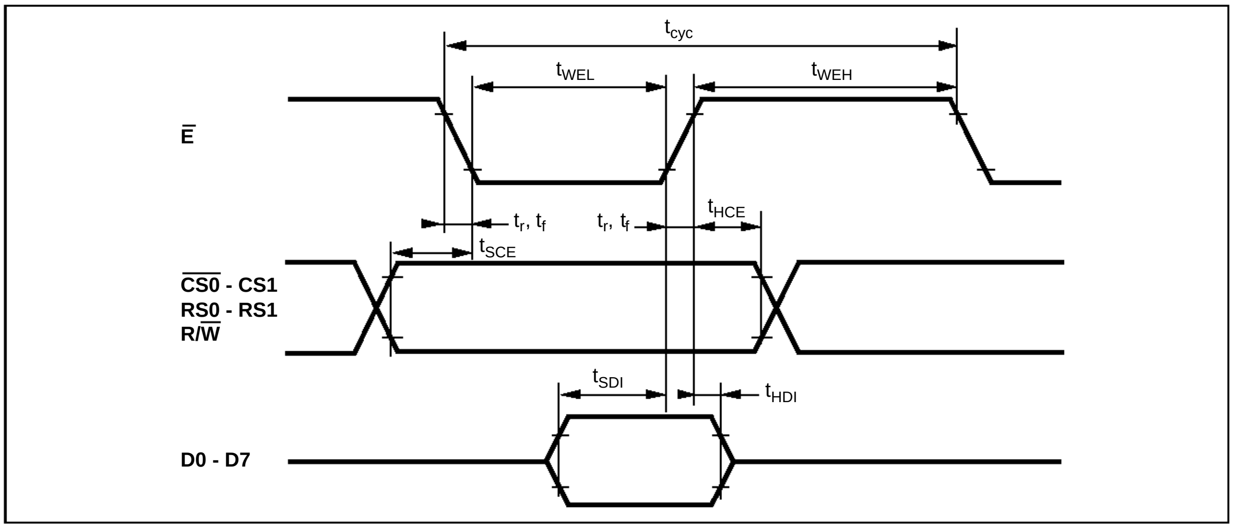
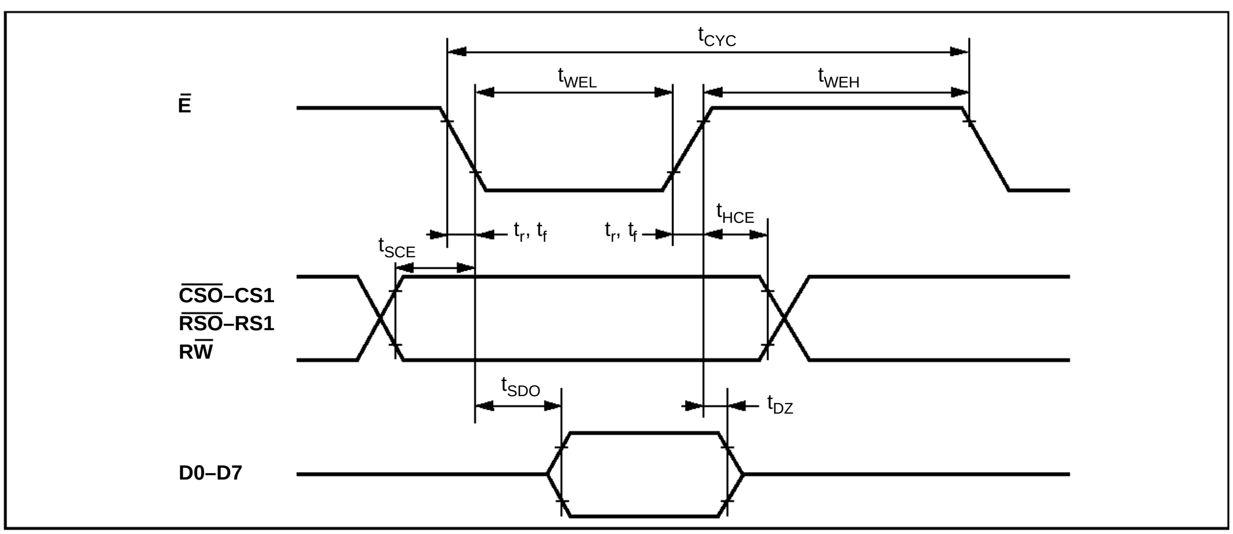


Figure 3 : Read Operation



RECEPTION CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
PERFORMANCE OF THE WHOLE RECEPTION CHAIN (input RAI or LEI, output RR1)					
G	Gain (AGC gain = 0dB, RxCCLK = 9600Hz, V_{IN} = 77mV_{EFF}, f = 2000Hz)	-0.5		-0.5	dB
TD	Total Non Harmonic Distortion (AGC gain = 0dB, RxCCLK = 9600Hz, V_{IN} = 775mV_{EFF}, f = 2000Hz)			-58	dB
PERFORMANCE OF THE RECEPTION SUB-CHAIN (from RAI input to S/H2 input)					
TD	Total Distortion (RxCCLK = 9600 Hz, V_{IN} = 1.6V_{EFF}, f = 2000Hz)			-72	dB

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RECEIVE BAND-PASS FILTER AND REJECTION FILTER (input RAI, output RFO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
LOW-PASS FILTER (f_S = 288kHz)					
G_{REF}	Reference Gain (V_{IN} = 775mV_{EFF}, f = 1800Hz)	-0.5		0.5	dB
G_{REL}	Relative Gain to G_{REF} 0Hz < f < 3000Hz f = 3200Hz f > 6250Hz	 -0.4 -3		 0.3 0.3 -60	dB
T_{gp}	Group Propagation Delay Time (f = 1800Hz)			300	µs
T_{gpd}	Group Propagation Delay Time Distortion (600Hz < f < 3000Hz)			360	µs
HIGH-PASS FILTER (f_S = 72kHz)					
G_{REF}	Reference Gain (V_{IN} = 775mV_{EFF}, f = 1800Hz)	-0.5		0.5	dB
G_{REL}	Relative Gain to G_{REF} 500Hz < f ≤ 3000Hz f = 500Hz f < 100Hz	 -0.4 -3		 0.3 0.5 -25	dB
T_{gp}	Group Propagation Delay Time (f = 1800Hz)			50	µs
T_{gpd}	Group Propagation Delay Time Distortion (600Hz < f < 3000Hz)			450	µs
HIGH-PASS FILTER AND REJECTION FILTER (f_S = 72kHz)					
G_{REF}	Reference Gain (V_{IN} = 775mV_{EFF}, f = 1800Hz)	-1		0	dB
G_{REL}	Relative Gain to G_{REF} f = 100Hz f = 370Hz 390Hz < f < 450Hz f = 470Hz f = 900Hz			 -25 -27 -30 -27 0	dB
T_{gp}	Group Propagation Delay Time (f = 1800Hz)			75	µs
T_{gpd}	Group Propagation Delay Time Distortion (600Hz < f < 3000Hz)			1400	µs

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Note : The measurement frequencies are integer sub-multiples of filters sampling frequencies.

RECONSTRUCTION FILTER

Symbol	Parameter	Min.	Typ.	Max.	Unit
RECONSTRUCTION FILTER (f_S = 288kHz)					
G_{REF}	Reference Gain (V_{IN} = 775mV_{EFF}, f = 2000Hz)	-0.3		0.3	dB
G_{REL}	Relative Gain to G_{REF} 0Hz < f < 2900Hz f = 3100Hz f > 6000Hz	 -0.4 -3 		 0.3 0.3 -60	dB
T_{gp}	Group Propagation Delay Time (f = 1800Hz)			300	µs
T_{gpd}	Group Propagation Delay Time Distortion (600Hz < f < 3000Hz)			440	µs
WHOLE RECEPTION FILTERING CHAIN (input RAI or LEI, output RFO)					
G_{REF}	Reference Gain (V_{IN} = 775mV_{EFF}, f = 2000Hz, RC3 = $AO)	-0.5		0.5	dB
N_{rfo}	Noise on RFO (RAI, LEI, EEI tied to AGND, 250Hz < f < 3200Hz)			350	µV_{EFF}

68951-08.TBL

PERFORMANCE OF RESIDUAL SIGNAL CHANNEL AND A/D CONVERTER (input EEI, output RR2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{in}	Input Voltage (peak to peak)			5	V
R_{esh}	A/D Converter Resolution			12	Bit
LSB	Analog Increment		1.2		mV
E_{il}	Integral Linearity Error	-16		16	LSB
E_{dl}	Differential Linearity Error	-0.7		0.7	LSB
V_{os}	Offset Voltage	-100		100	LSB

68951-09.TBL

AGC AMPLIFIER AND A/D CONVERTER (input AGC1, output RR1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
G_{rel}	Relative Gain to Programmed Gain 0dB ≤ AGC ≤ 24dB 25.5dB ≤ AGC ≤ 46.5dB	 -0.5 -1		 0.5 1	dB
V_{os}	Offset Voltage	-70		70	LSB
N	Equivalent RMS Noise (AGC gain = 0dB, RAI, LEI, EEI tied to AGND)			1.2	mV_{EFF}

68951-10.TBL

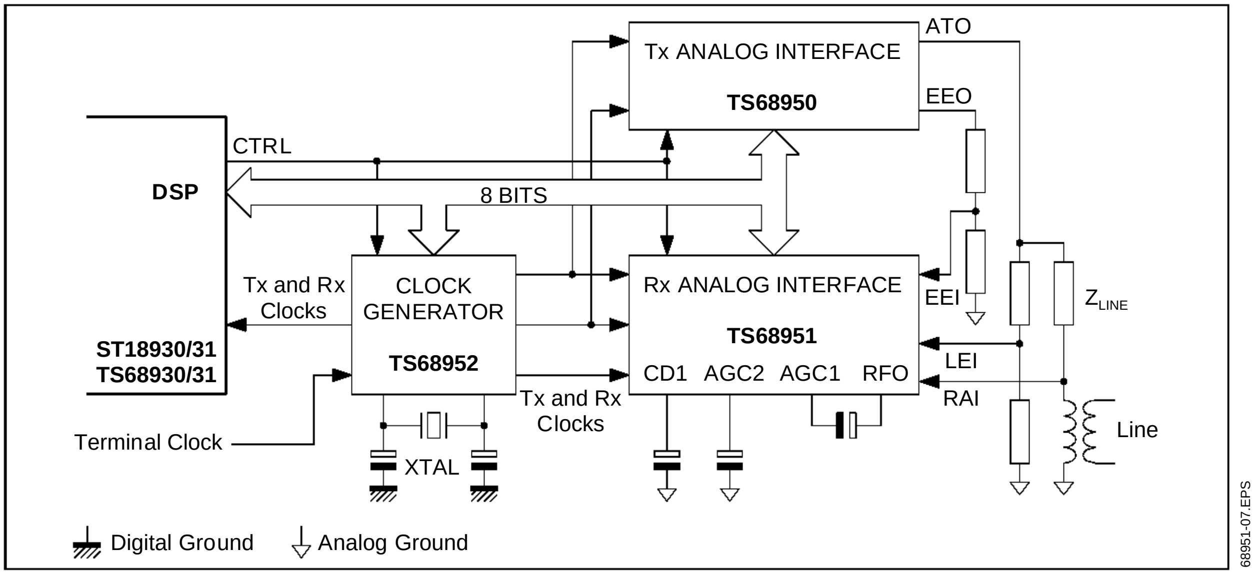
CARRIER LEVEL DETECTOR (input AGC1, output CDR)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{rel}	Relative Threshold to Programmed Threshold	-1		1	dB
H_{yst}	Hysteresis	2		3	dB
V_{os}	Input Offset Voltage 1st Threshold Pair 2nd Threshold pair 3rd Threshold Pair	 -1 -2 -3		 1 2 3	mV
T_{dd}	Detection Delay Time 0mV_{EFF} to 775mV_{EFF} Transition or 775mV_{EFF} to 0V_{EFF} Transition	1		3	ms

68951-11.TBL

APPLICATION INFORMATION

Figure 4 : Modem Analog Front-end Chip Set



Note : In some cases, external-user circuitry may induce power-up sequency latch-up problems that can be efficiently avoided using ST BAT43 Schottky small signal diodes as follow :

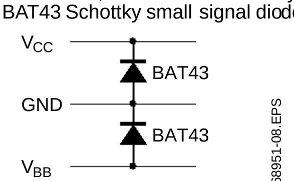


Figure 5 : Four-wire or Two-wire Half Duplex and Two-wire Band-split Analog Signal Treatment

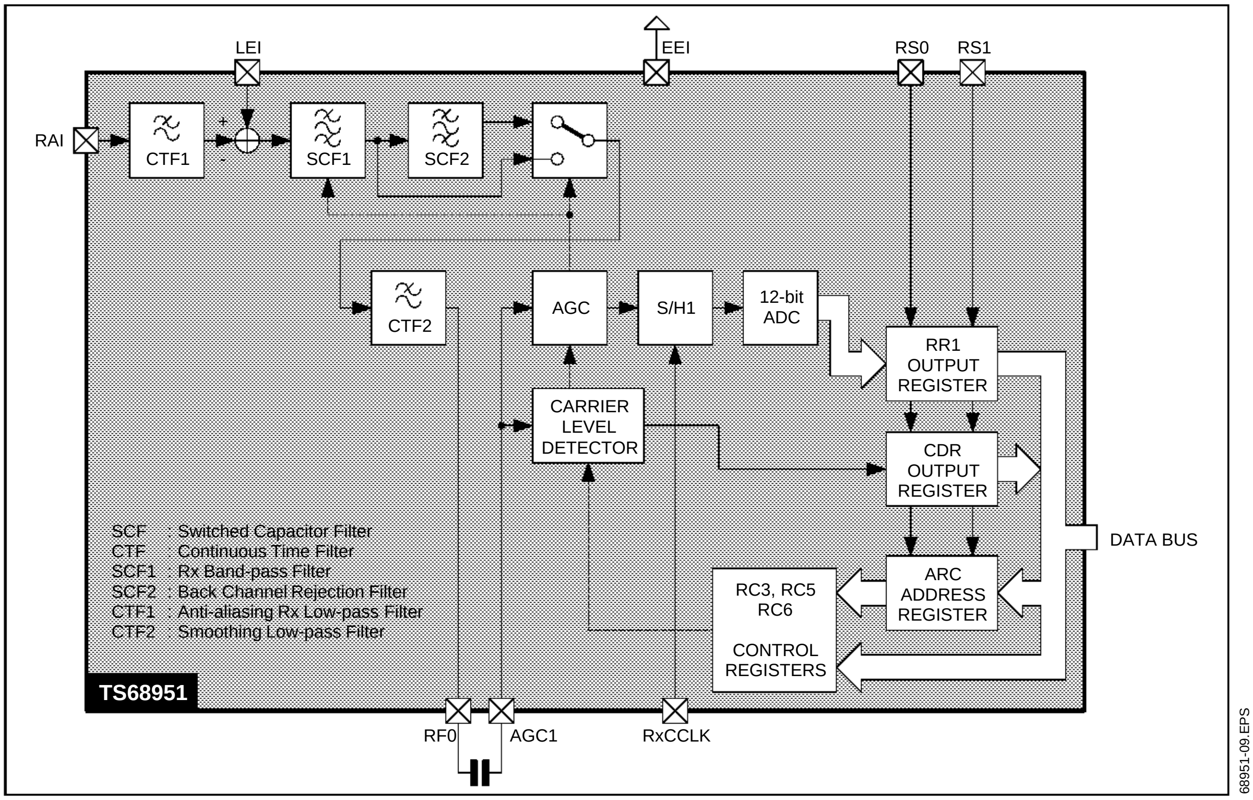
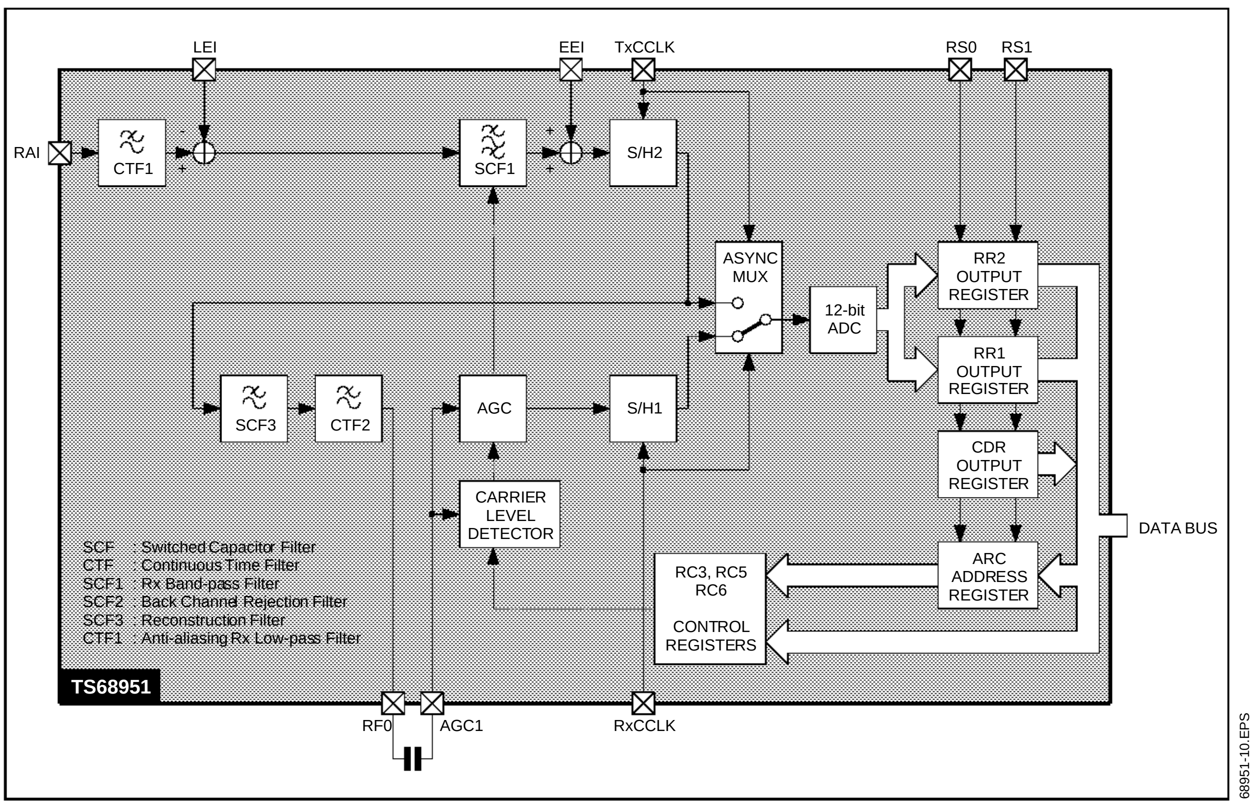
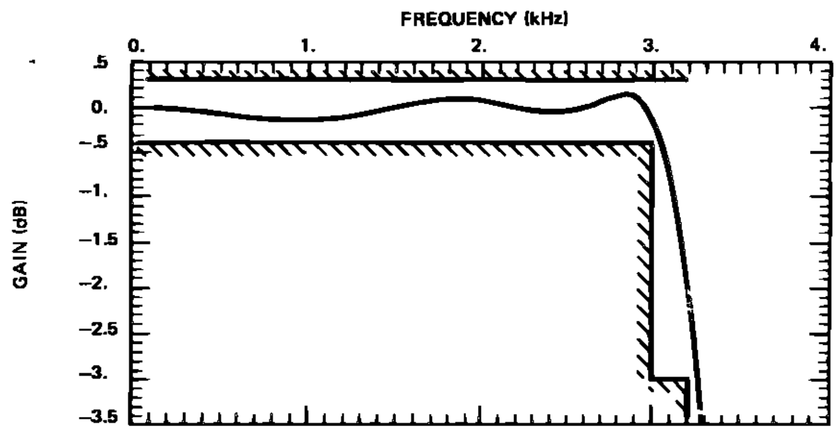


Figure 6 : Two-wire Echo Cancelling Analog Signal Treatment



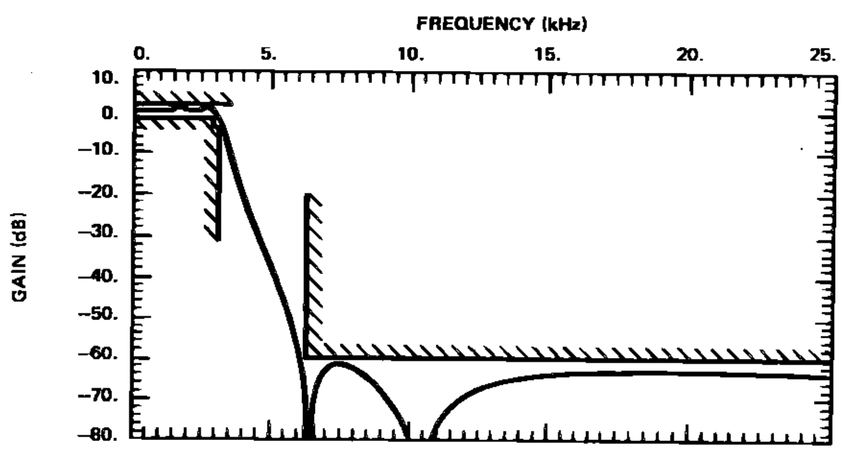
APPENDIX 1

Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (fs = 288kHz)



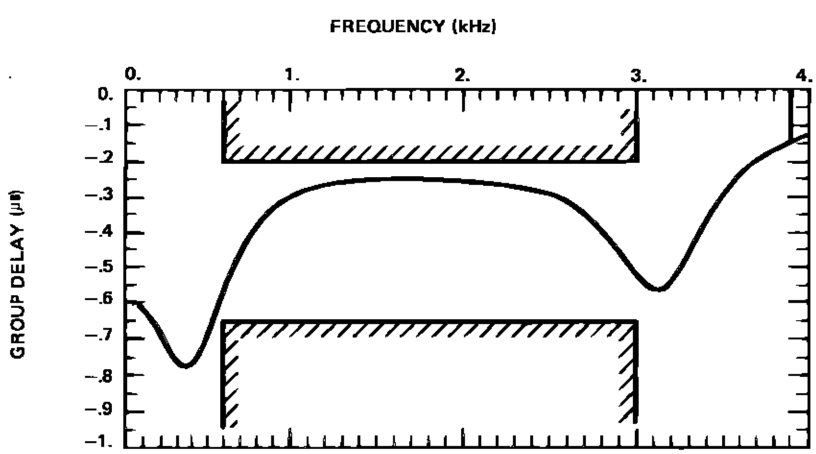
68951-11.EPS

Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (fs = 288kHz)



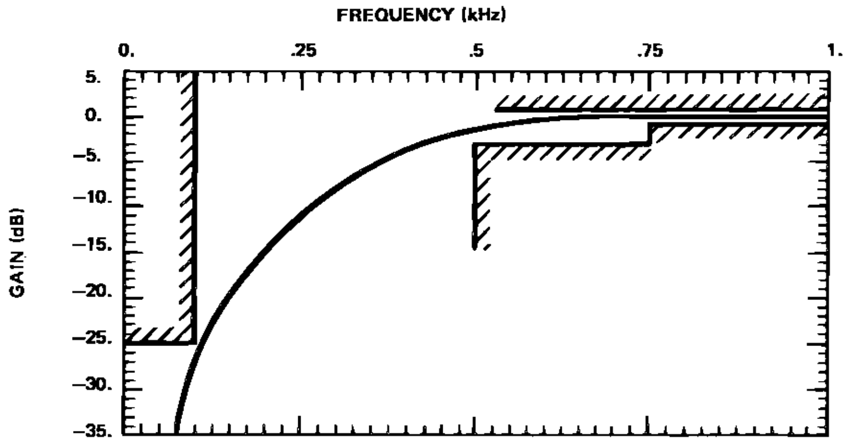
68951-12.EPS

Rx LOW-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (fs = 288kHz)



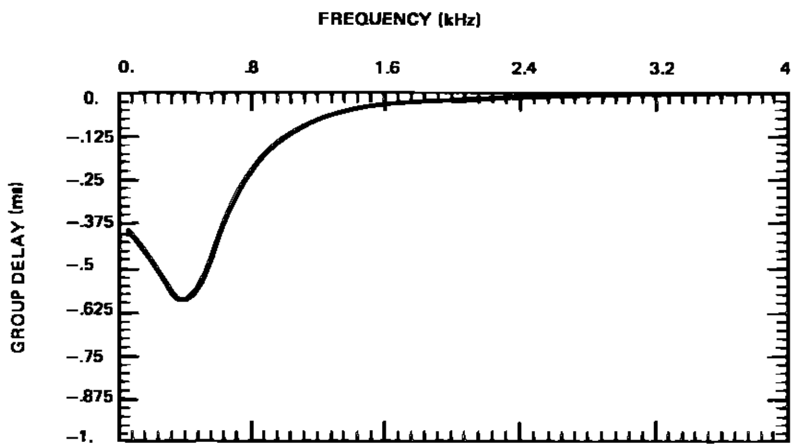
68951-13.EPS

Rx HIGH-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (f_S = 72kHz)



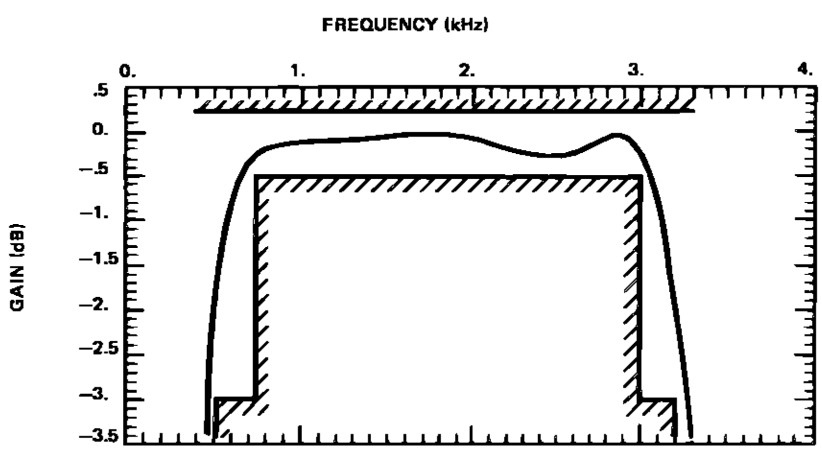
68951-14.EPS

Rx HIGH-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (f_S = 72kHz)



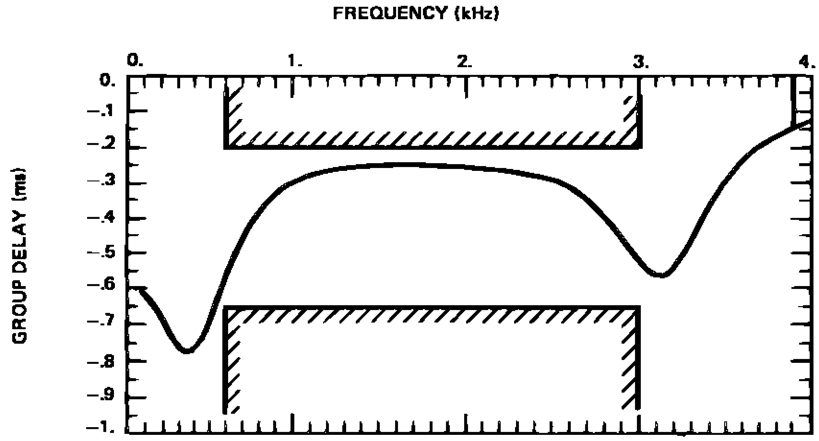
68951-15.EPS

Rx HIGH-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (HP : f_S = 72kHz, LP : f_S = 288kHz)



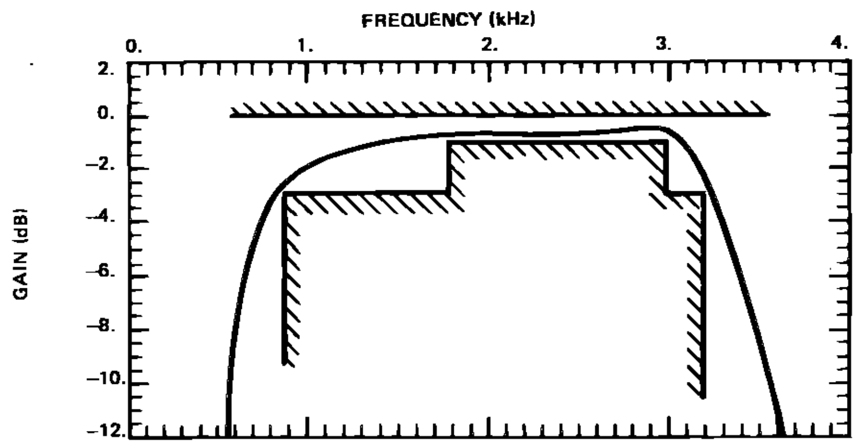
68951-16.EPS

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART
(HP : f_S = 72kHz, LP : f_S = 288kHz)



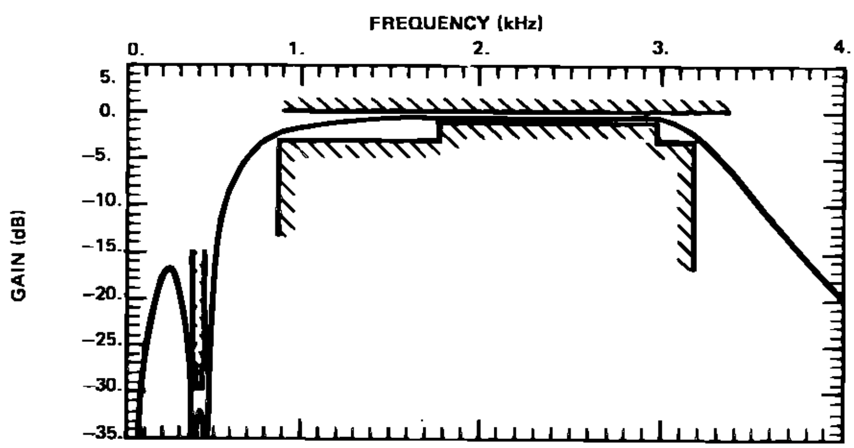
68951-17.EPS

Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP and REJ. : f_S = 72kHz, LP : f_S = 288kHz)



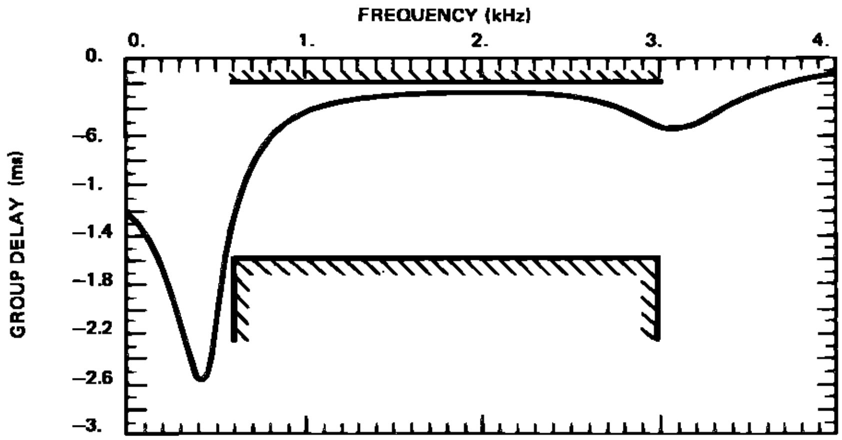
68951-18.EPS

Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP and REJ. : f_S = 72kHz, LP : f_S = 288kHz)



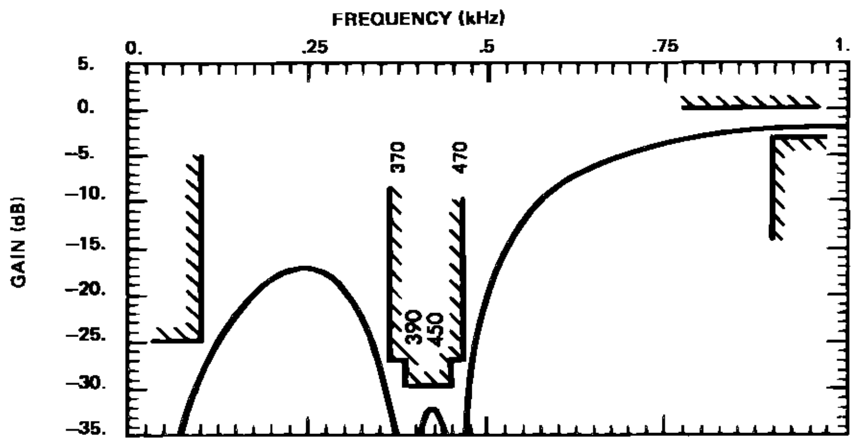
68951-19.EPS

Rx BAND-PASS AND REJECTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART
(HP and REJ. : f_S = 72kHz, LP : f_S = 288kHz)



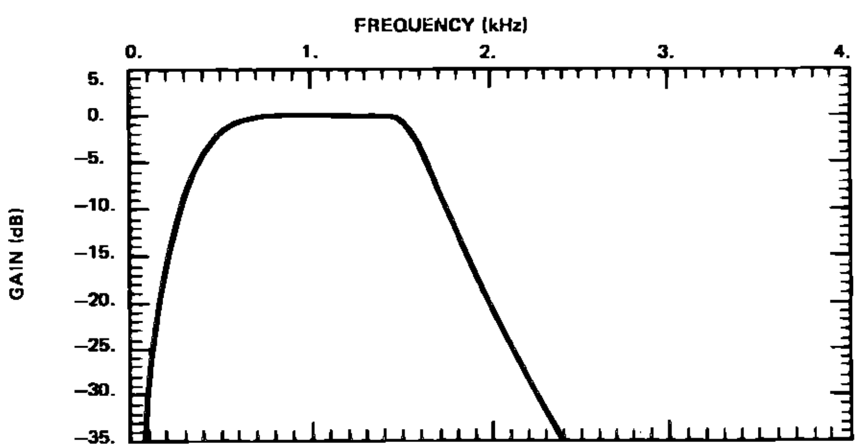
68951-20.EPS

Rx HIGH-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART (f_S = 72kHz)



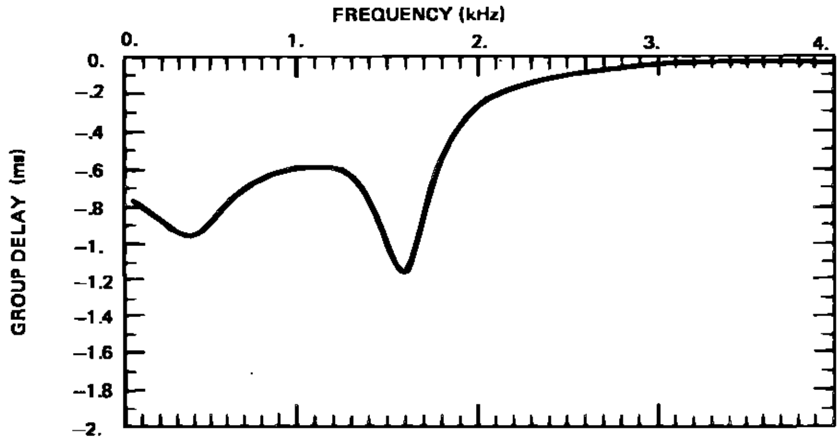
68951-21.EPS

Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V.22 MODE (Low Channel)
(HP : f_S = 72kHz, LP : f_S = 144kHz)



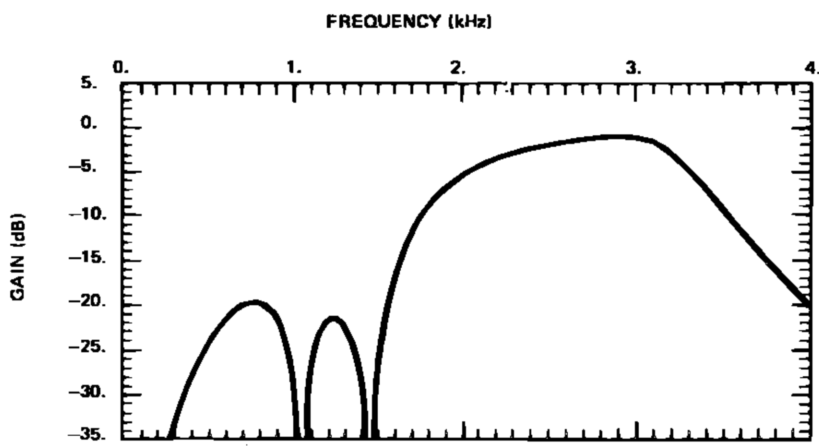
68951-22.EPS

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (Low Channel)
(HP : f_S = 72kHz, LP : f_S = 144kHz)



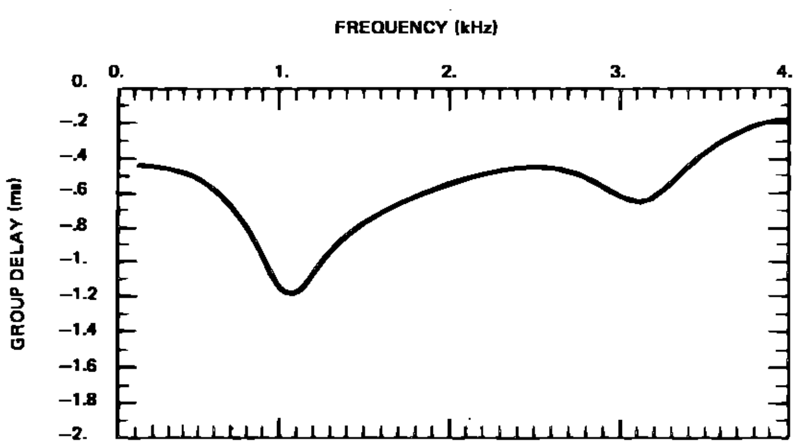
68951-23.EPS

Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V.22 MODE (Low Channel)
(HP and REJ. : f_S = 144kHz, LP : f_S = 288kHz)



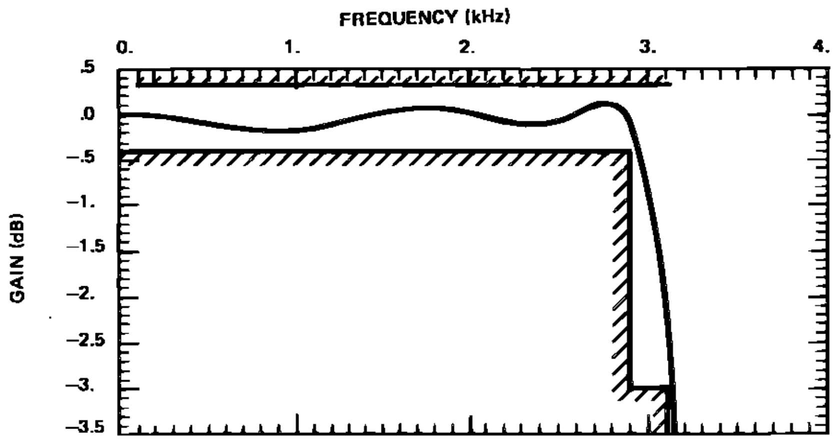
68951-24.EPS

Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (High Channel)
(HP and REJ. : f_S = 144kHz, LP : f_S = 288kHz)



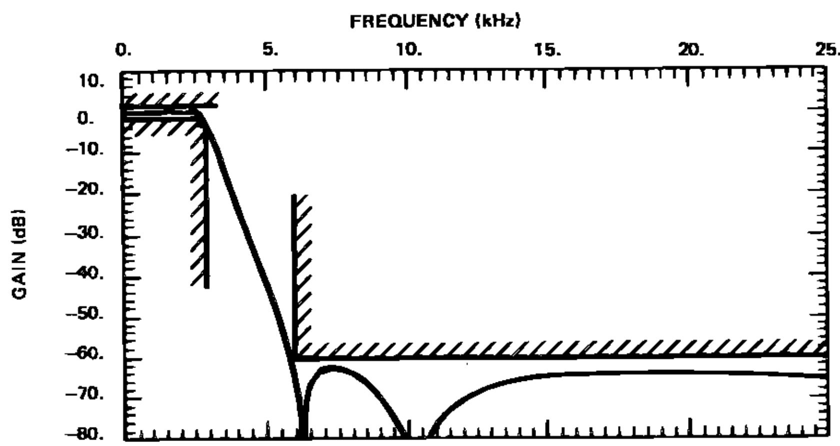
68951-25.EPS

RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHART



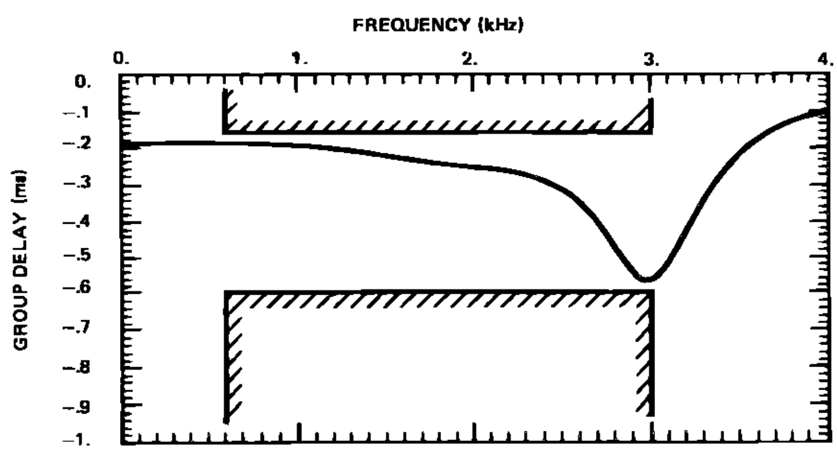
68951-26.EPS

RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHART



68951-27.EPS

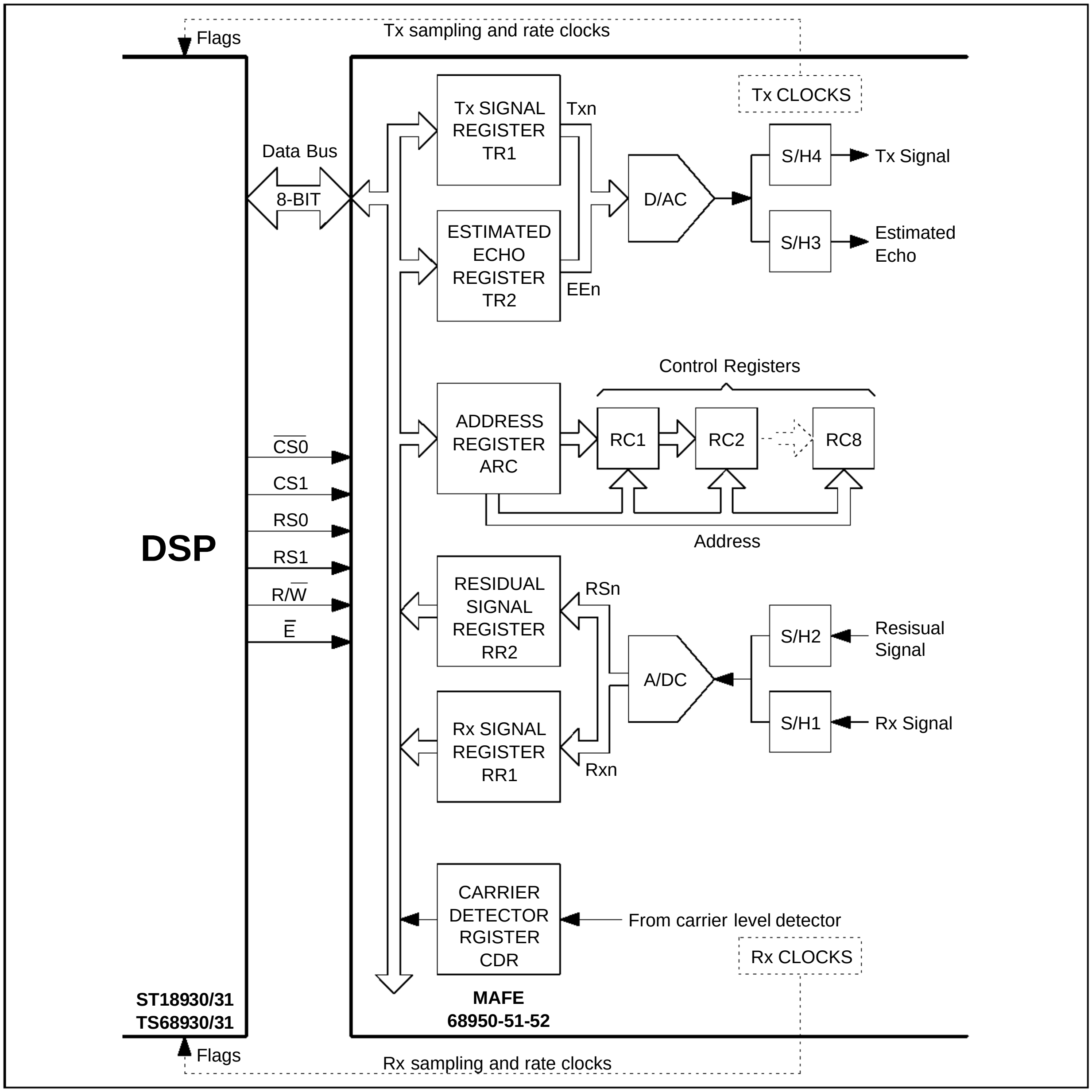
RECONSTRUCTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART



68951-28.EPS

APPENDIX 2

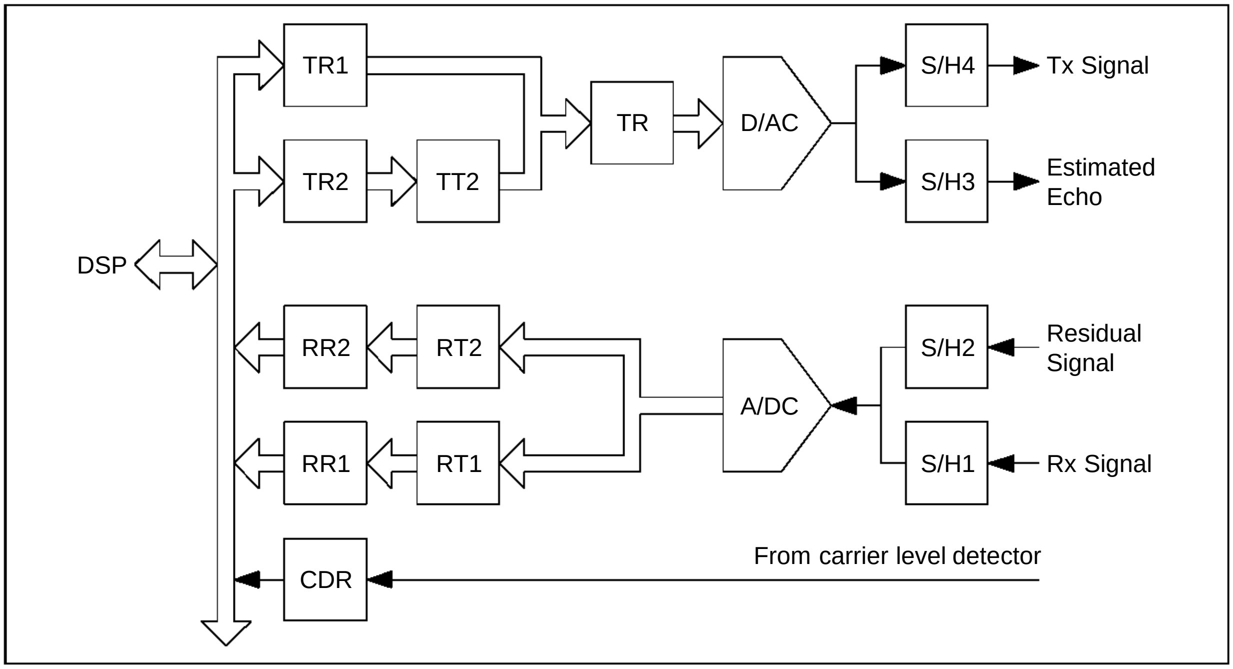
INTERFACE BETWEEN DSP AND MODEM ANALOG FRONT-END (TS68950/51/52)



68951-29.EPS

APPENDIX 3

DETAILED INPUT/OUTPUT REGISTERS DIAGRAM



68950-30.EPS

	R/$\overline{W}$	RS0	RS1	Register Accessed
Writing	0 0 0 0	0 0 1 1	0 1 0 1	TR1 TR2 ARC Control Register Addressed by ARC
Reading	1 1 1 1	0 0 1 1	0 1 0 1	RR1 RR2 CDR Not Used

68951-12.TBL

APPENDIX 4

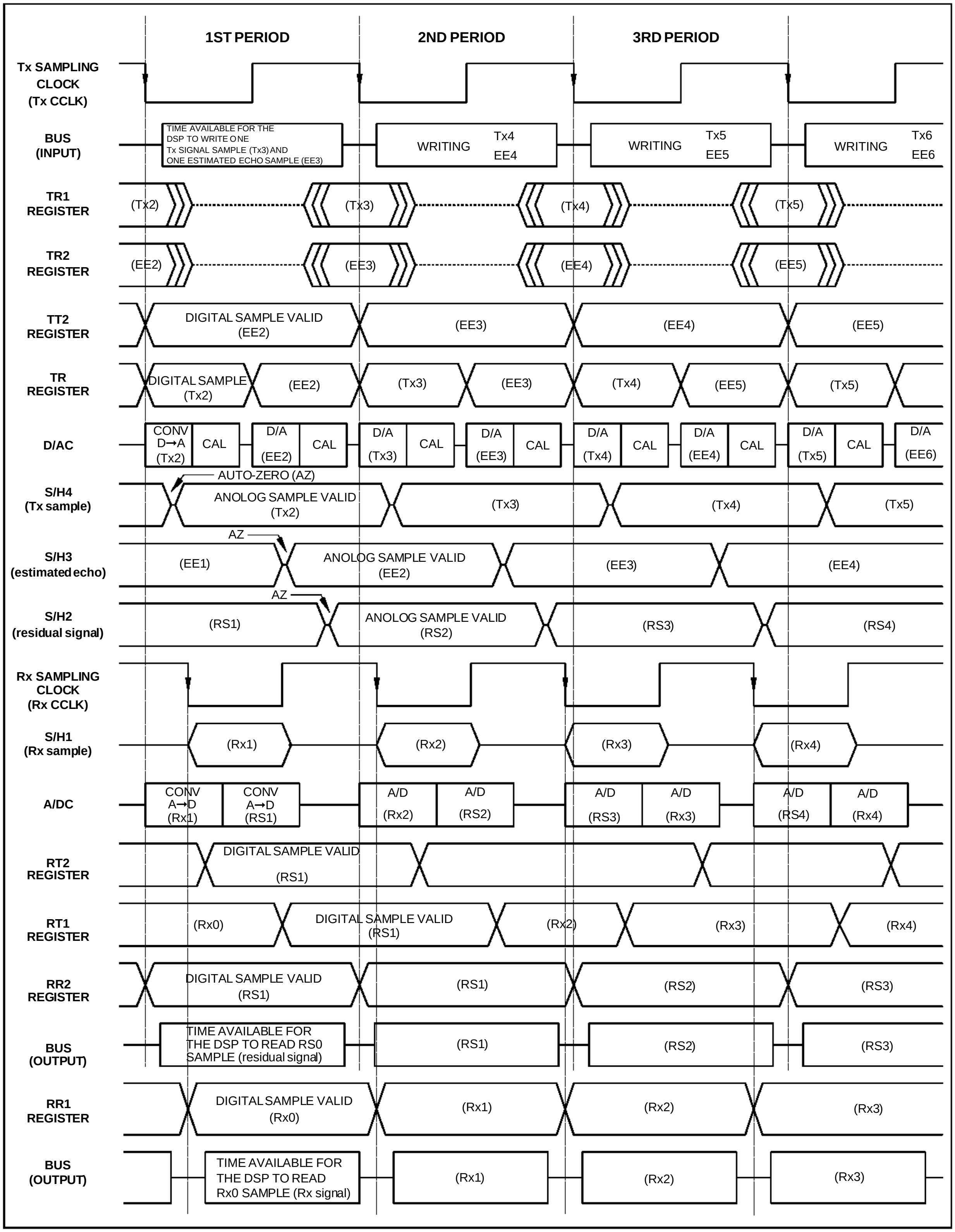
CONTROL REGISTERS PROGRAMMING

Register Name	Circuit Including this Register	Register Content								ARC Content (register address)		
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5
RC1	68952	HB4	HB3	HB2	HB1	HR3	HR2	HR1	-	0	0	1
RC2	68952	HM3	HM2	HM1	HS2	HS1	HTHR	-	-	0	0	1
RC3	68951	HP2	HP1	LP2	LP1	REJ	S/A	REC	-	0	1	0
RC4	68950	ATE4	ATE3	ATE2	ATE1	-	EM2	EM1		0	1	1
RC5	68951	GR5	GR4	GR3	GR2	GR1	-	-		1	0	0
RC6	68951	GDS2	GDS1	HDS	-	-	-	-		1	0	1
RC7	68952	SP5	SP4	SP3	SP2	SP1	-	-		1	1	0
RC8	68952	MPE	SPR	AVRE	VAL	INIT	-	-		1	1	1

68951-13.TBL

APPENDIX 5

PROGRESSION OF THE DIGITAL AND ANALOG SAMPLES IN THE MAFE



68951-31.EPS

APPENDIX 6 : FURTHER REFERENCES

Mafe Characterization Report

This report gives the results of the measurements performed on the TS68950-51-52 Modem Analog Front-End (MAFE) chip set.

Chapter 1 describes the configuration and the method used for these measurements.

Chapter 2 comments the results obtained on the two signal paths of the transmit (Tx) analog front-end TS68950. i.e the echo path and the Tx signal path. Similarly chapter 3 gives the results obtained on the echo path and the receive (Rx) signal path of the Rx analog front-end TS68951.

Performances obtained on the TS68951 when using plesiochronous clocks are given in chapter 4. In this case, the TS68952 clock generator delivers the main clock and the two sampling clocks to the Rx analog interface.

Mafe Evaluation Board

The MAFE evaluation board is a complete unit for evaluation of the TS68950/51/52 MAFE chip set.

The MAFE evaluation board is equipped with the TS68950/51/52 chip set and a phone line interface facilities.

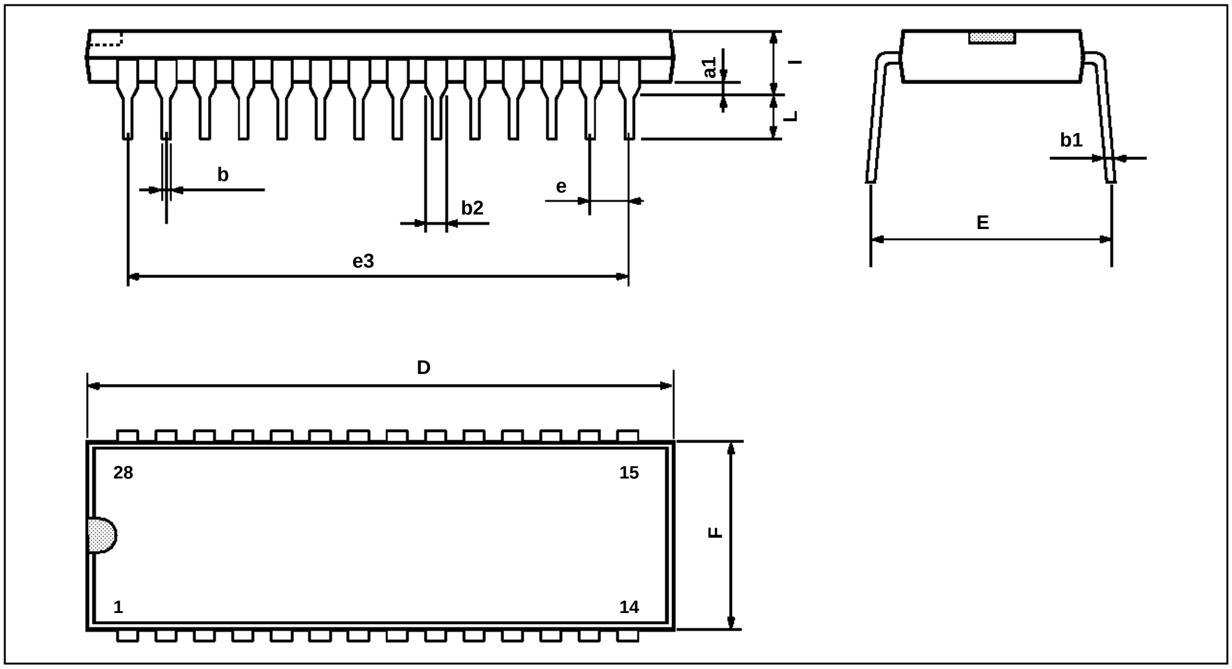
It can be directly connectable to an external Digital Signal Processor through a 50-pins connector or can be linked to the SGS-THOMSON family of digital signal processors emulation-evaluation tools. In this case, along with the software tools (MACROASSEMBLER, SIMULATOR and LINKER), it provides a ready-to-use Digital Signal Processor System Interface well adapted to the analog word and high speed modems development.

Application Note

This application note describes the development of Real-Time Algorithms using the SGS-THOMSON Digital Signal Processor TS68930 and the MAFE chip set.

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



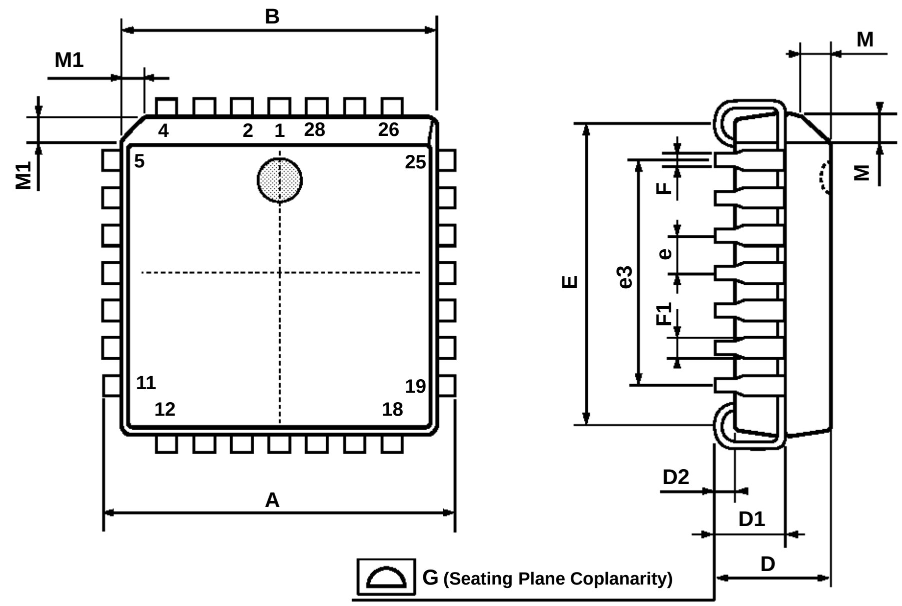
PM-DIP28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP28.TBL

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC CHIP CARRIER



PMPLCC28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

PLCC28.TBL