DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD30200, 30210

VR4300™, VR4305™, VR4310™
64-BIT MICROPROCESSOR

The μPD30200 (VR4300), 30200-133 (VR4305), and 30210 (VR4310)Note are high-performance, 64-bit RISC (Reduced Instruction Set Computer) type microprocessors employing the RISC architecture developed by MIPS.

The VR4300, VR4305, and VR4310 are intended for the high-performance embedded device field and have 32-bit system buses.

Note Under development

Detailed functions are descrided in the following manual. Be sure to read the manual when designing your system.

- **VR4300, VR4305, VR4310 User's Manual (U10504E)**

FEATURES

- Employs 64-bit RISC MIPS architecture
- High-speed operation processing
  - 5-stage pipeline processing
  - High-speed execution of integer and floating-point operations
  - ★ 48 SPECint92, 36 SPECfp92, 106MIPS, at 80 MHz (μPD30200-80)
    60 SPECint92, 45 SPECfp92, 131MIPS, at 100 MHz (μPD30200-100)
    ★ 60 SPECint92, 45 SPECfp92, 133MIPS, at 100 MHz (μPD30210-100)
    80 SPECint92, 60 SPECfp92, 173MIPS at 133 MHz (μPD30200-133)
    ★ 80 SPECint92, 60 SPECfp92, 176MIPS at 133 MHz (μPD30210-133)
    ★ 100 SPECint92, 75 SPECfp92, 221MIPS at 167 MHz (μPD30210-167)
- Instruction set compatible with VR4000™ series (conforms to MIPS-I/II/III)
- Cache memory (instruction: 16K bytes, data: 8K bytes)
- 32-bit address/data miltiplexed bus facilitating system design
- Low power consumption
  - ★ μPD30200-80 : 1.5 W (TYP.) (at 80 MHz)
  - μPD30200-100, 30200-133: 1.8 W (TYP.) (at 100 MHz), 2.4 W (TYP.) (at 133 MHz)
  - ★ μPD30210-xxx: 1.4 W (TYP.) (at 100 MHz, target value), 1.9 W (TYP.) (at 133 MHz, target value)
    2.4 W (TYP.) (at 167 MHz, target value)
- ★ Supply voltage: 3.3 ± 0.3 V (μPD30200-80, 30200-100), 3.0 to 3.5 V (μPD30200-133, 30210-xxx)

Unless otherwise specified, the VR4300 (μPD30200) is treated as the representative model throughout this document.

The information in this document is subject to change without notice.

Document No. U10116EJ4V0DS00 (4th edition)
Date Published April 1998 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

- Embedded controller
- Page printer controller
- Amusement game machines, etc.

ORDERING INFORMATION

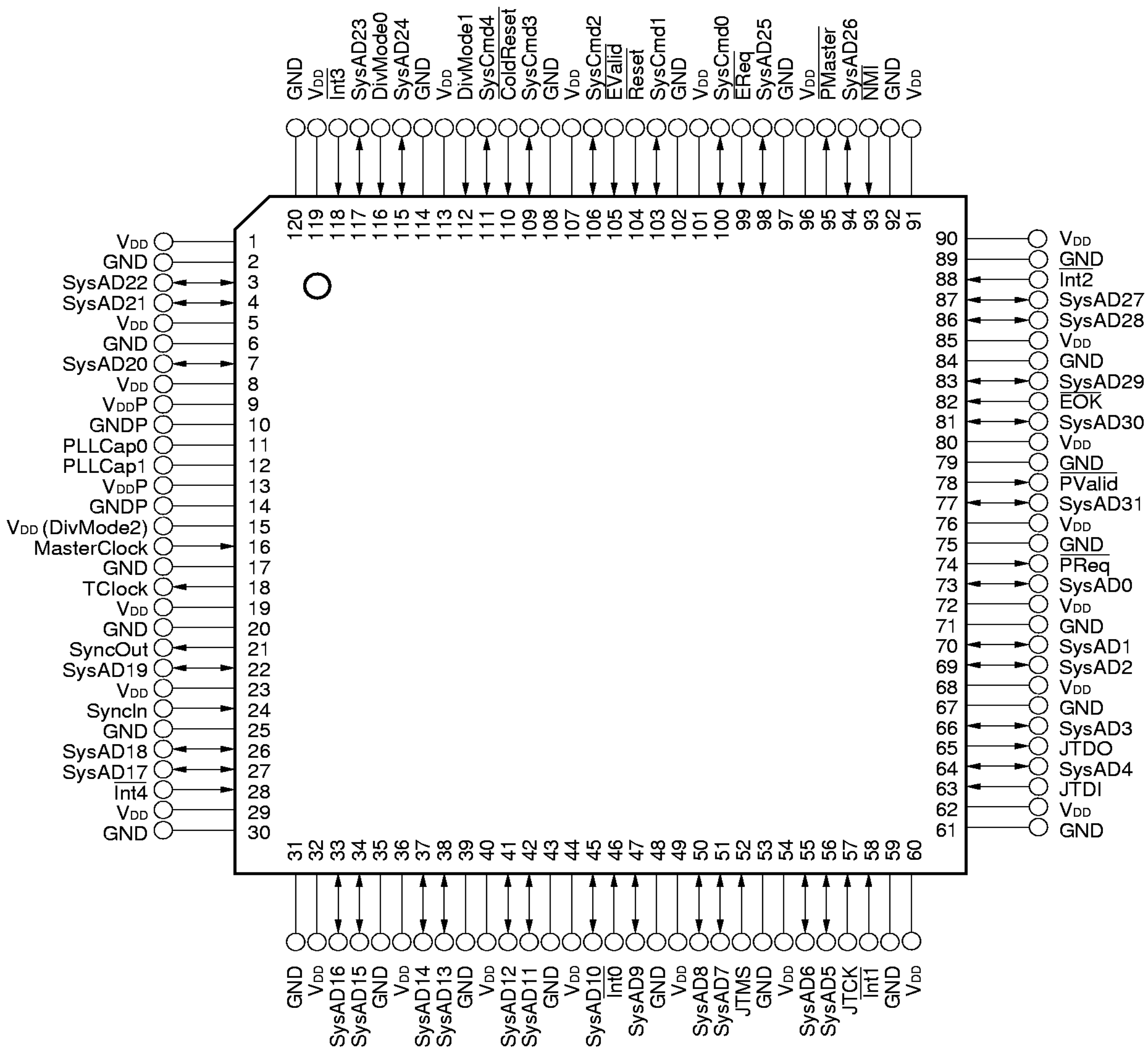
	Part Number	Package	Maximum Internal Operating Frequency (MHz)
★	μPD30200GD-80-LBB	120-pin plastic QFP (28 × 28 mm)	80
	μPD30200GD-100-MBB	120-pin plastic QFP (28 × 28 mm)	100
	μPD30200GD-133-MBB	120-pin plastic QFP (28 × 28 mm)	133
★	μPD30210GD-100-MBB[Note]	120-pin plastic QFP (28 × 28 mm)	100
★	μPD30210GD-133-MBB[Note]	120-pin plastic QFP (28 × 28 mm)	133
★	μPD30210GD-167-MBB[Note]	120-pin plastic QFP (28 × 28 mm)	167

Note Under development

PIN CONFIGURATION (Top View)

- 120-pin plastic QFP (28 × 28 mm)
  μPD30200GD-80-LBB
  μPD30200GD-100-MBB
  μPD30200GD-133-MBB
  μPD30210GD-100-MBB
  μPD30210GD-133-MBB
  μPD30210GD-167-MBB

★



Remark ( ): Pin name in the μPD30210-xxx

PIN NAMES

$\overline{\text{ColdReset}}$	:	Cold Reset
DivMode (1:0)[Note]	:	Divide Mode
$\overline{\text{EOK}}$	:	External OK
$\overline{\text{EReq}}$	:	External Request
$\overline{\text{EValid}}$	:	External Valid
$\overline{\text{Int(4:0)}}$	:	Interrupt Request
JTCK	:	JTAG Clock Input
JTDI	:	JTAG Data In
JTDO	:	JTAG Data Out
JTMS	:	JTAG Command Signal
MasterClock	:	Master Clock
$\overline{\text{NMI}}$	:	Non-maskable Interrupt Request
PLLCap (1:0)	:	Phase Locked Loop Capacitance
$\overline{\text{PMaster}}$	:	Processor Master
$\overline{\text{PReq}}$	:	Processor Request
$\overline{\text{PValid}}$	:	Processor Valid
$\overline{\text{Reset}}$	:	Reset
SyncIn	:	Synchronization Clock Input
SyncOut	:	Synchronization Clock Output
SysAD(31:0)	:	System Address/Data Bus
SysCmd (4:0)	:	System Command/Data ID Bus
TClock	:	Transmit Clock
V_{DD}	:	Power Supply
GND	:	Ground
V_{DD}P	:	V_{DD} for PLL
GNDP	:	GND for PLL

Note In the μPD30200-xxx. DivMode (2:0) in the μPD30210-xxx.

INTERNAL BLOCK DIAGRAM

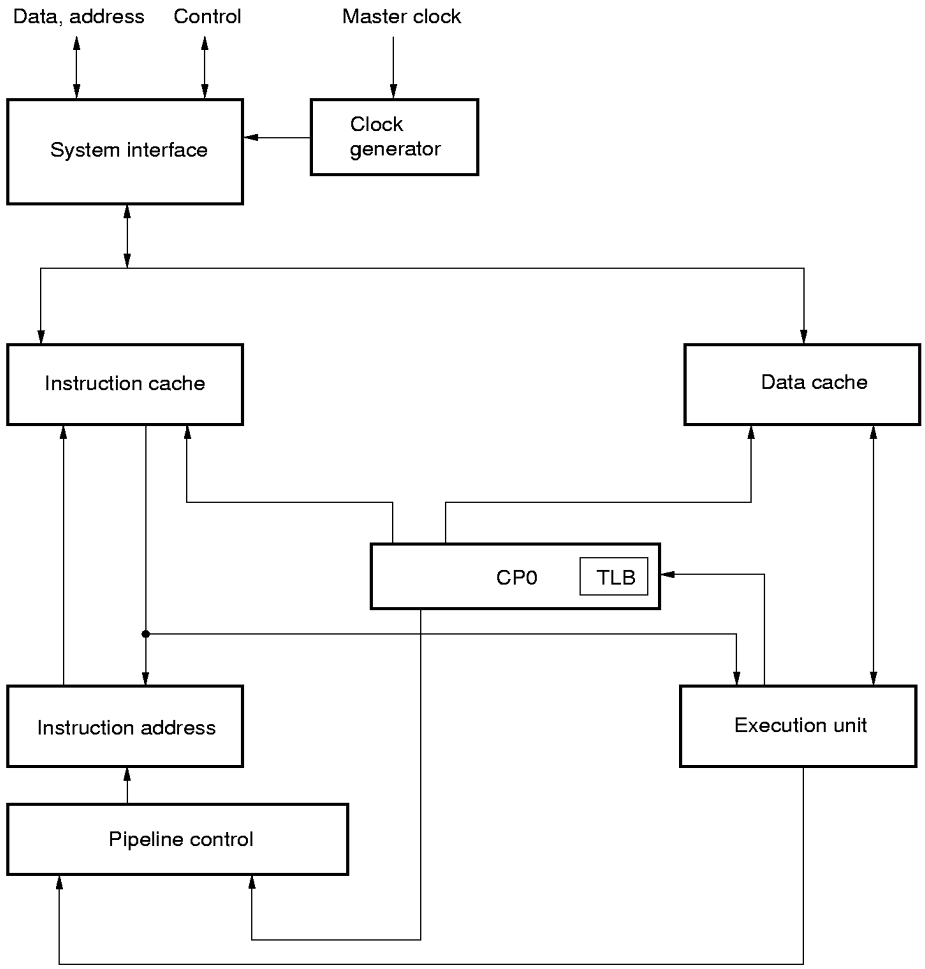


TABLE OF CONTENTS

1. PIN FUNCTIONS

Pin Name	I/O	Function
SysAD (31:0)	I/O	System address/data bus. 32-bit bus for communication between processor and external agent.
SysCmd (4:0)	I/O	System command/data ID bus. 5-bit bus for communication of commands and data identifiers between processor and external agent.
$\overline{\text{EValid}}$	Input	External valid. Signal indicating that external agent has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{PValid}}$	Output	Processor valid. Signal indicating that processor has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{EReq}}$	Input	External request. Signal used by external agent to request for its use by system interface.
$\overline{\text{PReq}}$	Output	Processor request. Signal used by processor to request for its use by system interface. If the processor detects a protocol error, this signal oscillates with the same frequency as SClock (internal), and the system interface hangs up.
$\overline{\text{PMaster}}$	Output	Processor master. Signal indicating that processor controls system interface.
$\overline{\text{EOK}}$	Input	External OK. Signal indicating that external agent can accept processor request.
$\overline{\text{Int (4:0)}}$	Input	Interrupt. General-purpose processor interrupt requests whose input statuses can be confirmed by bits 14 through 10 of cause register.
$\overline{\text{NMI}}$	Input	Non-maskable interrupt. Interrupt request that cannot be masked.
$\overline{\text{ColdReset}}$	Input	Cold reset. Signal that initializes internal status of processor. It can be made active/inactive without synchronizing with the MasterClock.
$\overline{\text{Reset}}$	Input	Reset. Signal that generates reset exception without initializing internal status of processor.
MasterClock	Input	Master clock. Clock input signal to processor.
TClock	Output	Transmit-receive signal clock This is the basic clock for the system interface and is synchronized with the MasterClock.
SyncOut	Output	Synchronization clock output. Output of synchronization clock.
SyncIn	Input	Synchronization clock input. Input of synchronization clock.
JTDI	Input	JTAG data input. Input of JTAG serial data.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>JTDO</td><td>Output</td><td>JTAG data output.
Output of JTAG serial data.</td></tr>
<tr><td>JTMS</td><td>Input</td><td>JTAG command.
Indicates that input serial data is command data.</td></tr>
<tr><td>JTCK</td><td>Input</td><td>JTAG clock input.
Input of JTAG serial clock. If the JTAG interface is not used, set it to low level.</td></tr>
<tr><td>★ DivMode</td><td>Input</td><td>Mode setting.
Sets frequency ratio of MasterClock, TClock, and PClock.
• DivMode (1:0) (V$_{R}$4300)
Example
<table>
<tr><th>DivMode (1:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th><th></th></tr>
<tr><td>00</td><td>33.3 MHz</td><td>133 MHz</td><td>33.3 MHz</td><td>1:4:1</td><td>Note 1</td></tr>
<tr><td>01</td><td>66.7 MHz</td><td>100.0 MHz</td><td>66.7 MHz</td><td>2:3:2</td><td>Note 2</td></tr>
<tr><td>10</td><td>50.0 MHz</td><td>100.0 MHz</td><td>50.0 MHz</td><td>1:2:1</td><td></td></tr>
<tr><td>11</td><td>33.3 MHz</td><td>100.0 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
</table>
Notes 1. This setting is allowed with the 133 MHz model only. With the 100 MHz model, this setting is reserved.
2. This setting is allowed with the 100 MHz model only. With the 133 MHz model, this setting is reserved.

• DivMode (1:0) (V$_{R}$4305)
Example
<table>
<tr><th>DivMode (1:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th></tr>
<tr><td>00</td><td>66.7 MHz</td><td>66.7 MHz</td><td>66.7 MHz</td><td>1:1:1</td></tr>
<tr><td>01</td><td>–</td><td>–</td><td>–</td><td>Reserved</td></tr>
<tr><td>10</td><td>40 MHz</td><td>80 MHz</td><td>40 MHz</td><td>1:2:1</td></tr>
<tr><td>11</td><td>20 MHz</td><td>60 MHz</td><td>20 MHz</td><td>1:3:1</td></tr>
</table>
• DivMode (2:0) (V$_{R}$4310)
Example
<table>
<tr><th>DivMode (2:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th><th></th></tr>
<tr><td>000</td><td>33.3 MHz</td><td>167 MHz</td><td>33.3 MHz</td><td>1:5:1</td><td>Note 1</td></tr>
<tr><td>001</td><td>27.8 MHz</td><td>167 MHz</td><td>27.8 MHz</td><td>1:6:1</td><td>Note 1</td></tr>
<tr><td>010</td><td>66.7 MHz</td><td>167 MHz</td><td>66.7 MHz</td><td>2:5:2</td><td>Note 2</td></tr>
<tr><td>011</td><td>33.3 MHz</td><td>100 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
<tr><td>100</td><td>33.3 MHz</td><td>133 MHz</td><td>33.3 MHz</td><td>1:4:1</td><td></td></tr>
<tr><td>101</td><td>66.7 MHz</td><td>100 MHz</td><td>66.7 MHz</td><td>2:3:2</td><td></td></tr>
<tr><td>110</td><td>50.0 MHz</td><td>100 MHz</td><td>50.0 MHz</td><td>1:2:1</td><td></td></tr>
<tr><td>111</td><td>33.3 MHz</td><td>100 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
</table>
Notes 1. This setting is allowed with the 133 MHz and 167 MHz models only. With the 100 MHz model, this setting is reserved.
2. This setting is allowed with the 167 MHz model only. With the 100 MHz and 133 MHz models, this setting is reserved.

After power application, do not change the value of these pins. Otherwise, the operation is not guaranteed.</td></tr>
<tr><td>PLLCap (1:0)</td><td>–</td><td>PLL capacitor.
Connect capacitor to adjust internal PLL.</td></tr>
<tr><td>V_{DD}P</td><td>–</td><td>PLL V_{DD}.
Power supply for internal PLL.</td></tr>
<tr><td>GNDP</td><td>–</td><td>PLL GND.
Ground for internal PLL.</td></tr>
<tr><td>V_{DD}</td><td>–</td><td>Positive power supply pin.</td></tr>
<tr><td>GND</td><td>–</td><td>Ground pin.</td></tr>
</table>

2. INTERNAL BLOCK

(1) Execution unit

Executes integer operation instructions and floating-point operation instructions.
This unit is provided with the following:

- 64-bit register file
- 64-bit integer/mantissa data bus
- 12-bit exponent data bus

(2) Coprocessor 0 (CP0)

This coprocessor is provided with the following:

- Exception processing unit
- Memory management unit
  The memory management unit converts virtual addresses into physical addresses and checks memory access between different memory segments (kernel, supervisor, and user).

TLB (translation lookaside buffer) converts virtual addresses into physical addresses.
The VR4300 supports seven types of page size, in a range of 4K bytes to 16M bytes in 4 × increments, with VSIZE (virtual address) = 40 and PSIZE (physical address) = 32. TLB has 32 entries. Each entry is mapped to an even/odd page of a page frame number.
The exception processing unit is provided with system control coprocessor registers.

(3) Pipeline control

The pipeline is controlled and appropriate processing is executed in the following cases:

- Occurrence of cache miss
- Flash buffer full
- Multi-cycle instruction
- Occurrence of system exception, etc.

(4) Instruction address

The execution address of the next instruction to be fetched is calculated.
For this purpose, the following units are provided:

- PC incrementer
- Branch address adder
- Conditional branch address selector

(5) Instruction cache

The instruction cache employs the following methods:

- Direct map
- Virtual index address
- Physical tag cache

No hardware is provided to check generation of cache alias due to virtual address.
Each cache line consists of 8-word data, 20-bit tag, and 1-line valid bit.
The cache data interface is 64 bits wide.
Cache parity is not supported.

(6) Data cache

The following methods are employed:

- Direct map
- Virtual index address
- Physical tag, write back cache

Each cache line consists of 4-word data, 20-bit tag, 1-line dirty bit, and 1-line valid bit.
Data is read from the cache in 1 cycle, and is written to the data cache in 2 cycles.
Cache parity is not supported.

(7) System interface

This interface enables the processor to access external resources to satisfy internal requests.
The system interface consists of a 32-bit multiplexed address/data bus, clock signal, interrupt, and control signal.

(8) Clock generator

Generates PClock based on an input clock (MasterClock).
The frequency ratio of PClock to MasterClock can be set by using the DivMode(1:0)[Note] signals on power application.
The frequency of TClock, the reference clock for the external agent, is the same as that of MasterClock.
The clock generator also supports the low power mode, whose operation frequency is a quarter of the normal one. This mode is set with the status register RP bit during operation. The PClock and system interface clock (SClock) frequencies are dynamically switched by this means.
To suppress skewing of the input clock and internal clock, a phased lock loop (PLL) is used.

★ **Note** In the VR4300 and VR4305. DivMode(2:0) in the VR4310.

3. INTERNAL ARCHITECTURE

3.1 Pipeline

Each instruction is executed in the following five steps:

(1) IC instruction fetch
(2) RF decode, register fetch, jump/branch
(3) EX execution
(4) DC data cache read
(5) WB write to register file and data cache

The VR4300 is provided with a 5-stage pipeline. Although it takes five clocks to execute each instruction, paralleling is implemented at instruction level.

★ • VR4300

PClock, which is the pipeline clock, operates at a frequency 1.5[Note 1], 2, 3, or 4[Note 2] times higher than that of the master clock, and the multiple is specified by the DivMode (1:0) pins on power application.

Notes 1. The 1.5 times frequency setting is allowed with the 100 MHz model only. (With the 133 MHz model, this setting is reserved.)

2. The 4 times frequency setting is allowed with the 133 MHz model only. (With the 100 MHz model, this setting is reserved.)

★ • VR4305

PClock, which is the pipeline clock, operates at a frequency 1, 2, or 3 times higher than that of the master clock, and the multiple is specified by the DivMode (1:0) pins on power application.

★ • VR4310

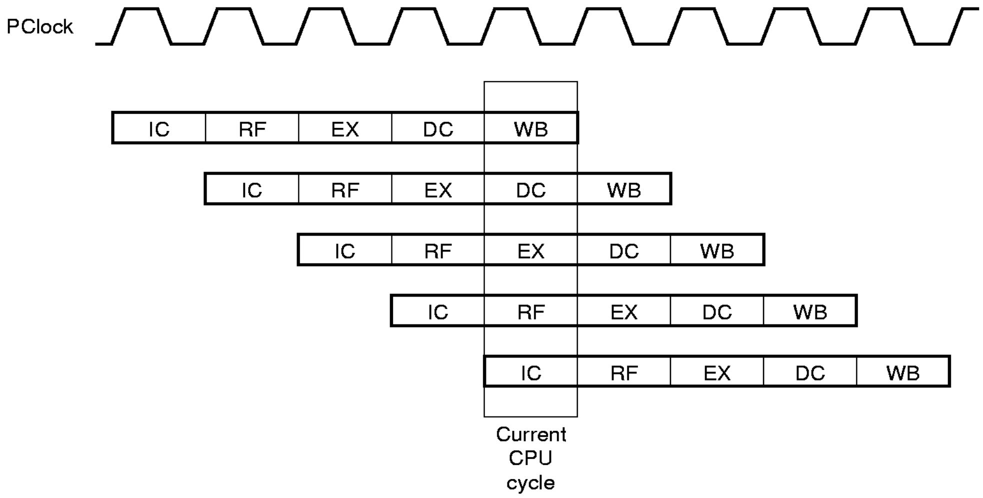
PClock, which is the pipeline clock, operates at a frequency 1.5, 2, 2.5[Note 1], 3, 4, 5[Note 2], or 6[Note 2] times higher than that of the master clock, and the multiple is specified by the DivMode (2:0) pins on power application.

Notes 1. The 2.5 times frequency setting is allowed with the 167 MHz model only. (With the 100 MHz and 133 MHz models, this setting is reserved.)

2. The 5 or 6 times frequency setting is allowed with the 133 MHz and 167 MHz models only. (With the 100 MHz model, this setting is reserved.)

The outline of the pipeline is described below.

Figure 3-1. Pipeline of VR4300 (5 stages)



3.2 CPU Register

The VR4300's CPU registers are shown in Figure 3-2. The bit widths of these registers are determined by the operation mode of the processor (32 bits in 32-bit mode; 64 bits in 64-bit mode).

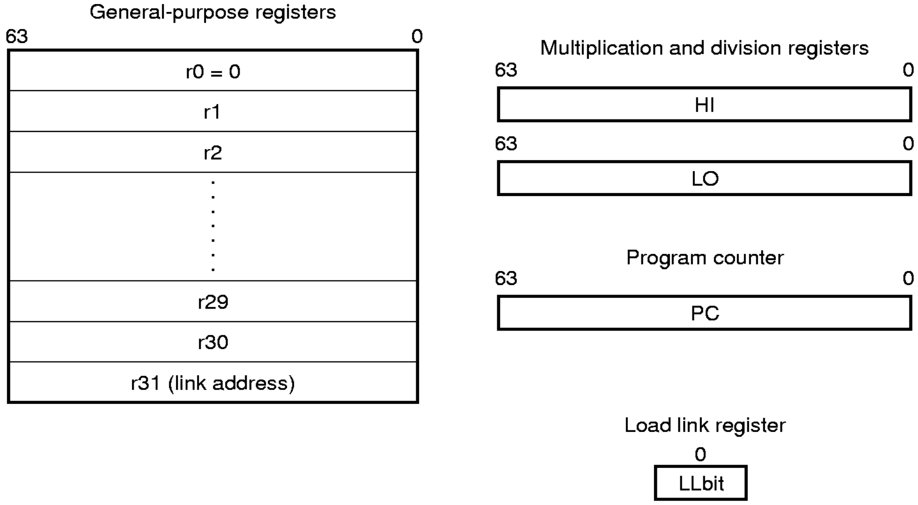
Among the 32 general-purpose registers, the following two registers have special meanings.

- Register r0: The content is always 0. Register r0 can be coded as the instruction's target register to discard the operation result. When the value 0 is required, this register can be used as the source register.
- Register r31: Refers to the link register for the JAL and JALR instructions. Therefore, be sure not to use register r31 for other instructions.

Two multiplication and division registers (HI, LO) store integer multiplication results as well as the quotients (LO) and remainders (HI) from integer division.

The load link register is for synchronizing the processors on a multiprocessor system. However, this has no meaning for the VR4300, which does not support multiprocessor systems. The register is defined here for the purpose of maintaining compatibility with other VR series processors.

Figure 3-2. CPU Register



A program status word (PSW) is not provided. However, its functions are provided by the status register and the cause register incorporated in the system control processor (CP0).

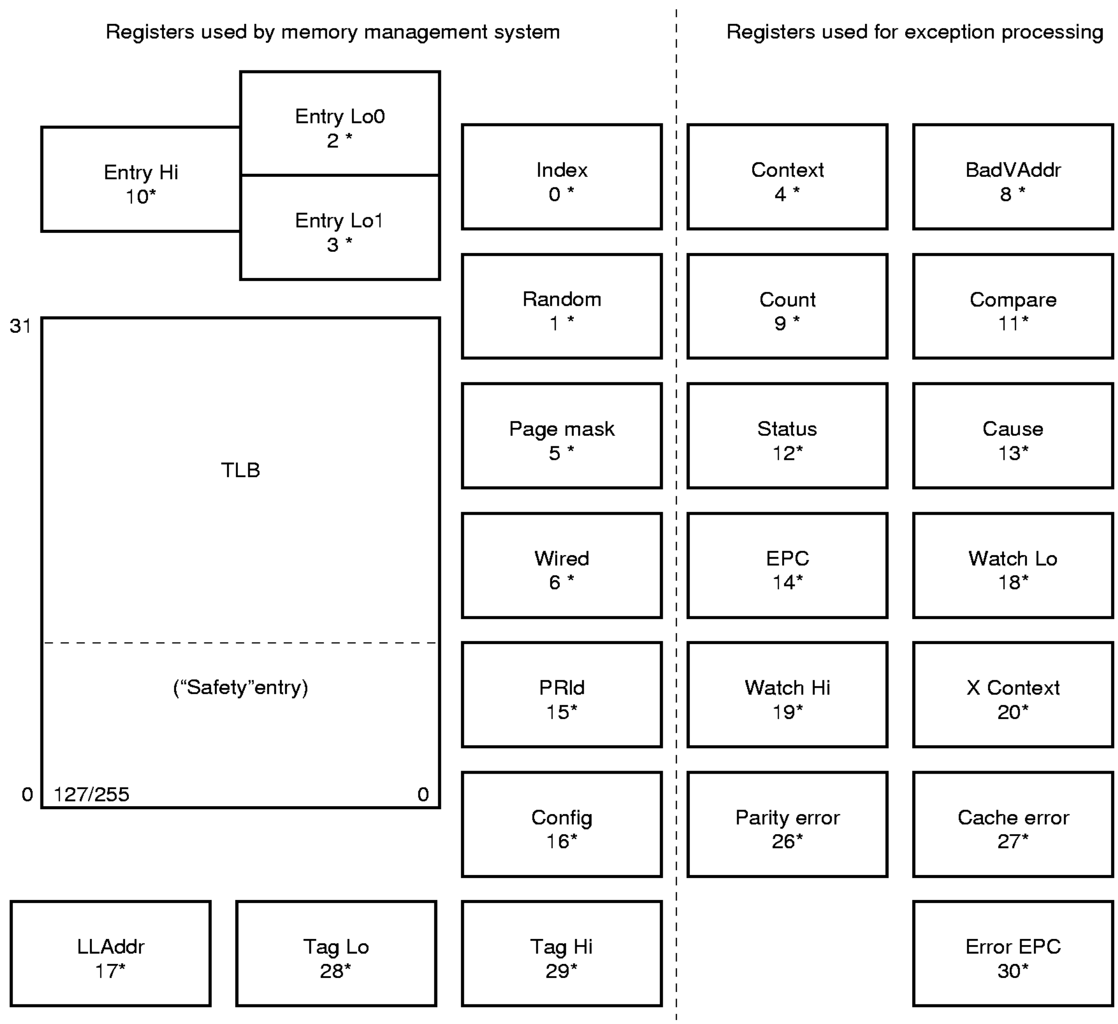
3.3 System Control Coprocessor (CP0)

The CP0 register/CP0 instruction accesses the TLB and cache. Moreover, operation of the mode using the processor, exception, and interrupt processing are also controlled by CP0. Further, a test/debug function is also provided to CP0.

The CP0 register of the VR4300 is compatible with the VR4200™, but the registers related to parity errors don't have a meaning.

All the CP0 registers of the VR4300 that can be used are listed below. Writing or reading an unused register (RFU) is undefined.

Figure 3-3. CP0 Registers and TLB



Remark " * " indicates register number.

Table 3-1. CP0 Registers

Number	Register	Description
0	Index	Programmable pointer to TLB entry
1	Random	Random pointer to TLB entry
2	Entry Lo0	Second half of TLB entry for even VPN
3	Entry Lo1	Second half of TLB entry for odd VPN
4	Context	Pointer to PTE table
5	Page mask	TLB page mask
6	Wired	Number of wired TLB entries
7	–	RFU (Reserved for Future Use)
8	BadVAddr	Virtual address at which error occurs last
9	Count	Timer count
10	Entry Hi	First half of TLB entry
11	Compare	Timer comparison
12	Status	Status register
13	Cause	Cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision identifier
16	Config	Configuration register
17	LLAddr	Address of LL instruction
18	Watch Lo	Low-order bit of memory reference trap address
19	Watch Hi	High-order bit of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21 to 25	–	RFU
26	Parity error[Note]	Parity error of cache
27	Cache error[Note]	Index and status field of cache error
28	Tag Lo	Cache tag register, low-order
29	Tag Hi	Cache tag register, high-order (reserved register)
30	Error EPC	Error exception program counter
31	–	RFU

Note This register is defined to preserve software compatibility with the VR4200.
It has no effect on the operation of the VR4300.

3.4 Data Format and Addressing

The VR4300 uses the following four types of data formats.

Double word (64 bits)
Word (32 bits)
Half-word (16 bits)
Byte (8 bits)

When the data format is double-word, word, or half-word, the alignment of bytes can be set to either big endian or little endian with the configuration register BE bit.

Figure 3-4. Byte Address in Word: Big Endian

	31 24	23 16	15 8	7 0	Word address
High-order address	12	13	14	15	12
	8	9	10	11	8
	4	5	6	7	4
Low-order address	0	1	2	3	0

Remarks 1. The most significant byte is at the lowest address.

2. The word is addressed at the highest address.

Figure 3-5. Byte Address in Word: Little Endian

	31 24	23 16	15 8	7 0	Word address
High-order address	15	14	13	12	12
	11	10	9	8	8
	7	6	5	4	4
Low-order address	3	2	1	0	0

Remarks 1. The least significant byte is at the lowest address.

2. The word is addressed at the lowest address.

Figure 3-6. Byte Address in Double-Word: Big Endian

	Word				Half word			Byte	
	63			32	31	16	15 8	7 0	Double-word address
High-order address	16	17	18	19	20	21	22	23	16
	8	9	10	11	12	13	14	15	8
Low-order address	0	1	2	3	4	5	6	7	0

Remarks **1.** The most significant byte is at the lowest address.

2. The word is addressed at the highest address.

Figure 3-7. Byte Address in Double-Word: Little Endian

	Word				Half word			Byte	
	63			32	31	16	15 8	7 0	Double-word address
High-order address	23	22	21	20	19	18	17	16	16
	15	14	13	12	11	10	9	8	8
Low-order address	7	6	5	4	3	2	1	0	0

Remarks **1.** The least significant byte is at the lowest address.

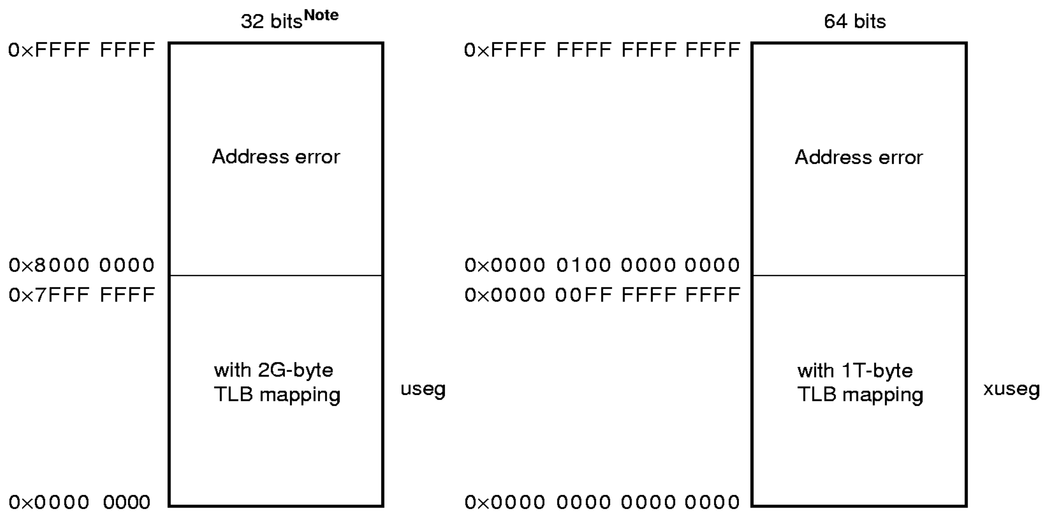
2. The word is addressed at the lowest address.

3.5 Virtual Memory

(1) Virtual address space

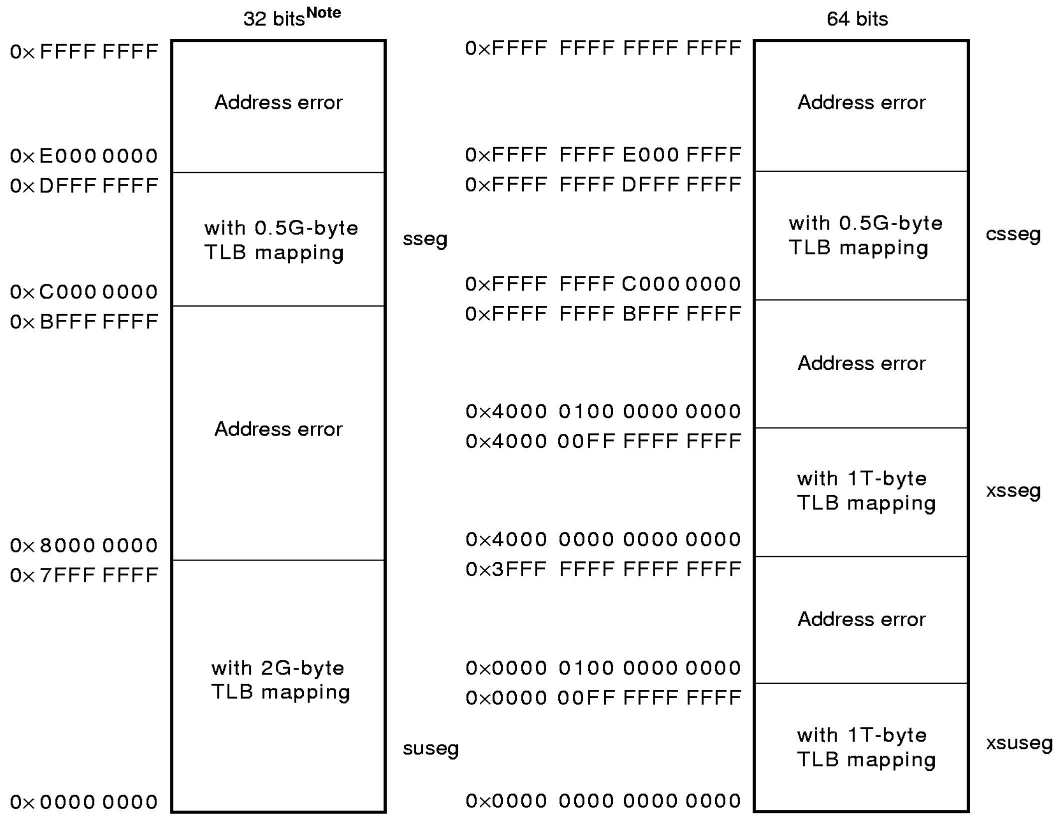
The VR4300 has two operation modes: 32-bit and 64-bit modes. It also has three operating modes: user, supervisor, and kernel. The figures below show the virtual address spaces in each operating mode.

Figure 3-8. User Mode Address Space



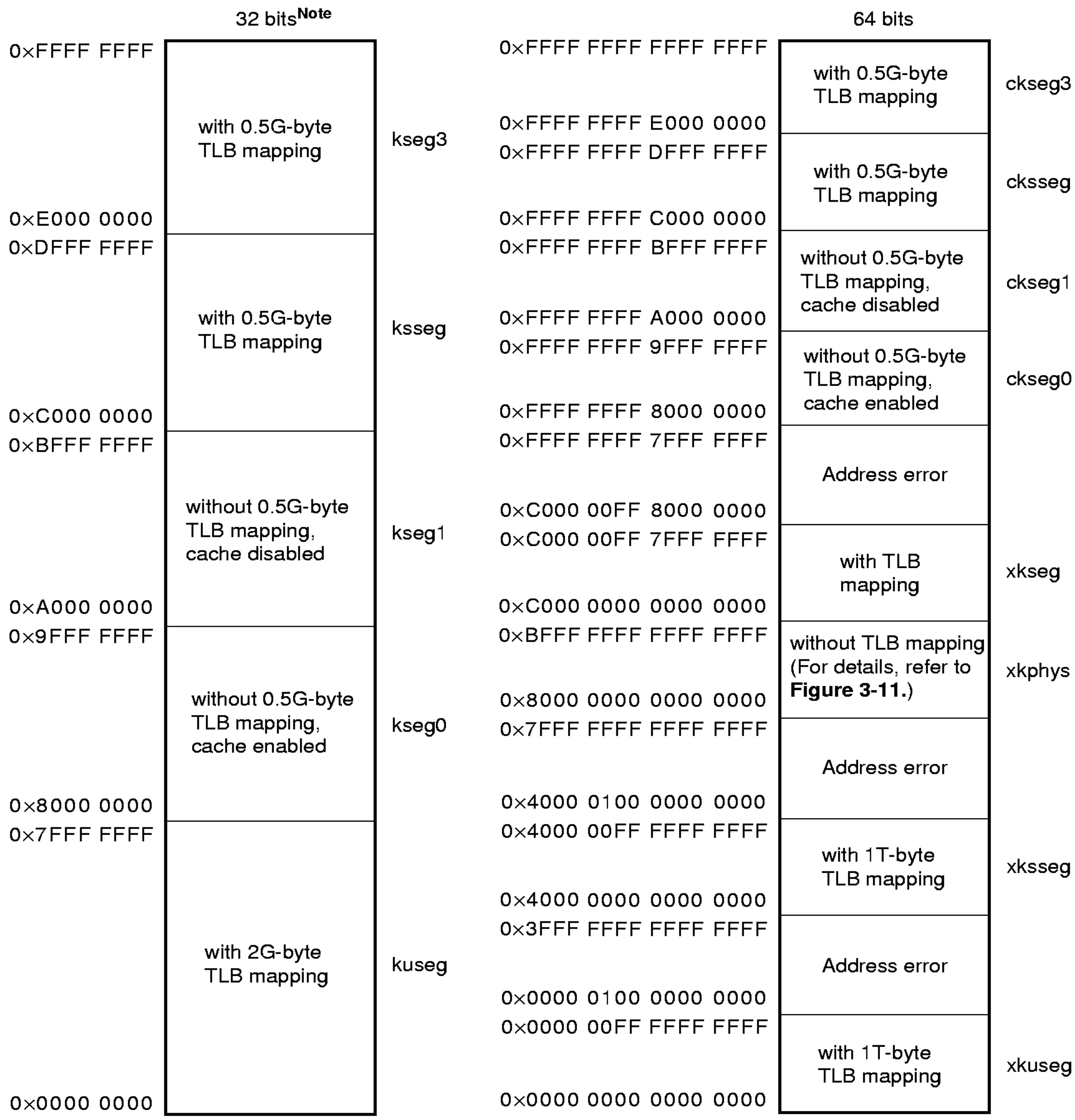
Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4300, VR4305, VR4310 User's Manual**.

Figure 3-9. Supervisor Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4300, VR4305, VR4310 User's Manual**.

Figure 3-10. Kernel Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4300, VR4305, VR4310 Manual**.

Figure 3-11. Details of xkphys Area

Start address	End address	Area
0xB800 0001 0000 0000	0xBFFF FFFF FFFF FFFF	Address error
0xB800 0000 0000 0000	0xB800 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0xB000 0001 0000 0000	0xB7FF FFFF FFFF FFFF	Address error
0xB000 0000 0000 0000	0xB000 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0xA800 0001 0000 0000	0xAFFF FFFF FFFF FFFF	Address error
0xA800 0000 0000 0000	0xA800 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0xA000 0001 0000 0000	0xA7FF FFFF FFFF FFFF	Address error
0xA000 0000 0000 0000	0xA000 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0x9800 0001 0000 0000	0x9FFF FFFF FFFF FFFF	Address error
0x9800 0000 0000 0000	0x9800 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0x9000 0001 0000 0000	0x97FF FFFF FFFF FFFF	Address error
0x9000 0000 0000 0000	0x9000 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache disabled
0x8800 0001 0000 0000	0x8FFF FFFF FFFF FFFF	Address error
0x8800 0000 0000 0000	0x8800 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used
0x8000 0001 0000 0000	0x87FF FFFF FFFF FFFF	Address error
0x8000 0000 0000 0000	0x8000 0000 FFFF FFFF	With 4G bytes w/o TLB mapping cache used

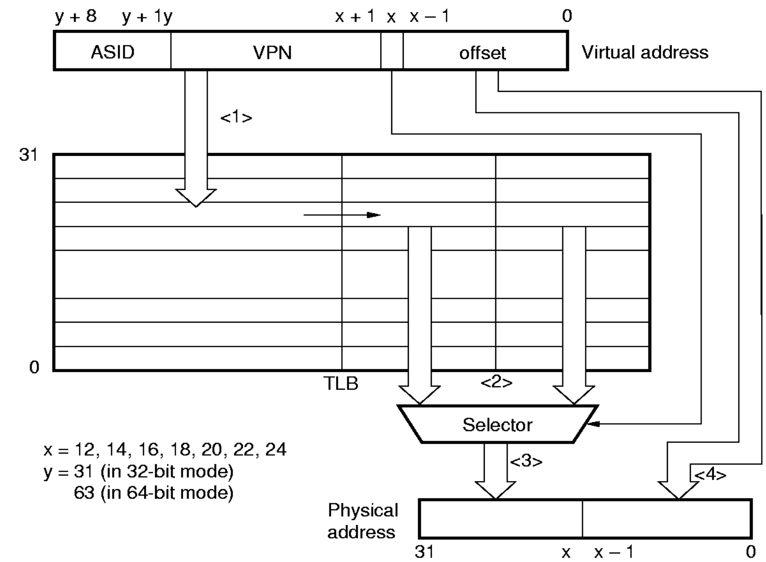
(2) Address conversion

Conversion from virtual addresses to physical addresses is performed per page by the built-in TLB (Translation Lookaside Buffer). The TLB, which is based on a full-associative configuration, has 64 entries on the virtual address side and 32 entries on the physical address side. The page size can be varied between 4 KB and 16 MB.

In case no TLB entry is hit, a TLB mismatch exception occurs in 32-bit mode; and an XTLB mismatch exception in 64-bit mode. Use software to reshuffle the TLB contents.

The address conversion is shown below diagramatically.

Figure 3-12. Overview of Address Conversion



<1> A virtual address page number (VPN) is compared with VPN in TLB.

<2> If the two VPNs coincide, a page frame number (PFN) indicating the high-order bits of a physical address is output to the selector.

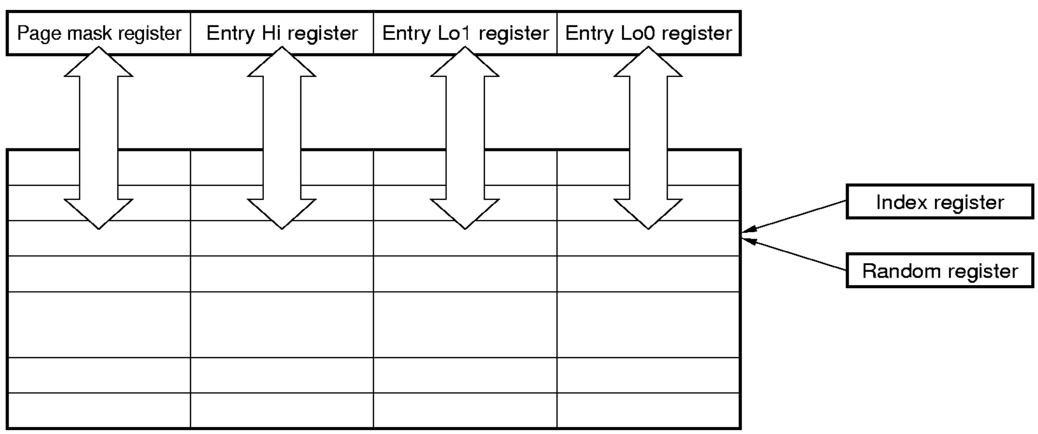
<3> If the low-order bit of VPN is 0, an even page is selected; if the bit is 1, an odd page is selected. The selected page is output to the high-order bits of the physical address.

<4> The offset is output to the low-order bits of the physical address not via TLB.

Reading and writing of TLB entries is performed by loading/storing between the TLB entry specified by the index register or the random register, and the entry Hi, entry Lo1, entry Lo0, and page mask registers.

The overview of TLB operation is shown below.

Figure 3-13. Overview of TLB Operation



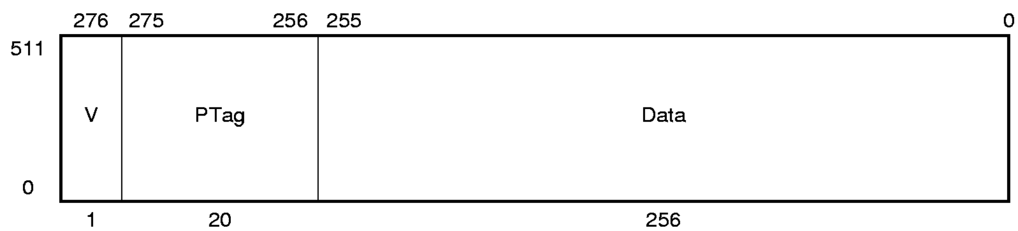
3.6 Caches

(1) Instruction cache

The features of the instruction cache are listed below.

- Built-in cache memory
- Capacity: 16 KB
- Direct mapping
- Virtual index address
- Physical tag check
- 8-word (32-byte) cache line

Figure 3-14. Instruction Cache Format



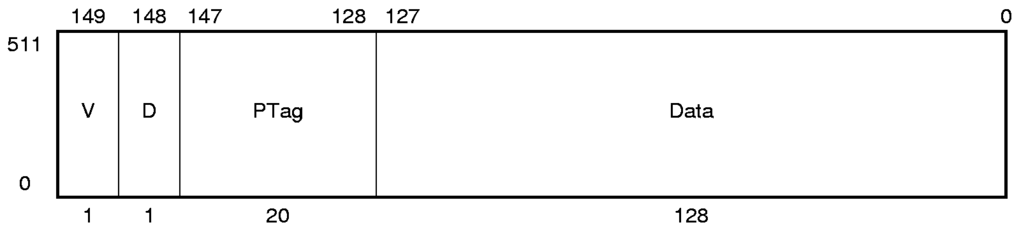
PTag : Physical tag (bits 31-12 of physical address)
V : Valid bit
Data : Cache data

(2) Data cache

The features of the data cache are listed below.

- Built-in cache memory
- Capacity: 8 KB
- Write back
- Direct mapping
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-15. Data Cache Format



PTag : Physical tag (bits 31-12 of physical address)
V : Valid bit
Data : Cache data
D : Dirty bit

3.7 Exception Processing

If an exception is detected, interrupts are inhibited, the operating mode is changed to kernel mode, and a jump is made to the specified exception handler.

In the case that an exception has occurred, the EPC register retains the restart address for restarting the execution. The restart address is the address of the instruction that was the cause of the exception, or, in the case where the instruction was being executed in the branch delay slot, the address of the immediately preceding branch instruction. On reset, when the NMI occurs, the restart address is retained in the error EPC register.

Table 3-2. Types of Exceptions

Exception	Abbreviation	Description
Reset	–	Aborts instruction execution and executes a handler on the reset vector. The internal status is undefined, except some bits of the status and config registers.
Software reset	–	Aborts instruction execution and executes a handler on the reset vector. The internal status before software reset is retained.
NMI	–	Non-maskable interrupt request by the external agent.
TLB mismatch	TLBL/TLBS	Occurs if the operating mode is the 32-bit mode and the number of TLB entries matching the referenced address runs short.
XTLB mismatch	TLBL/TLBS	Occurs if the operating mode is 64-bit mode and the number of TLB entries matching the referenced address runs short.
TLB invalid	TLBL/TLBS	Occurs if the TLB entry matching the referenced virtual address is invalid.
TLB change	Mod	Occurs when the matching TLB entry is valid but write is disabled (D bit = 0) when a virtual address is written.
Bus error	IBE/DBE	Occurs if an external agent inputs data accompanied with an error indication to the CPU due to an abnormality in the external system such as bus time out, or abnormality of address or access type.
Address error	AdEL/AdES	Occurs if an attempt is made to execute the LH, SH/LW/SW, LD, or SD instruction to the half word/word/double word not at the half word/word/double word boundary, or to reference a virtual address that cannot be accessed.
Integer overflow	Ov	Occurs if 2's complement overflow occurs as a result of addition or subtraction.
Trap	Tr	Occurs if the trap condition is true.
System call	Sys	Occurs when the SYSCALL instruction is executed.
Breakpoint	Bp	Occurs when the BREAK instruction is executed.
Reserved instruction	RI	Occurs when an instruction whose op code (bits 31-26) is undefined, or the SPECIAL instruction whose op code (bits 5-0) is undefined is executed.
Coprocessor unusable	CpU	Occurs if the coprocessor instruction is executed when the corresponding coprocessor use enable bit is not set.
Floating point	FPE	Occurs if a floating-point operation exception occurs in the floating-point operation coprocessor and when the corresponding enable bit is set.
Interrupt	Int	Occurs when one of the eight interrupt sources becomes active.
Watch	WATCH	Occurs when an attempt is made to reference the physical address in the watch Lo/Hi register with the load/store instruction.

The exception vectors and their offset values in the 64-bit and 32-bit modes are shown in the tables below.

Table 3-3. Base Address of Exception Vector in 64-Bit Mode

	Vector Base Address	Vector Offset
Cold reset, software reset, NMI	0xFFFF FFFF BFC0 0000 (BEV bit is automatically set to 1.)	0x0000
TLB mismatch, EXL = 0	0xFFFF FFFF 8000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0000
XTLB mismatch, EXL = 0		0x0080
Others		0x0180

Table 3-4. Base Address of Exception Vector in 32-Bit Mode

	Vector Base Address	Vector Offset
Cold reset, software reset, NMI	0xBFC0 0000 (BEV bit is automatically set to 1.)	0x0000
TLB mismatch, EXL = 0	0x8000 0000 (BEV = 0 0xBFC0 0200 (BEV = 1)	0x0000
XTLB mismatch, EXL = 0		0x0080
Others		0x0180

4. FPU INTERNAL ARCHITECTURE

VR4300's FPU (floating-point arithmetic unit) is integrated into the CPU (integer arithmetic unit). The CPU and the FPU use the same data bus, and FPU instructions are executed by the CPU hardware.

The VR4300 deals with the FPU as a logically independent coprocessor (CP1), thus making it possible to execute all the floating-point instructions defined by MIPS ISA.

4.1 FPU Registers

(1) Floating-point general-purpose registers (FGR)

These are the 32 physical general-purpose registers that can be accessed directly. The bit length varies depending on the contents of the status register FR bit.

(2) Floating-point registers (FPR)

These are the logical 64-bit registers, that hold floating-point values while floating-point arithmetic is being performed. Their number varies depending on the contents of the status register FR bit.

(3) Floating-point control registers (FCR)

The following two FCR registers are provided.

(a) Control/status register (FCR31)

This register controls and monitors exceptions, holds the arithmetic comparison results, and sets the rounding mode.

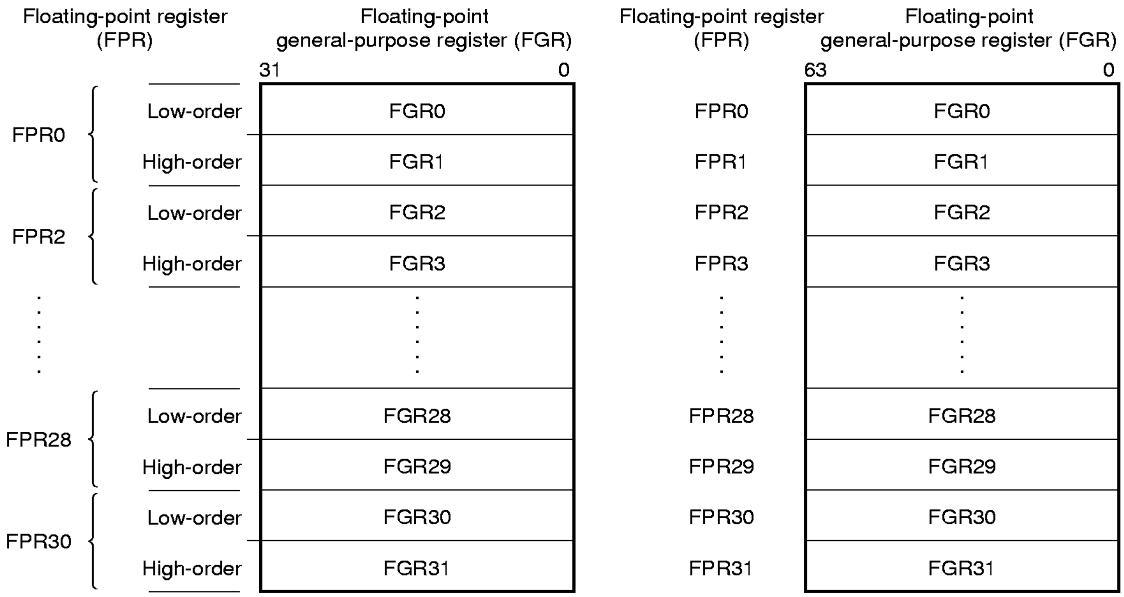
(b) Processor/revision register (FCR0)

Holds the FPU's revision information.

Figure 4-1. FPU Registers

(a) FGR and FPR

(i) When FR bit = 0 (ii) When FR bit = 1



(b) FCR

(i) Control/status register (FCR31) (ii) Processor/revision register (FCR0)

4.2 Data Formats

(1) Floating-point format

The FPU supports 32-bit (single precision) and 64-bit (double precision) IEEE754 floating-point arithmetic.

(2) Fixed-point format

Fixed-point values are computed in 2's compliment format.

5. INTERFACES

5.1 System Interface

The processor's input/output timings are as follows:

- The processor output starts to change at the rising edge of SClock.
- The processor input is latched at the rising edge of SClock.

There are the following two system interface buses.

- SysAD (31:0) : This bus is for address and data transfer.
- SysCmd (4:0) : This bus is for command and data identifier transfer.

The SysAD and SysCmd buses are bidirectional and driven by the processor or an external agent. Depending on the direction, they are placed in either of the following two statuses.

- Master status : The bus is driven by the processor, because a processor request is issued.
- Slave status : The bus is driven by an external agent, because an external request is issued.

Depending on the information included in the SysAD bus, two cycles occur as follows.

- Address cycle : The SysAD bus contains a valid address.
- Data cycle : The SysAD bus contains valid data.

The interface control signals are briefly described below.

- $\overline{\text{EValid}}$: Activate this signal when an external agent is in the master status and the SysAD and SysCmd buses are valid.
- $\overline{\text{PValid}}$: This signal is activated when the processor is in the master status and the SysAD and SysCmd buses are valid.
- $\overline{\text{EReq}}$: Activate this signal when an external agent requests the right to use the interface.
- $\overline{\text{PReq}}$: This signal is activated when the processor requests the right to use the interface.
- $\overline{\text{PMaster}}$: This signal is activated when the processor is placed in the master status.
- $\overline{\text{EOK}}$: Activate this signal when an external agent becomes capable of accepting the processor request.

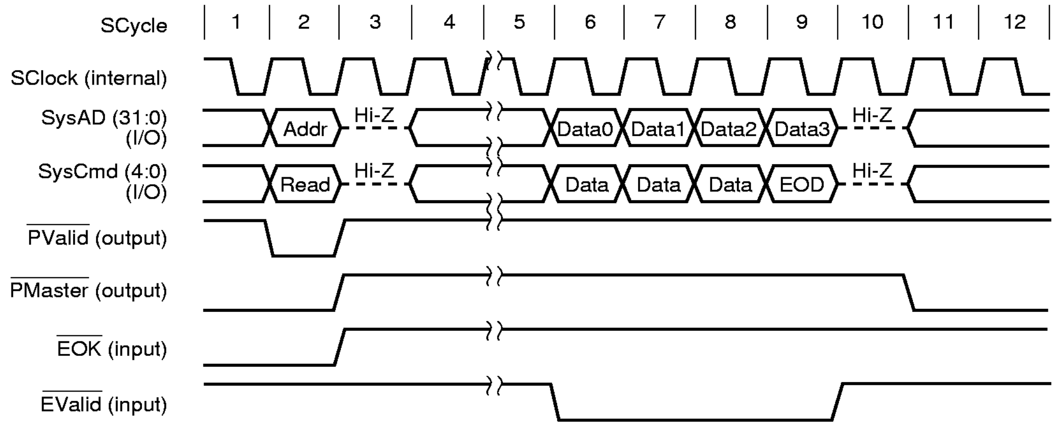
(1) System interface requests

The following requests are supported by the system interface.

Request	Outline	Data Unit
Processor read request	Read request to main memory or I/O	1 to 4 bytes (single); 2/4/8 word (block)
Processor write request	Write request to main memory or I/O	
External write request	Interrupt request from the system bus	1 word

As an example of the system interface request protocol, Figure 5-1 shows the timing between a processor block read request and the response.

Figure 5-1. Processor Block Read Request and Subsequent Read Response



(2) Control of data transfer rate

The system interface of the VR4300 can transfer word data in one cycle. However, the rate at which data is transferred to the processor is determined by the data transfer capability of the external agent.

The external agent can transfer data to the processor at any transfer rate. The processor decodes the contents of the SysCmd bus, including a data identifier, in a cycle in which the EValid signal is active and the data is valid. The processor continues receiving the data until it detects the last data transfer.

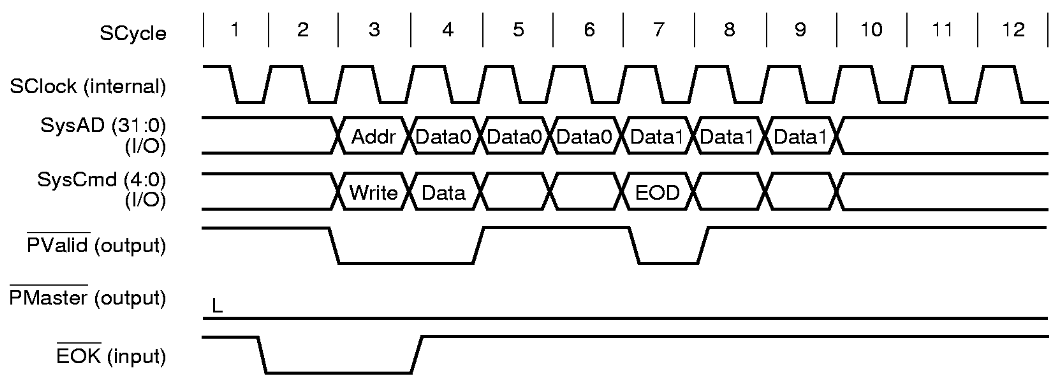
The rate at which data is transferred from the processor to the external agent is set by the EP field of the config register. The pattern of the data transfer rate is expressed by a combination of symbols “D” and “X”, where “D” indicates the data transfer cycle, and “X” indicates an unused cycle. This transfer pattern indicates an appropriate data transfer rate by a data cycle and unused cycle.

Example DXX: Transfers 1-word data every 3 cycles

In the VR4300, there are two data transmission rates: “D” and “DXX”. Also, the processor during the time period “X”, and SysAD (31:0) during the immediately preceding “D” time period preserve the data that was output and continue outputting.

Figure 5-2 shows the timing of the processor block write request when the transfer pattern is DXX.

Figure 5-2. Processor Block Write Request When Transfer Pattern Is DXX



(3) **Clock interface**

The clock signals used by the VR4300 are described below.

(a) **MasterClock (input)**

The VR4300's internal and external clocks are all generated and operate based on the MasterClock.

(b) **PClock (internal)**

This is the basic clock for pipeline operation. All the internal circuits use this clock.

- VR4300

Its frequency is a multiple of the MasterClock with the value specified by the DivMode (1:0) signal. The value settings that can be selected are listed below.

DivMode (1:0)	MasterClock:PClock
00	1:4 Note 1
01	1:1.5 Note 2
10	1:2
11	1:3

Notes 1. This setting is allowed with the 133 MHz model only. (With the 100 MHz model, this setting is reserved.)

2. This setting is allowed with the 100 MHz model only. (With the 133 MHz model, this setting is reserved.)

★ • VR4305

Its frequency is a multiple of the MasterClock with the value specified by the DivMode (1:0) signal. The value settings that can be selected are listed below.

DivMode (1:0)	MasterClock:PClock
00	1:1
01	Reserved
10	1:2
11	1:3

★ • VR4310

Its frequency is a multiple of the MasterClock with the value specified by the DivMode (2:0) signal. The value settings that can be selected are listed below.

DivMode (2:0)	MasterClock:PClock
000	1:5 Note 1
001	1:6 Note 1
010	1:2.5 Note 2
011	1:3
100	1:4
101	1:1.5
110	1:2
111	1:3

Notes 1. This setting is allowed with the 133 MHz and 167 MHz models only. (With the 100 MHz model, this setting is reserved.)

2. This setting is allowed with the 167 MHz model only. (With the 100 MHz and 133 MHz models, this setting is reserved.)

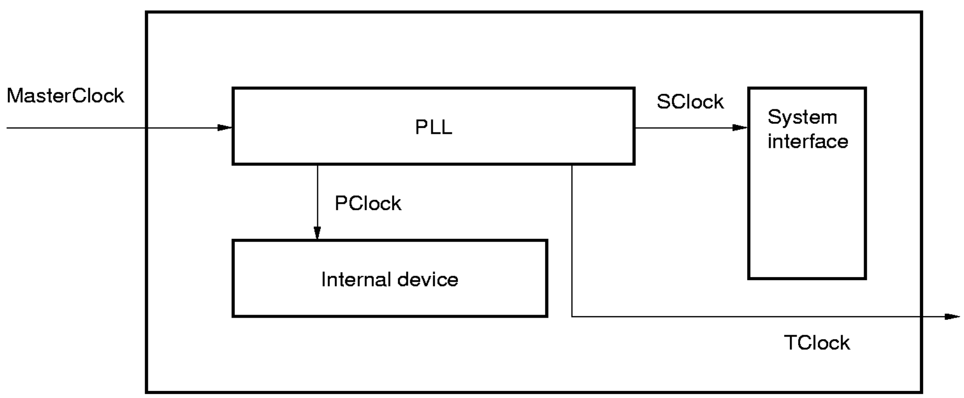
(c) SClock (internal)

This clock is the basis for the system interface. Its frequency is always the same as that of the MasterClock. Its phase is also in line with that of the MasterClock. However, being an internal clock, this clock is not supplied to an external agent.

(d) TClock (output)

This is the basic clock for the external agents. Its frequency is always the same as that of SClock in normal operation. Its phase is also in line with that of the SClock

Figure 5-3. Clock Interface



(e) Low-power mode

If the status register RP bit is set, the machine is placed in low-power mode.

In normal operation, the CPU's internal clock (PClock) is generated at the frequency ratio shown in (b) PClock (internal), based on the MasterClock.

In low-power mode, PClock, SClock, and TClock's frequencies can be reduced to a quarter of normal ones and the processor's power consumption can also be reduced to about a quarter of normal consumption.

6. INTERNAL/EXTERNAL CONTROL FUNCTIONS

6.1 Reset Function

The VR4300 has two reset signals: cold reset (ColdReset) and software reset (Reset). Setting of the necessary mode is controlled directly by pins and the config register.

(1) Cold reset

When ColdReset signal is asserted active, all the internal states, except the following registers, are initialized. At this time, either assert the Reset signal active/inactive in synchronization with Master Clock, or keep it inactive.

- Status register TS, SR, and RP bits and the configuration register EP bit: 0
- Status register ERL and BEV bits and the configuration register BE bit: 1
- Random register: Upper-limit value (31)
- Configuration register EC (2:0) bits: content of DivMode (1:0)[Note] pins

★ **Note** In the VR4300 and VR4305. DivMode (2:0) in the VR4310.

Control of the ColdReset signal does not have to be synchronized with the rising edge of the MasterClock. However, please synchronize the Reset signal with the MasterClock's rising edge.

(2) Software reset

This reset operation can be executed when the Reset signal is asserted active. This reset does not perform initialization, and the status before reset is retained as much as possible. However, if a multi-cycle instruction or floating-point operation instruction is aborted by this reset, the result is undefined.

6.2 Interrupt Functions

There are two major categories of interrupt requests as follows:

- Maskable interrupt requests
- Non-maskable interrupt (NMI) requests

(1) Maskable interrupt requests

These interrupts undergo mask control. The mask processing is performed by the status register. (Each interrupt can be handled individually, or interrupts can be handled as a group.)
There is no priority among interrupts.

(a) Hardware interrupt request (5 sources)

Accepted by activating an external write request or Int (4:0) signal.

(b) Software interrupt request (2 sources)

Accepted by setting the cause register IP0 and IP1 bits.

(c) Timer interrupt request (1 source)

If the value of the count register becomes equal to that of the compare register, the cause register IP7 bit is set and the interrupt is accepted.

(2) NMI request (1 source)

This interrupt request does not undergo mask control. The interrupt can be accepted by activating the external write request or $\overline{\text{NMI}}$ signal.

6.3 JTAG Function

The JTAG boundary scan mechanism tests the mutual connection between the processor and the other components. This mechanism does not test the processor itself.

As the minimum JTAG function, the VR4300 has the following. Functionally, however, only the external test function of the JTAG boundary scan register is provided:

- TAP controller
- JTAG instruction register
- JTAG bypass register
- JTAG boundary scan register

6.4 Hardware Debugging Support Functions

The VR4300 has a function in which, when the instruction address has been changed by a branch instruction, a jump instruction, or the occurrence of an exception, the VR4300 outputs the physical address of the branch destination from SysAD (31:0) by forcibly generating an instruction cache error.

This function can be used by setting bit 24 of the status register (ITS bit: instruction trace) to 1.

(1) Output of the branch destination address

This function forces an instruction cache error in the following cases.

- A branch condition is true when executing a branch instruction
- The PC content has been changed by a jump instruction or the occurrence of an exception.

If an instruction cache error occurs, a processor block read request is issued from SysAD (31:0). This enables the change of the address to be externally recognized.

For the processor block read request, please return response data in the same manner as in the case of a normal request. The address that is output is not a PC value (virtual address) but a physical address.

7. INSTRUCTION SET

The VR4300's instructions consist of 1 word (32 bits) located on a word boundary. The instruction format has three types as shown in Figure 7-1. Decoding of instructions is simplified by having only three format types. Complicated and infrequently used operations and addressing modes are realized by compilers.

7.1 Instruction Format

VR4300's instruction formats are as shown below.

Figure 7-1. CPU Instruction Formats

I-type (Immediate format)

31 – 26	25 – 21	20 – 16	15 – 0
op	rs	rt	immediate

J-type (Jump format)

31 – 26	25 – 0
op	target

R-type (Register format)

31 – 26	25 – 21	20 – 16	15 – 11	10 – 6	5 – 0
op	rs	rt	rd	sa	funct

op	6-bit instruction code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register, or branch condition
immediate	16-bit immediate value, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register specifier
sa	5-bit shift quantity
funct	6-bit function field

7.2 List of CPU Instruction Set

The VR4300's CPU instructions are classified into three categories: the instruction set (ISA: Instruction Set Architecture) common to all VR series processors, the instruction set (extended ISA) executed on the VR4000 series, and the system control coprocessor instruction set. The instruction set is listed below.

Table 7-1. CPU Instruction Set: ISA (1/3)

Instructions	Description	Format
Load/store instruction		op | base | rt | offset
LB	Load Byte	LB rt, offset (base)
LBU	Load Byte Unsigned	LBU rt, offset (base)
LH	Load Halfword	LH rt, offset (base)
LHU	Load Halfword Unsigned	LHU rt, offset (base)
LW	Load Word	LW rt, offset (base)
LWL	Load Word Left	LWL rt, offset (base)
LWR	Load Word Right	LWR rt, offset (base)
SB	Store Byte	SB rt, offset (base)
SH	Store Halfword	SH rt, offset (base)
SW	Store Word	SW rt, offset (base)
SWL	Store Word Left	SWL rt, offset (base)
SWR	Store Word Right	SWR rt, offset (base)
ALU immediate instruction		op | rs | rt | offset
ADDI	Add Immediate	ADDI rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU rt, rs, immediate
ANDI	And Immediate	ANDI rt, rs, immediate
ORI	Or Immediate	ORI rt, rs, immediate
XORI	Exclusive Or Immediate	XORI rt, rs, immediate
LUI	Load Upper Immediate	LUI rt, immediate
3-operand type instruction		op | rs | rt | rd | sa | funct
ADD	Add	ADD rd, rs, rt
ADDU	Add Unsigned	ADDU rd, rs, rt
SUB	Subtract	SUB rd, rs, rt
SUBU	Subtract Unsigned	SUBU rd, rs, rt
SLT	Set On Less Than	SLT rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU rd, rs, rt
AND	And	AND rd, rs, rt
OR	Or	OR rd, rs, rt
XOR	Exclusive Or	XOR rd, rs, rt
NOR	Nor	NOR rd, rs, rt
Shift instruction		op | rs | rt | rd | sa | funct
SLL	Shift Left Logical	SLL rd, rt, sa
SRL	Shift Right Logical	SRL rd, rt, sa
SRA	Shift Right Arithmetic	SRA rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV rd, rt, rs

Table 7-1. CPU Instruction Set: ISA (2/3)

Instructions	Description	Format	
Multiplication/division instruction	op | rs | rt | rd | sa | funct		
MULT	Multiply	MULT	rs, rt
MULTU	Multiply Unsigned	MULTU	rs, rt
DIV	Divide	DIV	rs, rt
DIVU	Divide Unsigned	DIVU	rs, rt
MFHI	Move From HI	MFHI	rd
MFLO	Move From LO	MFLO	rd
MTHI	Move To HI	MTHI	rs
MTLO	Move To LO	MTLO	rs
Jump instruction (1)	op | target		
J	Jump	J	target
JAL	Jump And Link	JAL	target
Jump instruction (2)	op | rs | rt | rd | sa | funct		
JR	Jump Register	JR	rs
JALR	Jump And Link Register	JALR	rs, rd
Branch instruction (1)	op | rs | rt | offset		
BEQ	Branch On Equal	BEQ	rs, rt, offset
BNE	Branch On Not Equal	BNE	rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ	rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ	rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset		
BLTZ	Branch On Less Than Zero	BLTZ	rs, offset
BGEZ	Branch On Greater Than Or Equal to Zero	BGEZ	rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL	rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL	rs, offset
Special instruction	SPECIAL | rs | rt | rd | sa | funct		
SYNC	Synchronize	SYNC	
SYSCALL	System Call	SYSCALL	
BREAK	Breakpoint	BREAK	
Coprocessor instruction (1)	op | base | rt | offset		
LWCz	Load Word To Coprocessor z	LWCz	rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz	rt, offset (base)
Coprocessor instruction (2)	COPz | sub | rt | rd | 0		
MTCz	Move To Coprocessor z	MTCz	rt, rd
MFCz	Move From Coprocessor z	MFCz	rt, rd
CTCz	Move Control To Coprocessor z	CTCz	rt, rd
CFCz	Move Control From Coprocessor z	CFCz	rt, rd

Table 7-1. CPU Instruction Set: ISA (3/3)

Instructions	Description	Format
Coprocessor instruction (3)	COPz | CO | cofun	
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instruction (4)	COPz | BC | br | offset	
BCzT	Branch On Coprocessor z True	BCzT offset
BCzF	Branch On Coprocessor z False	BCzF offset

Table 7-2. CPU Instruction Set: Etended ISA (1/2)

Instructions	Description	Format
Load/store instruction	op | base | rt | offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LL	Load Linked	LL rt, offset (base)
LLD	Load Linked Doubleword	LLD rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SC	Store Conditional	SC rt, offset (base)
SCD	Store Conditional Doubleword	SCD rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
ALU immediate instruction	op | rs | rt | immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op | rs | rt | rd	sa | funct
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op | rs | rt | rd	sa | funct
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shift Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, rs
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, rs
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, rs
DSLL32	Doubleword Shift Left Logical + 32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logical + 32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic + 32	DSRA32 rd, rt, sa

Table 7-2. CPU Instruction Set: Extended ISA (2/2)

Instructions	Description	Format	
Multiplication/division instruction	op | rs | rt | rd | sa | funct		
DMULT	Doubleword Multiply	DMULT	rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU	rs, rt
DDIV	Doubleword Divide	DDIV	rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU	rs, rt
Branch instruction (1)	op | rs | rt | offset		
BEQL	Branch On Equal Likely	BEQL	rs, rt, offset
BNEL	Branch On Not Equal Likely	BNEL	rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely	BLEZL	rs, offset
BGTZL	Branch On Greatrer Than Zero Likely	BGTZL	rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset		
BLTZL	Branch On Less Than Zero Likely	BLTZL	rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely	BGEZL	rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely	BLTZALL	rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely	BGEZALL	rs, offset
Exception instruction	SPECIAL | rs | rt | rd | sa | funct		
TGE	Trap If Greater Than Or Equal	TGE	rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned	TGEU	rs, rt
TLT	Trap If Less Than	TLT	rs, rt
TLTU	Trap If Less Than Unsigned	TLTU	rs, rt
TEQ	Trap If Equal	TEQ	rs, rt
TNE	Trap If Not Equal	TNE	rs, rt
Exception immediate instruction	REGIMM | rs | sub | immediate		
TGEI	Trap If Greater Than Or Equal Immediate	TGEI	rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned	TGEIU	rs, immediate
TLTI	Trap If Less Than Immediate	TLTI	rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned	TLTIU	rs, immediate
TEQI	Trap If Equal Immediate	TEQI	rs, immediate
TNEI	Trap If Not Equal Immediate	TNEI	rs, immediate
Coprocessor instruction (1)	COPz | sub | rt | rd | 0		
DMFCz	Doubleword Move From Coprocessor z	DMFCz	rt, rd
DMTCz	Doubleword Move To Coprocessor z	DMTCz	rt, rd
Coprocessor instruction (2)	op | base | rt | offset		
LDCz	Load Doubleword To Coprocessor z	LDCz	rt, offset (base)
SDCz	Store Doubleword From Coprocessor z	SDCz	rt, offset (base)
Coprocessor instruction (3)	COPz | BC | br | offset		
BCzTL	Branch On Coprocessor z True Likely	BCzTL	offset
BCzFL	Branch On Coprocessor z False Likely	BCzFL	offset

Table 7-3. System Control Coprocessor (CP0) Instruction Set

Instructions	Description	Format
System control coprocessor instruction (1)	COP0 | sub | rt | rd | 0	
MFC0	Move From Coprocessor 0	MFC0 rt, rd
MTC0	Move To Coprocessor 0	MTC0 rt, rd
DMFC0	Doubleword Move From Coprocessor 0	DMFC0 rt, rd
DMTC0	Doubleword Move To Coprocessor 0	DMTC0 rt, rd
System control coprocessor instruction (2)	COP0 | CO | funct	
TLBR	Read Indexed TLB Entry	TLBR
TLBWI	Write Indexed TLB Entry	TLBWI
TLBWR	Write Random TLB Entry	TLBWR
TLBP	Probe TLB For Matching Entry	TLBP
ERET	Exception Return	ERET
System control coprocessor instruction (3)	CACHE | base | sub | offset	
CACHE	Cache Operation	CACHE sub, offset (base)

7.3 List of FPU Instruction Set

All FPU instructrions are 32 bits and are aligned on word boundaries.

Table 7-4 shows the FPU instruction set.

Table 7-4. FPU Instructions

Instructions	Description	Format
Load/store instruction	op | base | ft | offset	
LWC1	Load Word To FPU	LWC1 ft, offset (base)
SWC1	Store Word From FPU	SWC1 ft, offset (base)
LDC1 Load	Doubleword To FPU	LDC1 ft, offset (base)
SDC1 Store	Doubleword From FPU	SDC1 ft, offset (base)
Transfer instruction	COP1 | sub | rt | fs | 0	
MTC1	Move Word To FPU	MTC1 rt, fs
MFC1	Move Word From FPU	MFC1 rt, fs
CTC1	Move Control Word To FPU	CTC1 rt, fs
CFC1	Move Control Word From FPU	CFC1 rt, fs
DMTC1	Doubleword Move To FPU	DMTC1 rt, fs
DMFC1	Doubleword Move From FPU	DMFC1 rt, fs
Conversion instruction	COP1 | fmt | 0 | fs | fd | funct	
CVT. S. fmt	Floating-point Convert To Single Floating-point Format	CVT. S. fmt fd, fs
CVT. D. fmt	Floating-point Convert To Double Floating-point Format	CVT. D. fmt fd, fs
CVT. L. fmt	Floating-point Convert To Long Fixed-point Format	CVT. L. fmt fd, fs
CVT. W. fmt	Floating-point Convert To Single Fixed-point Format	CVT. W. fmt fd, fs
ROUND. L. fmt	Floating-point Round To Long Fixed-point Format	ROUND. L. fmt fd, fs
ROUND. W. fmt	Floating-point Round To Single Fixed-point Format	ROUND. W. fmt fd, fs
TRUNC. L. fmt	Floating-point Truncate To Long Fixed-point Format	TRUNC. L. fmt fd, fs
TRUNC. W. fmt	Floating-point Truncate To Single Fixed-point Format	TRUNC. W. fmt fd, fs
CEIL. L. fmt	Floating-point Ceiling To Long Fixed-point Format	CEIL. L. fmt fd, fs
CEIL. W. fmt	Floating-point Ceiling To Single Fixed-point Format	CEIL. W. fmt fd, fs
FLOOR. L. fmt	Floating-point Floor To Long Fixed-point Format	FLOOR. L. fmt fd, fs
FLOOR. W. fmt	Floating-point Floor To Single Fixed-point Format	FLOOR. W. fmt fd, fs
Arithmetic operation instruction	COP1 | fmt | ft | fs | fd | funct	
ADD. fmt	Floating-point Add	ADD. fmt fd, fs, ft
SUB. fmt	Floating-point Subtract	SUB. fmt fd, fs, ft
MUL. fmt	Floating-point Multiply	MUL. fmt fd, fs, ft
DIV. fmt	Floating-point Divide	DIV. fmt fd, fs, ft
SQRT. fmt	Floating-point Square Root	SQRT. fmt fd, fs
ABS. fmt	Floating-point Absolute value	ABS. fmt fd, fs
MOV. fmt	Floating-point Move	MOV. fmt fd, fs
NEG. fmt	Floating-point Negate	NEG. fmt fd, fs
Compare instruction	COP1 | fmt | ft | fs | 0 | funct	
C. cond. fmt	Floating-point Compare C. cond. fmt fs, ft	
FPU branch instruction	COP1 | BC | br | offset	
BC1T	Branch On FPU True	BC1T offset
BC1F	Branch On FPU False	BC1F offset
BC1TL	Branch On FPU True Likely	BC1TL offset
BC1FL	Branch On FPU False Likely	BC1FL offset

7.4 Delay of Instruction

(1) Delay of integer operation instruction

Table 7-5 shows the delay of the integer operation instruction.

The VR4300 can execute a multiplication instruction with the number of cycles about 1/2 or 1/3 of that of the VR4200.

For the details of each instruction, refer to **VR4300, VR4305, VR4310 User's Manual**.

Table 7-5. Integer Operation Instruction Delay

Instruction Type	Pipeline Clock Cycle
Mult	5
MultU	5
DMult	8
DMultU	8
Div, DivU	37
DDiv, DDivU	69
Branch instr**Note 1**	1
Jump instr**Note 1**	1
Load instr**Note 2**	1
Store instr	1

Notes 1. The instruction at the branch destination is fetched at the EX stage of the branch instruction. Branch comparison and target address calculation are completed at Φ1 of the EX stage. Therefore, a branch delay slot of 1 cycle is necessary. Moreover, the jump instruction requires a delay slot of 1 cycle.

2. If the loaded result is used by the next instruction, the hardware generates interlock in order to maintain compatibility with the MIPS-II instruction set.

(2) Delay of floating-point operation instruction

Table 7-6 shows the execution delay cycle of the floating-point operation instruction.

The VR4300 can execute a multiplication instruction with less than 1/2 the number of cycles of the VR4200.

For the details of each instruction, refer to **VR4300, VR4305, VR4310 User's Manual**.

To improve the performance of the floating-point operation and to simplify designing, the execution unit employs a variable-length execution clock. Therefore, an instruction can be executed in 1 cycle in the following cases:

- When an exception can be detected by a source operand and early inspection (occurrence of an exception due to source data, etc.)
- When the result is determined by detection of a zero or infinite operand (numeric value other than $\infty \times 0$)

Table 7-6. Floating-Point Operation Instruction Delay

Instruction Type	Pipeline Clock Cycle			
	Single	Double	Word	Long Word
Add. fmt	3	3	–	–
Sub. fmt	3	3	–	–
Mul. fmt	5	8	–	–
Div. fmt	29	58	–	–
Sqrt. fmt	29	58	–	–
Abs. fmt	1	1	–	–
Mov. fmt	1	1	–	–
Neg. fmt	1	1	–	–
Round. W. fmt	5	5	–	–
Trunc. W. fmt	5	5	–	–
Ceil. W. fmt	5	5	–	–
Floor. W. fmt	5	5	–	–
Round. L. fmt	5	5	–	–
Trunc. L. fmt	5	5	–	–
Ceil. L. fmt	5	5	–	–
Floor. L. fmt	5	5	–	–
Cvt. s. fmt	–	2	5	5
Cvt. d. fmt	1	–	5	5
Cvt. W. fmt	5	5	–	–
Cvt. L. fmt	5	5	–	–
C. cond. fmt	1	1	–	–
BC1T**Note 1**	1	–	–	–
BC1F**Note 1**	1	–	–	–
BC1TL**Note 1**	1	–	–	–
BC1FL**Note 1**	1	–	–	–
LWC1**Note 2**	2/1	–	–	–
SWC1	1	–	–	–
LDC1**Note 2**	–	2/1	–	–
SDC1	–	1	–	–
MTC1	1	–	–	–
MFC1	1	–	–	–
CTC1	1	–	–	–
CFC1	1	–	–	–
DMTC1	–	1	–	–
DMFC1	–	1	–	–

Notes 1. The delay slot of the branch instruction of the floating-point operation coprocessor is the same as the delay slot of the integer branch instruction.

2. If the loaded result is used by the next instruction in the load delay slot, the hardware generates interlock in a cycle.

Remarks 1. If the result of one floating-point operation instruction (FP instruction) is used by the next FP instruction, add 1 to the number of cycles shown in the above table. This is because the result is passed from the DC stage to the EX stage of the next FP instruction.

2. The values shown in the above table is the number of cycles required for execution of ordinary operation instructions. Depending on the source data, execution may be completed in 1 or 2 cycles.

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage[Note]	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Operating case temperature	T_C		0 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note The upper limit of the input voltage (V_{DD} + 0.3) is +4.0 V.

Cautions 1. Do not short circuit two or more outputs at the same time.

2. If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

★ **DC Characteristics (T_C = 0 to +85 °C, V_{DD} = 3.3 ±0.3 V) : μPD30200-80, 30200-100**

★ **(T_C = 0 to +85 °C, V_{DD} = 3.0 to 3.5 V): μPD30200-133, 30210-xxx**

Parameter	Symbol	Condition		MIN.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = –400 μA		2.4		V
High-level output voltage[Note 1]	V_{OHC}	I_{OH} = –400 μA		2.7		V
Low-level output voltage	V_{OL}	I_{OL} = 2.5 mA			0.4	V
High-level input voltage	V_{IH}			2.0	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}			–0.5	+0.8	V
		Pulse of less than 10 ns		–1.5	+0.8	V
High-level input voltage[Note 2]	V_{IHC}			0.8 V_{DD}	V_{DD} + 0.3	V
Low-level input voltage[Note 2]	V_{ILC}			–0.5	0.2 V_{DD}	V
		Pulse of less than 10 ns		–1.5	0.2 V_{DD}	V
★ Supply current	I_{DD}	μPD30200	at 80 MHz		0.60	A
			at 100 MHz		0.67	A
			at 133 MHz		0.90	A
★		μPD30210	at 100 MHz		0.51	A
			at 133 MHz		0.69	A
			at 167 MHz		0.85	A
High-level input leakage current	I_{LIH}	V_I = V_{DD}			10	μA
Low-level input leakage current	I_{LIL}	V_I = 0 V			–10	μA
High-level output leakage current	I_{LOH}	V_O = V_{DD}			20	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V			–20	μA

Notes 1. Applied to the TClock pin.

2. Applied to the MasterClock pin only.

Remark The operating supply current is almost proportional to the operating clock frequency.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{In}	f_C = 1 MHz		10	pF
Output capacitance	C_{out}	Pins other than tested pin: 0 V		10	pF

★ **AC Characteristics (T_C = 0 to +85 °C, V_{DD} = 3.3 ±0.3 V) : μPD30200-80, 30200-100**

★ **(T_C = 0 to +85 °C, V_{DD} = 3.0 to 3.5 V): μPD30200-133, 30210-xxx**

Clock Parameter

(1) μPD30200-xxx

Parameter	Symbol	Condition	μPD30200-80		μPD30200-100		μPD30200-133		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Master clock high-level width	$t_{MCkHigh}$		3.5		3.5		3.5		ns
Master clock low-level width	t_{MCkLow}		3.5		3.5		3.5		ns
Master clock frequency[Note]		DivMode = 1:1	20	66.7	–	–	–	–	MHz
		DivMode = 1:2	20	66.7	20	66.7	34	66.7	MHz
		DivMode = 2:3	–	–	20	66.7	–	–	MHz
		DivMode = 1:3	20	66.7	20	66.7	24	66.7	MHz
		DivMode = 1:4	–	–	–	–	20	66.7	MHz
Master clock cycle	t_{MCkP}	DivMode = 1:1	15	50	–	–	–	–	ns
		DivMode = 1:2	15	50	15	50	15	29	ns
		DivMode = 2:3	–	–	15	50	–	–	ns
		DivMode = 1:3	15	50	15	50	15	41	ns
		DivMode = 1:4	–	–	–	–	15	50	ns
Clock jitter	$t_{MCJitter}$			±500		±500		±500	ps
Master clock rise time	t_{MCRise}			4.0		4.0		4.0	ns
Master clock fall time	t_{MCFall}			4.0		4.0		4.0	ns
JTAG clock cycle	$t_{JTAGCkP}$		4 × t_{MCkP}		4 × t_{MCkP}		4 × t_{MCkP}		ns

Note The operation of the internal PLL of the VR4300 is guaranteed. The RP mode is guaranteed when the master clock frequency is 40 MHz or higher.

★ **(2) µPD30210-xxx**

Parameter	Symbol	Condition	µPD30210-100		µPD30210-133		µPD30210-167		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Master clock high-level width	$t_{MCkHigh}$		3.5		3.5		3.5		ns
Master clock low-level width	t_{MCkLow}		3.5		3.5		3.5		ns
Master clock frequency[Note]		DivMode = 1.5	30	66.7	30	83.3	30	83.3	MHz
		DivMode = 2.0	50	50.0	50	66.7	50	83.3	MHz
		DivMode = 2.5	–	–	–	–	20	66.7	MHz
		DivMode = 3.0	30	33.3	30	44.4	30	55.6	MHz
		DivMode = 4.0	20	25.0	20	33.3	20	41.7	MHz
		DivMode = 5.0	–	–	20	26.7	20	33.3	MHz
		DivMode = 6.0	–	–	20	22.2	20	27.8	MHz
Master clock cycle	t_{MCkP}	DivMode = 1.5	15	33.3	12	33.3	12	33.3	ns
		DivMode = 2.0	20	20	15	20	15	20	ns
		DivMode = 2.5	–	–	–	–	15	50	ns
		DivMode = 3.0	30	33.3	22	33.3	18	33.3	ns
		DivMode = 4.0	40	50	30	50	24	50	ns
		DivMode = 5.0	–	–	37	50	30	50	ns
		DivMode = 6.0	–	–	45	50	36	50	ns
Clock jitter	$t_{MCJitter}$			±500		±500		±500	ps
Master clock rise time	t_{MCRise}			4.0		4.0		4.0	ns
Master clock fall time	t_{MCFall}			4.0		4.0		4.0	ns
JTAG clock cycle	$t_{JTAGCkP}$		$4 \times t_{MCkP}$		$4 \times t_{MCkP}$		$4 \times t_{MCkP}$		ns

Note The operation of the internal PLL of the VR4310 is guaranteed. The RP mode is guaranteed when the master clock frequency is 40 MHz or higher.

System Interface Parameter

★ **(1) μPD30200-80 (T_C = 0 to 85 °C, V_{DD} = 3.3 ±0.3 V)**

Parameter	Symbol	Condition	At 66.7 MHz Input[Note 3]		At 40 MHz Input[Note 3]		At 33.3 MHz Input[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		ns
Clock rise time[Note 2]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0	ns
Clock fall time[Note 2]	t_{COFall}			4.0		4.0		4.0	ns
Clock high-level width[Note 2]	t_{COHigh}		3.5		8.5		11.0		ns
Clock low-level width[Note 2]	t_{COLow}		3.5		8.5		11.0		ns

Notes **1.** Applied to all interface pins.
2. Applied to TClock pin.
3. Master clock frequency (example)

(2) μPD30200-100 (T_C = 0 to 85 °C, V_{DD} = 3.3 ±0.3 V)

Parameter	Symbol	Condition	At 66.7 MHz Input[Note 4]		At 62.5 MHz Input[Note 4]		At 50 MHz Input[Note 4]		At 33.3 MHz Input[Note 4]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		1.5		ns
Mode data setup time[Note 2]	t_{MDS}		3.5		3.5		3.5		3.5		ns
Clock rise time[Note 3]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0		4.0	ns
Clock fall time[Note 3]	t_{COFall}			4.0		4.0		4.0		4.0	ns
Clock high-level width[Note 3]	t_{COHigh}		3.5		4.0		6.0		11.0		ns
Clock low-level width[Note 3]	t_{COLow}		3.5		4.0		6.0		11.0		ns

Notes **1.** Applied to all interface pins (except DivMode (1:0) pin).
2. Applied to DivMode(1:0) pin.
3. Applied to TClock pin.
4. Master clock frequency (example)

(3) μPD30200-133 (T_C = 0 to 85 °C, V_{DD} = 3.0 to 3.5 V)

Parameter	Symbol	Condition	At 66.7 MHz Input[Note 4]		At 44.4 MHz Input[Note 4]		At 33.3 MHz Input[Note 4]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		ns
Mode data setup time[Note 2]	t_{MDS}		3.5		3.5		3.5		ns
Clock rise time[Note 3]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0	ns
Clock fall time[Note 3]	t_{COFall}			4.0		4.0		4.0	ns
Clock high-level width[Note 3]	t_{COHigh}		3.5		7.2		11.0		ns
Clock low-level width[Note 3]	t_{COLow}		3.5		7.2		11.0		ns

Notes **1.** Applied to all interface pins (except DivMode (1:0) pin).
2. Applied to DivMode(1:0) pins.
3. Applied to TClock pin.
4. Master clock frequency (example)

★ (4) μPD30210-xxx (T_C = 0 to 85 °C, V_{DD} = 3.0 to 3.5 V)

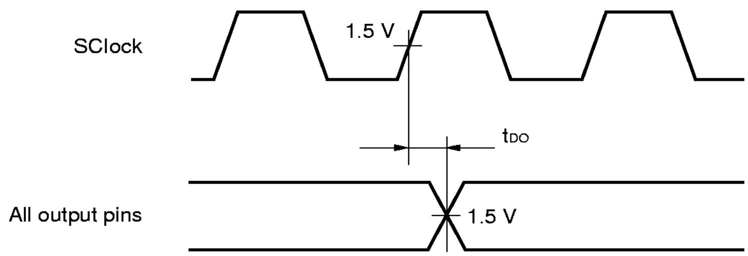
Parameter	Symbol	Condition		At 66.7 MHz Input[Note 3]		At 33.3 MHz Input[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	at 100/133 MHz	2.0	8.0	2.0	8.0	ns
			at 167 MHz	1.5	8.0	1.5	8.0	
Data setup delay time[Note 1]	t_{DS}			3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}			1.5		1.5		ns
Clock rise time[Note 2]	t_{CORise}	C_L = 50 pF			4.0		4.0	ns
Clock fall time[Note 2]	t_{COFall}				4.0		4.0	ns
Clock high-level width[Note 2]	t_{COHigh}			3.5		11.0		ns
Clock low-level width[Note 2]	t_{COLow}			3.5		11.0		ns

Notes **1.** Applied to all interface pins.
2. Applied to TClock pin.
3. Master clock frequency (example)

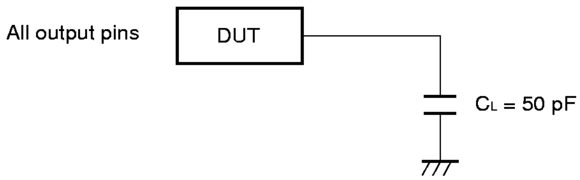
Load Coefficient

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			2	ns/25 pF

Test Condition

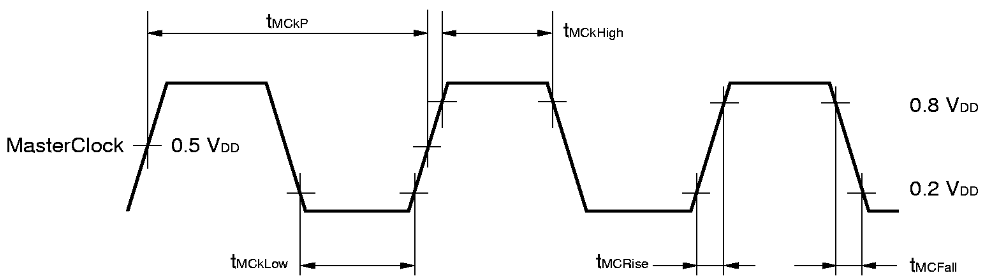


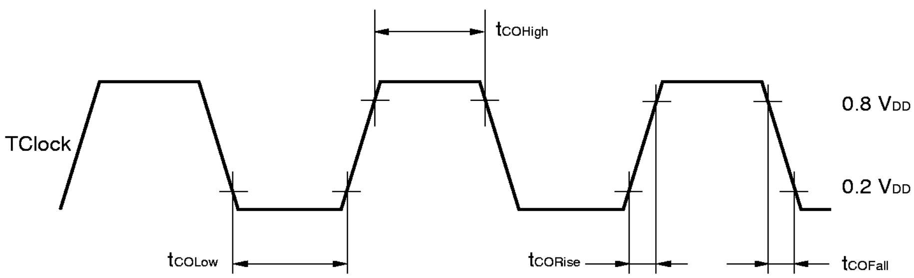
Test Load



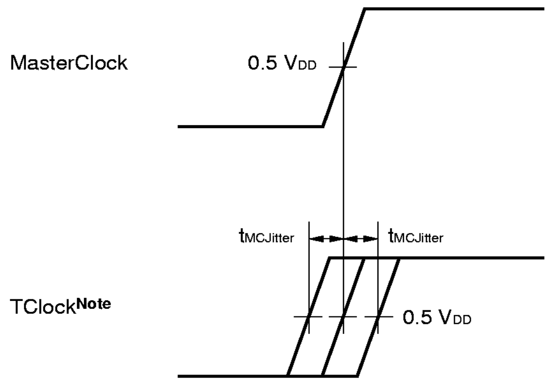
Timing Chart

Clock timing





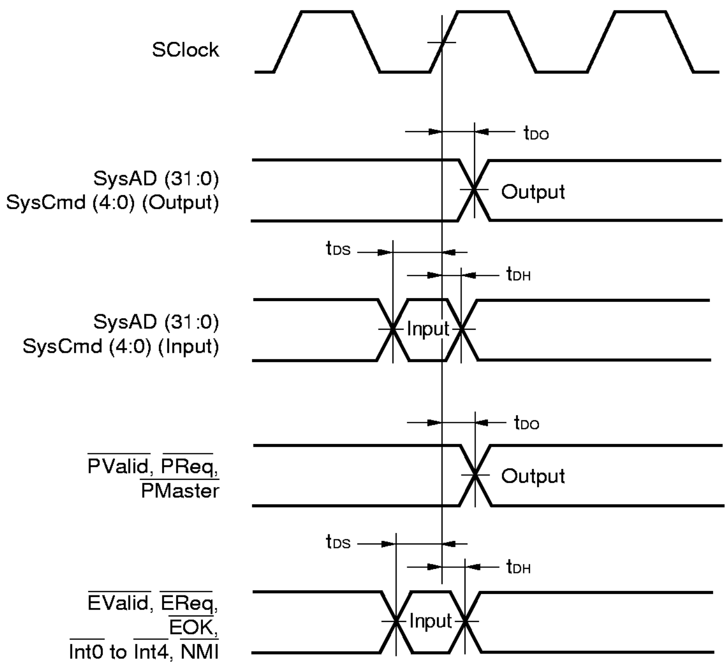
Clock jitter



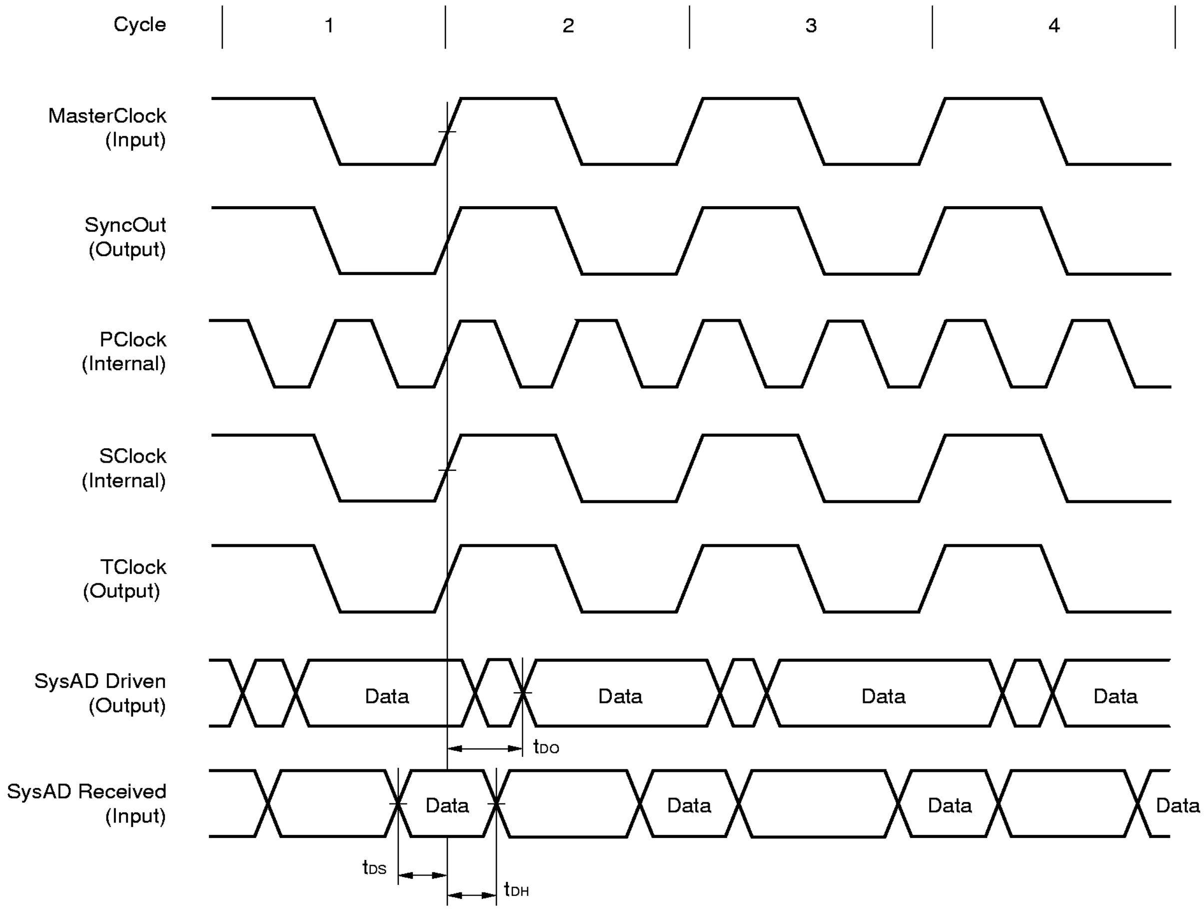
Note If SyncOut and SyncIn are connected with the shortest path, the point of TClock = 50 % is the point of MasterClock = 50 %.

Remark To match the MasterClock edge, keep the load capacitances of SyncIn/SyncOut path and TClock.

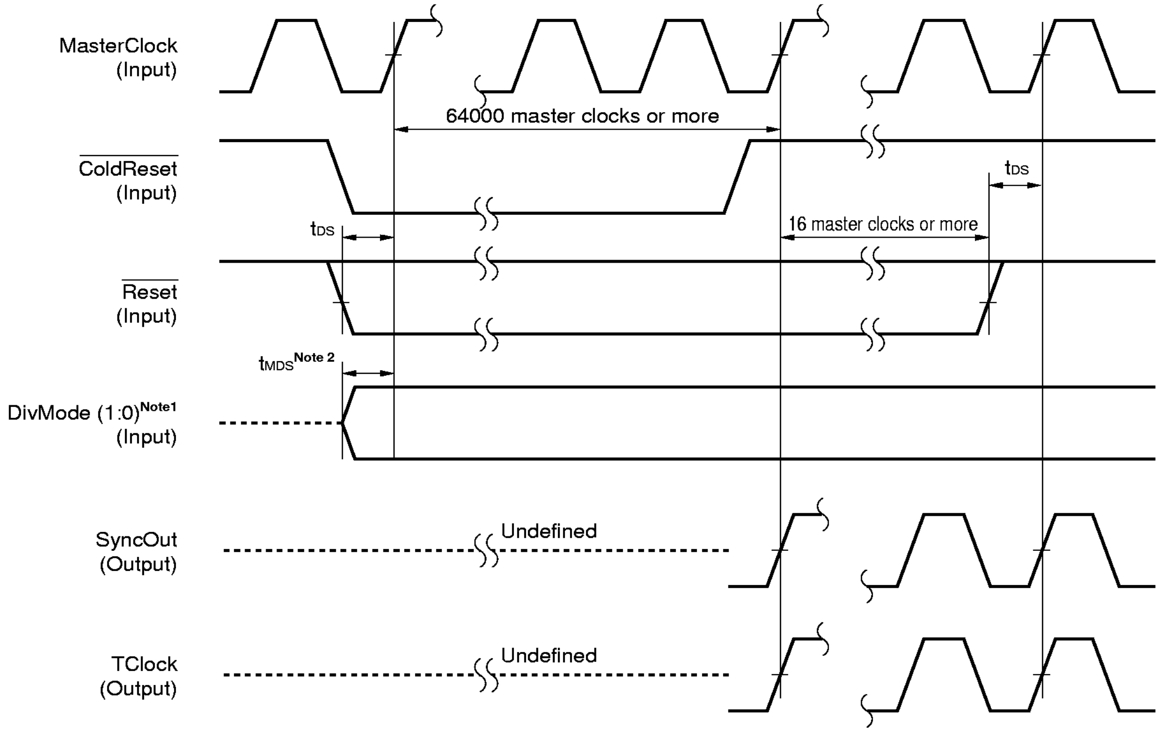
System interface edge timing



Clocking relations



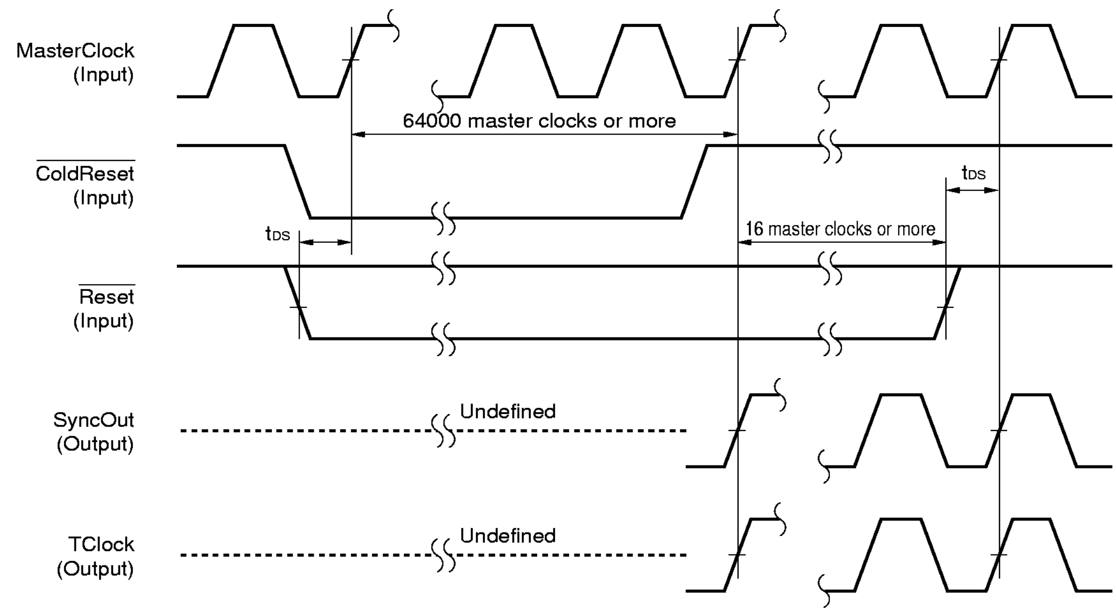
Power-on reset timing



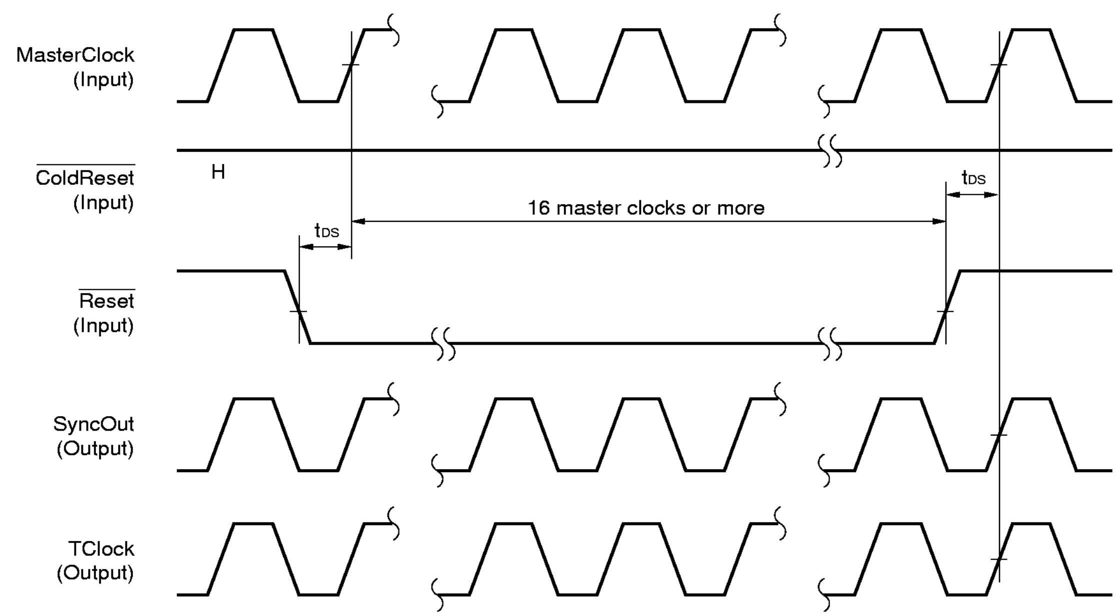
★ **Notes 1.** In the μPD30200-xxx. DivMode (2:0) in the μPD30210-xxx.

★ **2.** In the μPD30200-100 and 30200-133. t_{DS} in the μPD30200-80 and 30210-xxx.

Cold reset timing

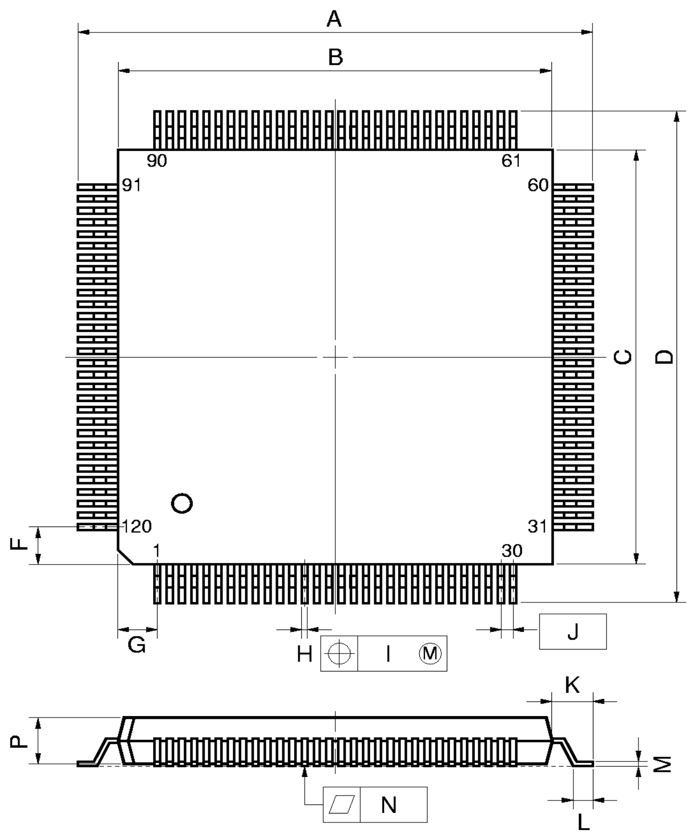


Software reset timing

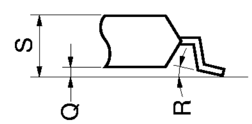


9. PACKAGE DRAWING

120 PIN PLASTIC QFP (□28)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	32.0±0.3	1.260±0.012
B	28.0±0.2	$1.102^{+0.009}_{-0.008}$
C	28.0±0.2	$1.102^{+0.009}_{-0.008}$
D	32.0±0.3	1.260±0.012
F	2.4	0.094
G	2.4	0.094
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	2.0±0.2	$0.079^{+0.009}_{-0.008}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.1	0.004
P	3.2	0.126
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.5 MAX.	0.138 MAX.

P120GD-80-LBB, MBB-1

10. RECOMMENDED SOLDERING CONDITIONS

Soldering this product under the following soldering conditions is recommended.

For the details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, consult NEC.

Table 10-1. Soldering Conditions of Surface Mount Type

★ **μPD30200GD-80-LBB : 120-pin plastic QFP (28 × 28 mm)**
μPD30200GD-100-MBB : 120-pin plastic QFP (28 × 28 mm)
μPD30200GD-133-MBB : 120-pin plastic QFP (28 × 28 mm)
★ **μPD30210GD-×××-MBB : 120-pin plastic QFP (28 × 28 mm)**

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 2 MAX., Number of days: 7[Note] (After that, prebaking is necessary at 125 °C for 36 hours.) **<Precaution>** Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	IR35-367-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX, (200 °C MIN.), Number of times: 2 MAX., Number of days: 7[Note] (After that, prebaking is necessary at 125 °C for 36 hours.) **<Precaution>** Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	VP15-367-2
Wave soldering	Solder bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1, Preheating temperature: 120 °C MAX. (Package surface), Number of days: 7[Note] (After that, prebaking is necessary at 125 °C for 36 hours)	WS60-367-1
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (Per side of device)	–

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65 % RH MAX.

Caution Do not use two or more soldering methods in combination (except the partial heating method).

★ APPENDIX DIFFERENCES BETWEEN THE VR4300, VR4305, VR4310 AND VR4100™

Parameter		VR4300	VR4305	VR4310	VR4100
System bus	Write data transfer	Two buses (DD×/D××)			Four buses (D/D×/D××/D×××)
	Initial value setting pins at reset time	DivMode (1:0) (Can be set on power application only)		DivMode (2:0) (Can be set on power application only)	BigEndian, $\overline{\text{Div2}}$, HizParity
	Block write access	Sequential ordering			Subblock ordering
	State after final data write	Final data retained in transfer rate setting			End of access
	Non-cache high-speed write	Provided			Provided (Set with a register)
CPU	Corresponding instructions	MIPS I, II, and III instruction sets			MIPS I, II, III instruction sets plus sum-of-products arithmetic
Cache memory	Data protection	None			Word parity (instructions); byte parity (data)
JTAG interface		Provided			None
SyncOut-SyncIn path		Provided			None
Clock interface	Input vs. internal multiplication rate	1.5[Note 1], 2, 3, 4[Note 2]	1, 2, 3	1.5, 2, 2.5[Note 3], 3, 4, 5[Note 4], 6[Note 4]	4
	Internal vs. bus frequency division rate	1.5[Note 1], 2, 3, 4[Note 2]	1, 2, 3	1.5, 2, 2.5[Note 3], 3, 4, 5[Note 4], 6[Note 4]	1, 2
Power mode	Low-power mode	Pipeline/system bus operated at a quarter of the normal rate			None
	Wait mode	None			Three types
PRId register		Imp = 0x0B			Imp = 0x0C

Notes
1. The 1.5 times frequency setting is allowed with the 100 MHz model only. (With the 133 MHz model, this setting is reserved.)
2. The 4 times frequency setting is allowed with the 133 MHz model only. (With the 100 MHz model, this setting is reserved.)
3. The 2.5 times frequency setting is allowed with the 167 MHz model only. (With the 100 MHz and 133 MHz models, this setting is reserved.)
4. The 5 or 6 times frequency setting is allowed with the 133 MHz and 167 MHz models only. (With the 100 MHz model, this setting is reserved.)