NEC

MOS INTEGRATED CIRCUIT

μPD75104, 75106, 75108

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μPD75108 is a 4-bit single-chip microcomputer integrating timer/event counters, serial interface, and vector interrupt function, in addition to a CPU, ROM, RAM, and I/O ports, on a single chip. Operating at high speeds, the microcomputer allows data to be manipulated in units of 1, 4, or 8 bits. In addition, various bit manipulation instructions are provided to reinforce I/O manipulation capability. Equipped with I/Os for interfacing with peripheral circuits operating on a different supply voltage, outputs that can directly drive LEDs, and analog inputs, μPD75108 is suitable for controlling such systems as VTRs, acoustic products, button telephones, radio communications equipment, and printers. A pin-compatible EPROM model is also available for evaluation of system development and small-scale production of application systems.

Detailed functions are described in the following user's manual. Be sure to read it for designing.
μPD751XX Series User's Manual: IEM-922

FEATURES

- Internal memory
  - Program memory (ROM)
    : 8068 × 8 bits (μPD75108)
    : 6016 × 8 bits (μPD75106)
    : 4096 × 8 bits (μPD75104)
  - Data memory (RAM)
    : 512 × 4 bits (μPD75108)
    : 320 × 4 bits (μPD75106, 75104)
- New architecture "75X series" rivaling 8-bit microcomputers
- 43 systematically organized instructions
  - A wealth of bit manipulation instructions
  - 8-bit data transfer, compare, operation, increment, and decrement instructions
  - 1-byte relative branch instructions
  - GETI instruction executing 2-/3-byte instruction with one byte
- High speed. Minimum instruction execution time: 0.95 μs (at 4.19 MHz), 5 V
- Power-saving, instruction time change function: 0.95 μs/1.91 μs/15.3 μs (at 4.19 MHz)
- I/O port pins as many as 58
- Three channels of 8-bit timers
- 8-bit serial interface
- Multiplexed vector interrupt function
- Model with PROM is available: μPD75P108B (One-time PROM, EPROM)

Unless there are differences among μPD75104, 75106, and 75108 functions, μPD75108 is treated as the representative model throughout this manual.

The information in this document is subject to change without notice.

Document No. IC-2520B
(O. D. No. IC-6906B)
Date Published January 1994 P
Printed in Japan

The mark ★ shows major revised points.

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ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75104CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75104GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75106CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75106GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75108CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75108GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Remarks: xxx is ROM code number.

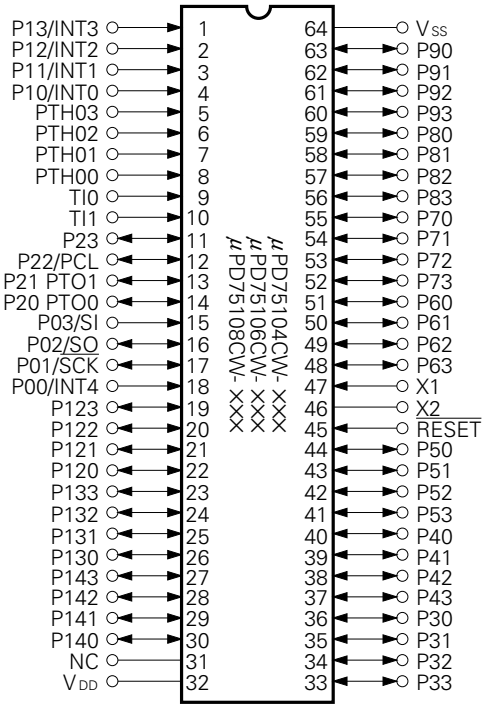
Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

FUNCTIONAL OUTLINE

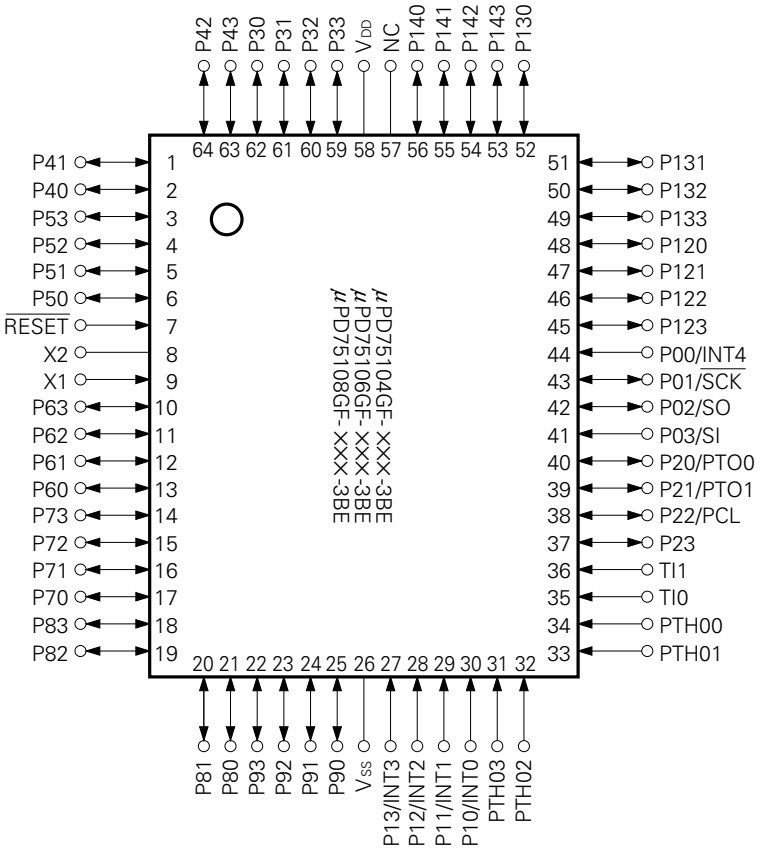
Item		Specifications
Number of Basic Instructions		43
Minimum Instruction Execution Time		Changeable in three steps: 0.95 μs, 1.91 μs, and 15.3 μs at 4.19 MHz
Internal Memory	ROM	8064 × 8 bits (μPD75108), 6016 × 8 bits (μPD75106), 4096 × 8 bits (μPD75104)
	RAM	512 × 4 bits (μPD75108), 320 × 4 bits (μPD75106, 75104)
General-Purpose Register		4 bits × 8 × 4 banks (memory mapped)
Accumulator		Three accumulators selectable according to the bit length of manipulated data: • 1-bit accumulator (CY), 4-bit accumulator (A), and 8-bit accumulator (XA)
I/O Port		58 port pins • CMOS input pins: 10 • CMOS I/O pins (can directly drive LEDs): 32 • Medium voltage N-ch open-drain I/O pins: 12 (can directly drive LEDs. Pull-up resistor can be connected to each bit) • Comparator input pins (4-bit accuracy): 4
Timer/Counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (can be used as watchdog timer)
Serial Interface		• 8 bits • LSB first/MSB first mode selectable • Two transfer modes (transfer/reception and reception only modes)
Vector Interrupt		External: 3, Internal: 4
Test Input		External: 2
Standby		• STOP and HALT modes
Instruction Set		• Various bit manipulation instructions (set, reset, test, Boolean operation) • 8-bit data transfer, compare, operation, increment, and decrement • 1-byte relative branch instructions • GETI instruction constituting 2 or 3-byte instruction with 1 byte
Others		• Power-ON reset circuit (mask option) • Bit manipulation memory (bit sequential buffer: 16 bits)
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)

1. PIN CONFIGURATION (Top View)

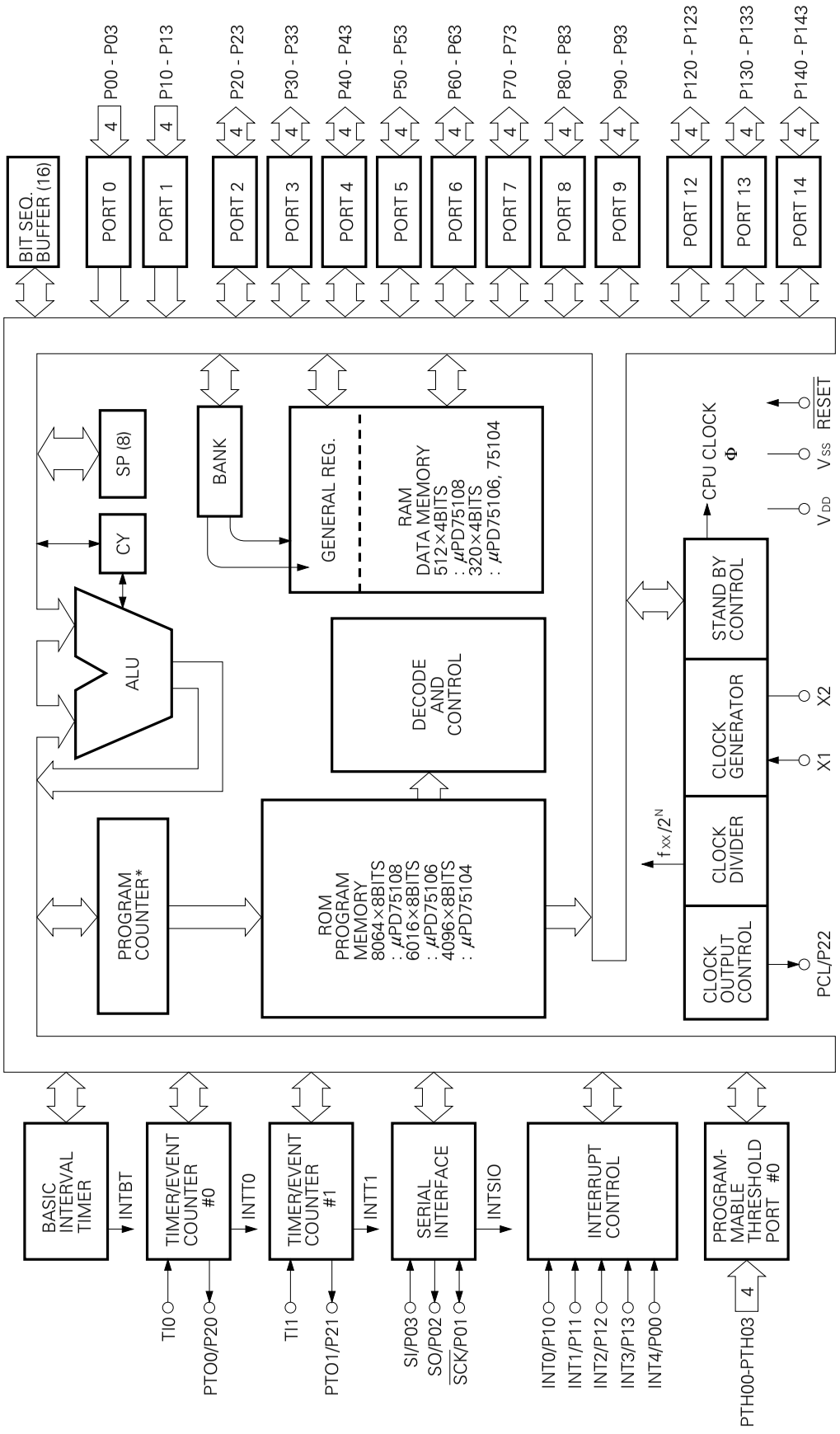
• 64-Pin Plastic Shrink DIP (750 mil)



• 64-Pin Plastic QFP (14 × 20 mm)



2. BLOCK DIAGRAM



*: 13 bits: μPD75106, 75108
12 bits: μPD75104

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	I/O	Shared with:	Function	8-Bit I/O	At Reset	I/O Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT 0)	x	Input	B
P01	I/O	$\overline{SCK}$				F
P02	I/O	SO				E
P03	Input	SI				B
P10	Input	INT0	4-bit input port (PORT 1)		Input	B
P11		INT1				
P12		INT2				
P13		INT3				
P20*3	I/O	PTO0	4-bit I/O port (PORT 2)	x	Input	E
P21*3		PTO1				
P22*3		PCL				
P23*3		—				
P30-P33*3	I/O	—	4-bit programmable I/O port (PORT 3) Can be specified for input or output bitwise.		Input	E
P40-P43*3	I/O	—	4-bit I/O port (PORT 4)	o	Input	E
P50-P53*3	I/O	—	4-bit I/O port (PORT 5)		Input	E
P60-P63*3	I/O	—	4-bit programmable I/O port (PORT 6) Can be specified for input or output bitwise.	o	Input	E
P70-P73*3	I/O		4-bit I/O port (PORT 7)		Input	E
P80-P83*3	I/O	—	4-bit I/O port (PORT 8)	o	Input	E
P90-P93*3	I/O	—	4-bit I/O port (PORT 9)		Input	E
P120-P123*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 12) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V	o	Input*2	M
P130-P133*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 13) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V		Input*2	M
P140-P143*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 14) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V	–	Input*2	M

*1: Circles indicate Schmitt trigger input pins.
2: With drain open: high impedance
With pull-up resistor connected: high level
3: Can directly drive LEDs.

3.2 PINS OTHER THAN PORTS

Pin Name	I/O	Shared with:	Function	At Reset	I/O Circuit TYPE*1
PTH00-PTH03	Input	—	4-bit variable threshold voltage analog input port	—	N
TI0 TI1	Input	—	External event pulse inputs for timer/event counter. Also serves as edge-detected vector interrupt input. 1-bit input also possible.	—	B
PTO0	I/O	P20	Outputs for timer/event counter	Input	E
PTO1		P21			
$\overline{SCK}$	I/O	P01	Serial clock I/O	Input	F
SO	I/O	P02	Serial data output	Input	E
SI	Input	P03	Serial data input	Input	B
INT4	Input	P00	Edge-detected vectored interrupt input (both rising and falling edges detected)	Input	B
INT0	Input	P10	Edge-detected vectored interrupt inputs (valid edge selectable)	Input	B
INT1		P11			
INT2	Input	P12	Edge-detected testable inputs (rising edge detected)	Input	B
INT3		P13			
PCL	I/O	P22	Clock output	Input	E
X1, X2	—	—	Crystal/ceramic system clock oscillator connections. Input external clock to X1, and signal in reverse phase with X1 to X2.	—	—
$\overline{RESET}$	Input	—	System reset input (low level active type)	—	B
NC*2	—	—	No Connection	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	GND	—	—

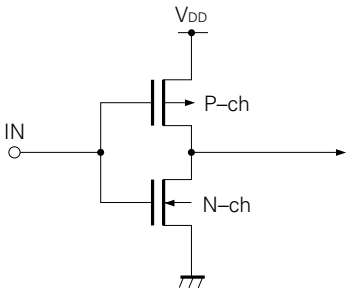
*1: Circles indicate Schmitt trigger input pins.

2: Connect the NC pin directly to the V_{DD} pin when μPD75P108B and a printed circuit board are shared.

3.3 PIN INPUT/OUTPUT CIRCUITS

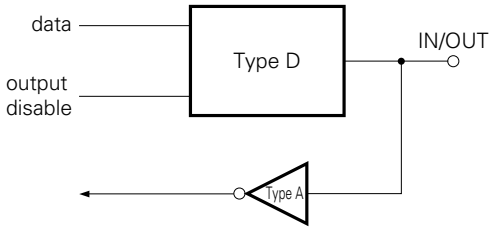
The following shows a simplified input/output circuit diagram for each pin of the μPD75108.

TYPE A



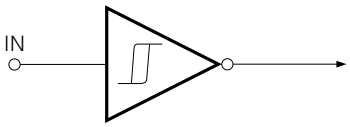
Input buffer of CMOS standard

TYPE E



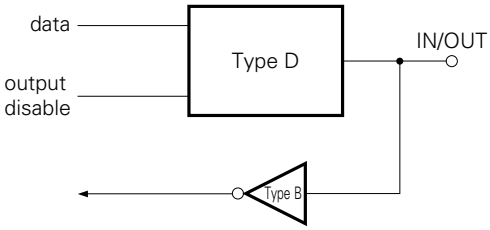
I/O circuit consisting of Type D push-pull output circuit and Type A input buffer

TYPE B



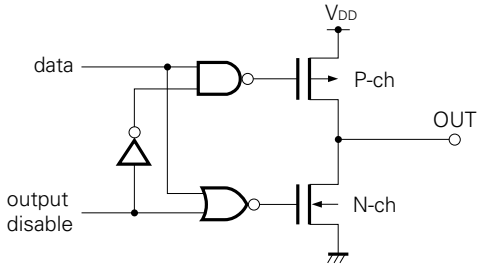
Schmitt trigger input with hysteresis characteristics

TYPE F



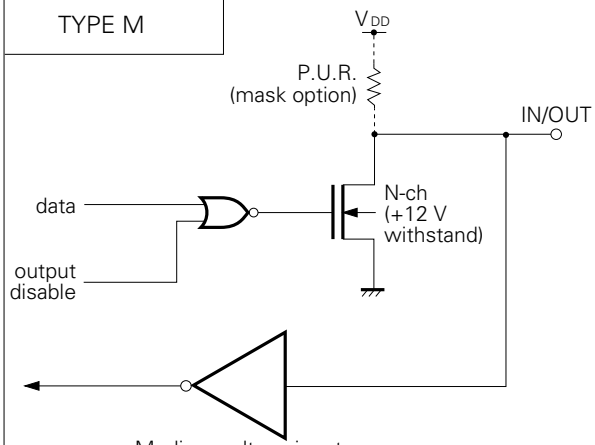
I/O circuit consisting of Type D push-pull output and Type B Schmitt trigger input

TYPE D



Push – pull output that can be set in a output high– impedance state (both P–ch and N–ch are off)

TYPE M



Medium-voltage input buffer (+12 V withstand)
P.U.R.: Pull-Up Resistor

12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 12, 13, 14		-0.3 to V_{DD}+0.3	V
	V_{I2}*1	Ports 12 to 14	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +13	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL}*2	1 pin	Peak	30	mA
			rms	15	mA
		Total of ports 0, 2 to 4, 12 to 14	Peak	100	mA
			rms	60	mA
		Total of ports 5 to 9	Peak	100	mA
			rms	60	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

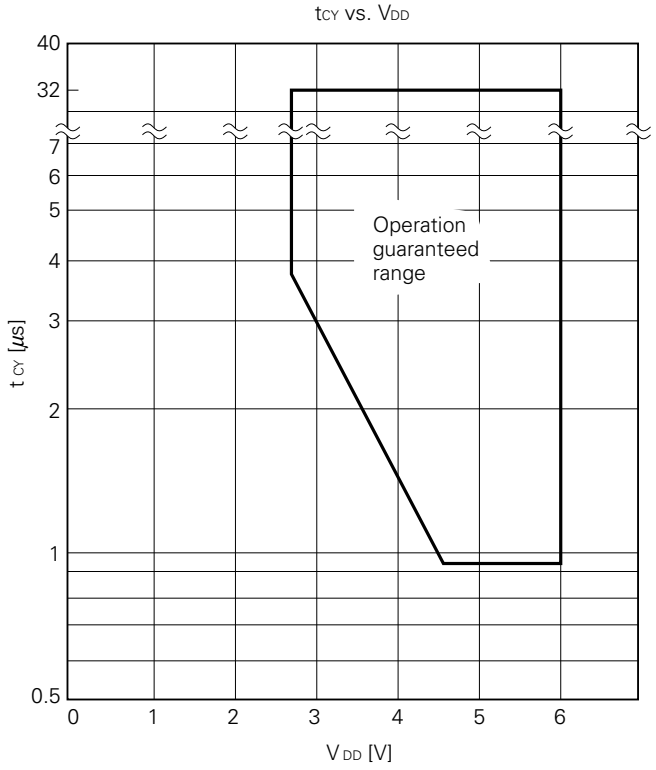
*1: The power supply impedance (pull-up resistance) must be 50 kΩ or higher when a voltage higher than 10 V is applied to ports 12, 13, and 14.

2: rms = Peak value x $\sqrt{\text{Duty}}$

AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time* (Minimum Instruction Execution Time = 1 Machine Cycle)	t_{CY}	V_{DD} = 4.5 to 6.0 V		0.95		32	μs
				3.8		32	μs
TI0, TI1 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 Input High-/Low-Level Width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ High-/Low-Level Width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V	Input	0.4			μs
			Output	t_{KCY}/2-50			ns
			Input	1.6			μs
			Output	t_{KCY}/2-150			ns
SI Setup Time (vs. $\overline{SCK}$↑)	t_{SIK}			100			ns
SI Hold Time (vs. $\overline{SCK}$↑)	t_{KSI}			400			ns
$\overline{SCK}$ ↓→ SO Output delay Time	t_{KSO}	V_{DD} = 4.5 to 6.0 V				300	ns
						1000	ns
INT0 to 4 High-/Low-Level Width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			5			μs

*: The cycle time of the CPU clock (Φ) is determined by the input frequency of the ceramic or crystal oscillator circuit and the set value of the processor clock control register. The t_{CY} vs. V_{DD} characteristics are as shown on the right.



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt request		*3		ms

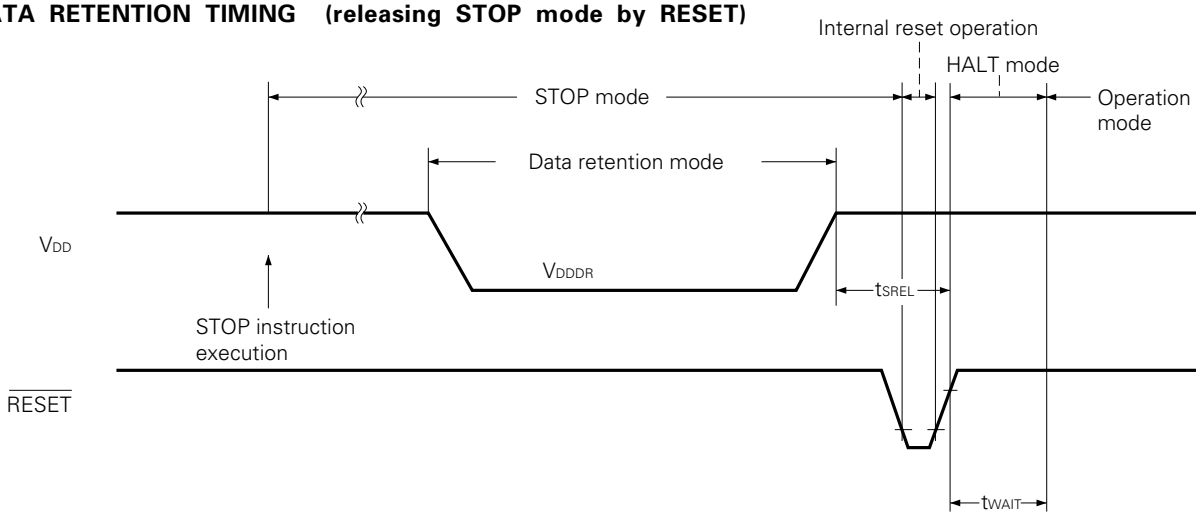
*1: The current flowing through internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

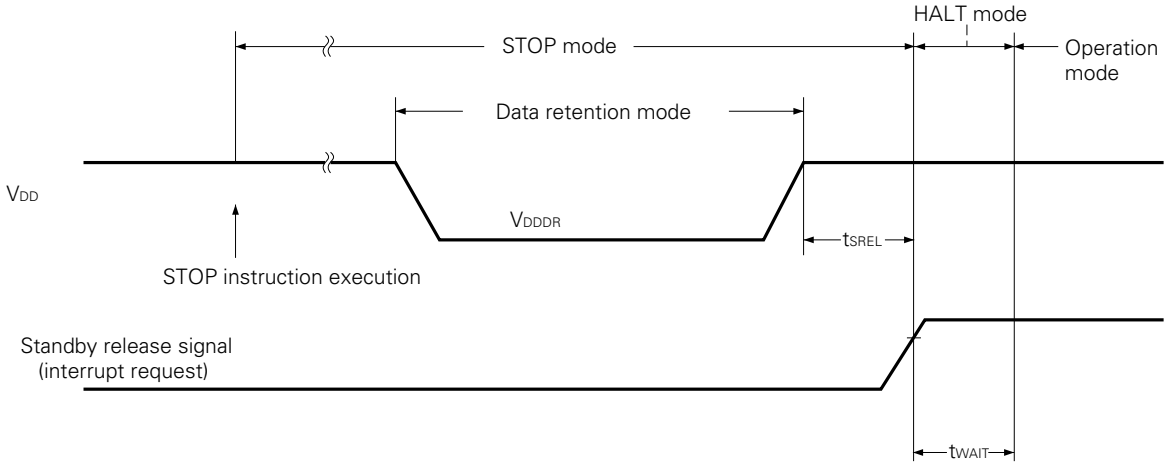
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	Wait time ( ): f_{XX} = 4.19 MHz
–	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)

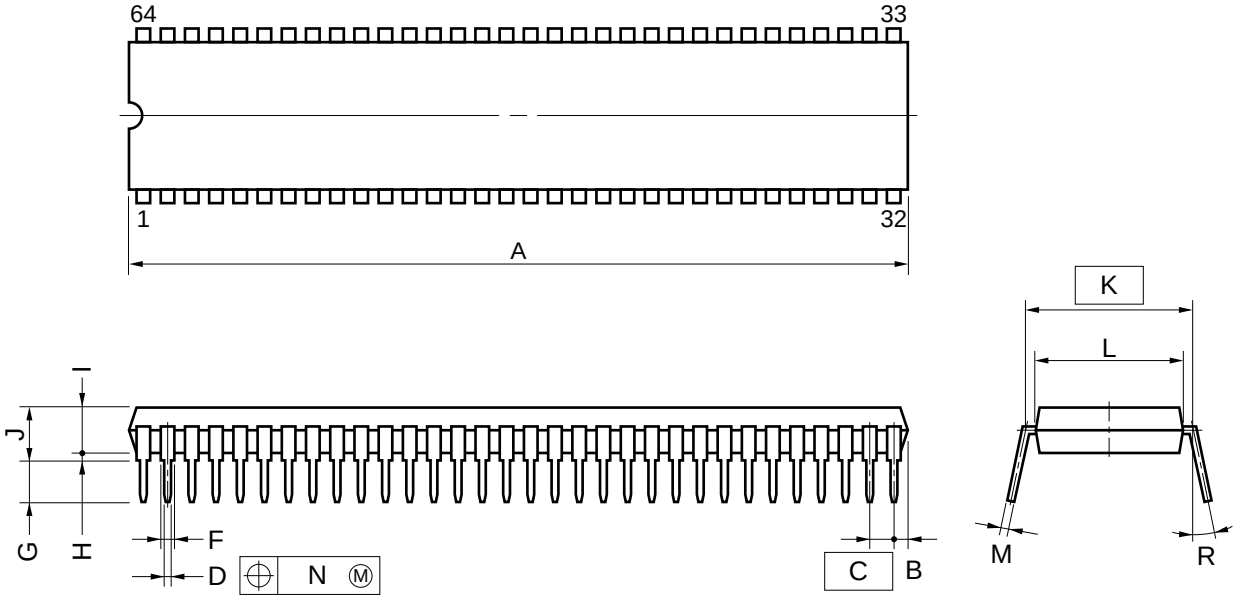


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



14. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



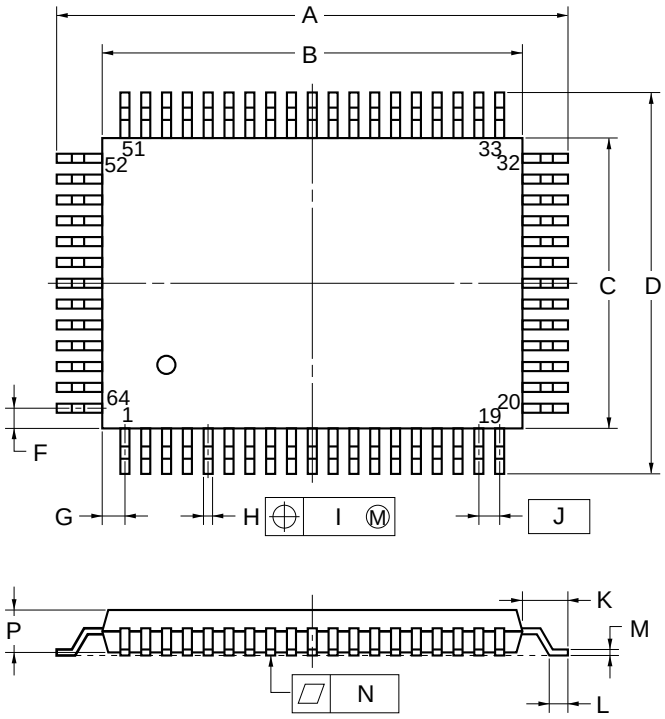
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

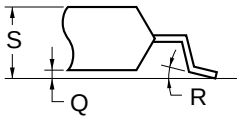
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



detail of lead end



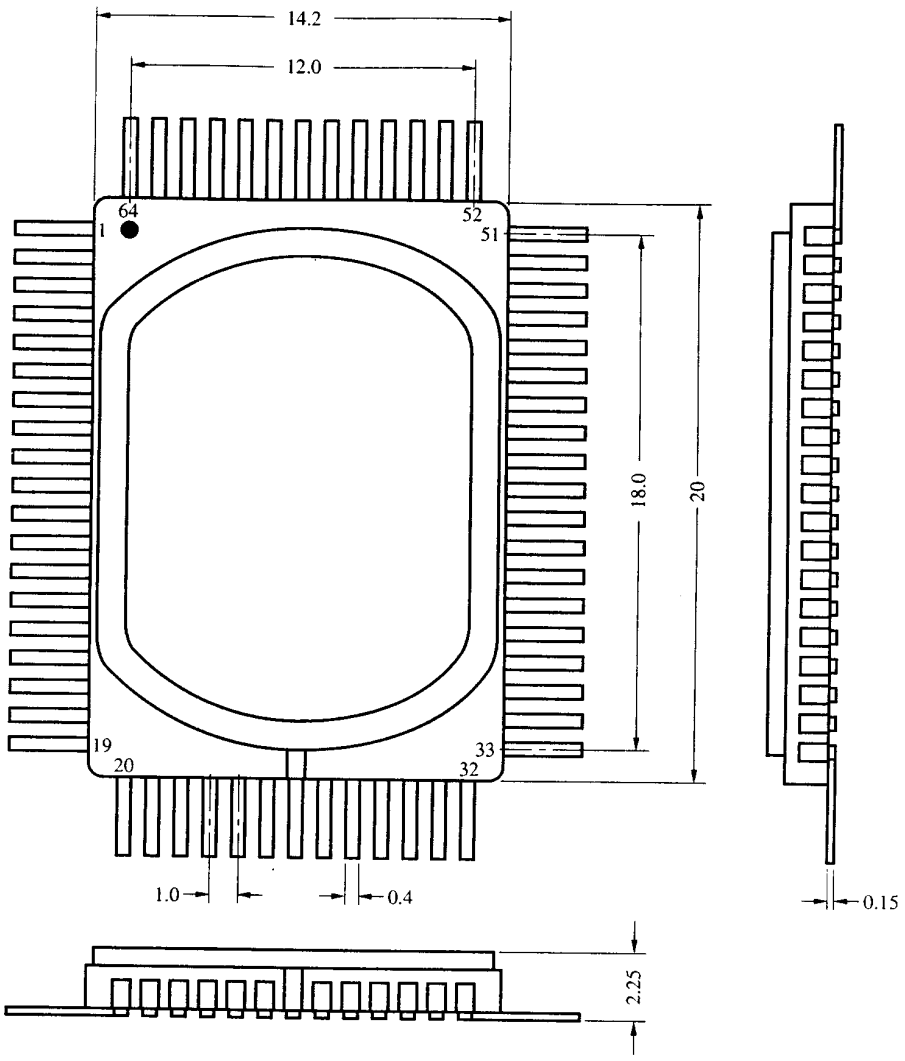
NOTE

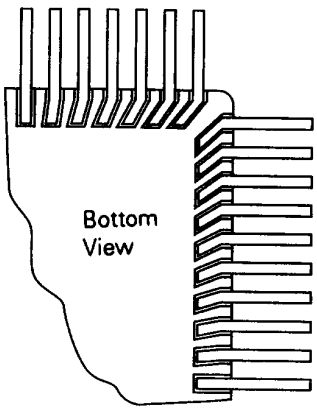
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

ES 64-Pin Ceramic QFP (Reference) (unit in mm)





Note 1. The metal cap is connected to pin 26, at the Vss (GND) level.

2. The leads are molded diagonally at the bottom.
3. The lead lengths are not specified, as the lead cutting process is not controlled.