

## DARLINGTON COPLEMENTARY SILICON POWER TRANSISTORS

...designed for general-purpose amplifier and low-speed switching applications

### FEATURES:

\* Collector-Emitter Sustaining Voltage-

$$V_{CEO(SUS)} = 60 \text{ V (Min) - 2N6040, 2N6043}$$

$$= 80 \text{ V (Min) - 2N6041, 2N6044}$$

$$= 100 \text{ V (Min) - 2N6042, 2N6045}$$

\* Collector-Emitter Saturation Voltage

$$V_{CE(sat)} = 2.0 \text{ V (Max.) @ } I_C = 4.0 \text{ A - 2N6040, 41, 2N6043, 44}$$

$$= 2.0 \text{ V (Max.) @ } I_C = 4.0 \text{ A - 2N6042, 2N6045}$$

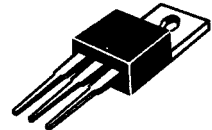
\* Monolithic Construction with Built-in Base-Emitter Shunt Resistor

PNP	NPN
2N6040	2N6043
2N6041	2N6044
2N6042	2N6045

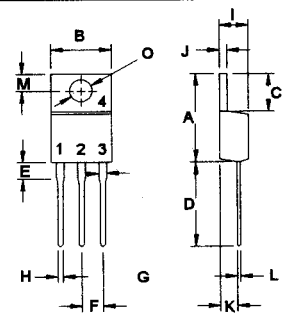
10 AMPERE  
DARLINGTON  
COMPLEMENTARY SILICON  
POWER TRANSISTORS  
60-100 VOLTS  
80 WATTS

### MAXIMUM RATINGS

Characteristic	Symbol	2N6040	2N6041	2N6042	Unit
		2N6043	2N6044	2N6045	
Collector-Emitter Voltage	$V_{CEO}$	60	80	100	V
Collector-Base Voltage	$V_{CBO}$	60	80	100	V
Emitter-Base Voltage	$V_{EBO}$	5.0			V
Collector Current-Continuous -Peak	$I_C$	8.0			A
	$I_{CM}$	16			
Base Current	$I_B$	120			mA
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75			W
		0.6			
Operating and Storage Junction Temperature Range	$T_J, T_{STG}$	- 65 to +150			$^\circ\text{C}$



TO-220



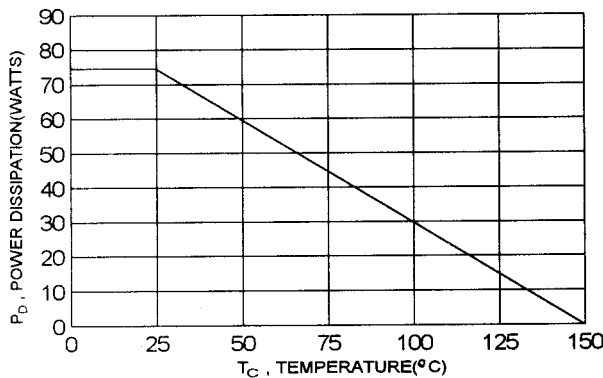
PIN 1.BASE  
2.COLLECTOR  
3.EMITTER  
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	1.67	$^\circ\text{C}/\text{W}$

FIGURE -1 POWER DERATING



**2N6040, 2N6041, 2N6042 PNP / 2N6043, 2N6044, 2N6045 NPN**

**ELECTRICAL CHARACTERISTICS (  $T_c = 25^\circ\text{C}$  unless otherwise noted )**

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector - Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ ) 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	$V_{CE(sus)}$	60 80 100		V
Collector Cutoff Current ( $V_{CE} = 30\text{ V}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ V}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ ) 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	$I_{CEO}$		0.5 0.5 0.5	mA
Collector Cutoff Current ( $V_{CB} = 60\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ V}$ , $I_E = 0$ ) 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	$I_{CBO}$		0.5 0.5 0.5	mA
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$		2.0	mA

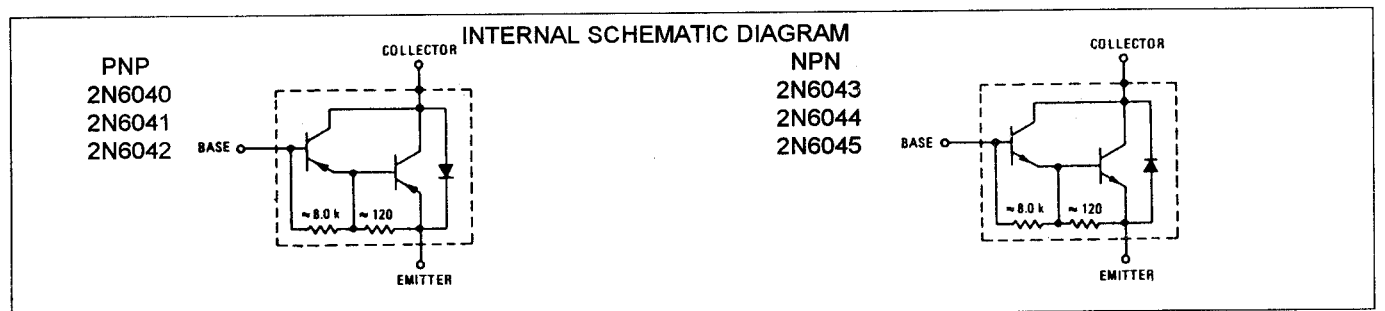
**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 3.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 8.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) 2N6040, 41/ 2N6043, 44 2N6042, 2N6045 All Types	hFE	1000 1000 100	20000 20000	
Collector-Emitter Saturation Voltage ( $I_C = 4.0\text{ A}$ , $I_B = 16\text{ mA}$ ) ( $I_C = 3.0\text{ A}$ , $I_B = 12\text{ mA}$ ) ( $I_C = 8.0\text{ A}$ , $I_B = 80\text{ mA}$ ) 2N6040, 41/ 2N6043, 44 2N6042, 2N6045 All Types	$V_{CE(sat)}$		2.0 2.0 4.0	V
Base-Emitter Saturation Voltage ( $I_C = 8.0\text{ A}$ , $I_B = 80\text{ mA}$ )	$V_{BE(sat)}$		4.5	V
Base-Emitter On Voltage ( $I_C = 4.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ )	$V_{BE(on)}$		2.8	V

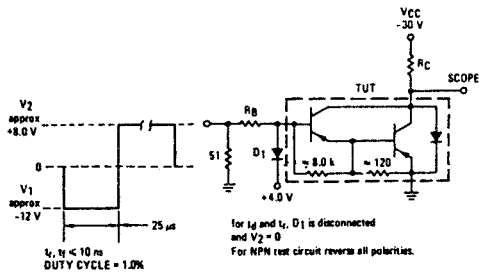
**DYNAMIC CHARACTERISTICS**

Output Capacitance ( $V_{CB} = 10\text{ V}$ , $I_E = 1.0\text{ A}$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$		300	pF
Small-Signal Current Gain ( $I_C = 3.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ , $f = 1.0\text{ KHz}$ )	$h_{fe}$	300		

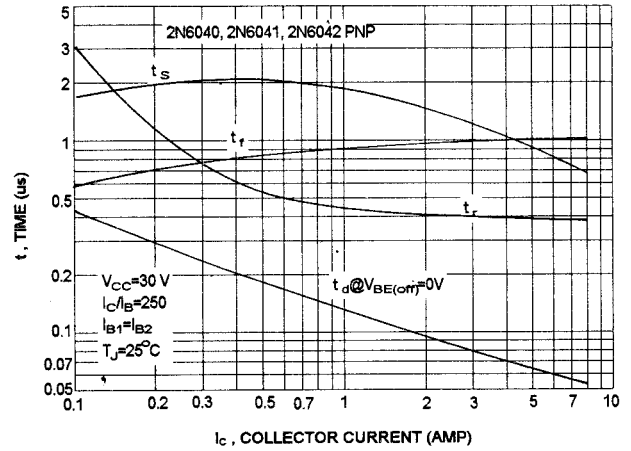
(1) Pulse Test: Pulse width = 300 us , Duty Cycle  $\leq 2.0\%$



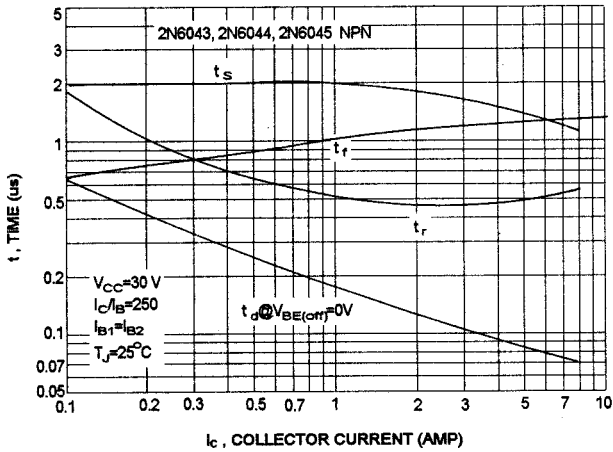
SWITCHING TIMES TEST CIRCUIT



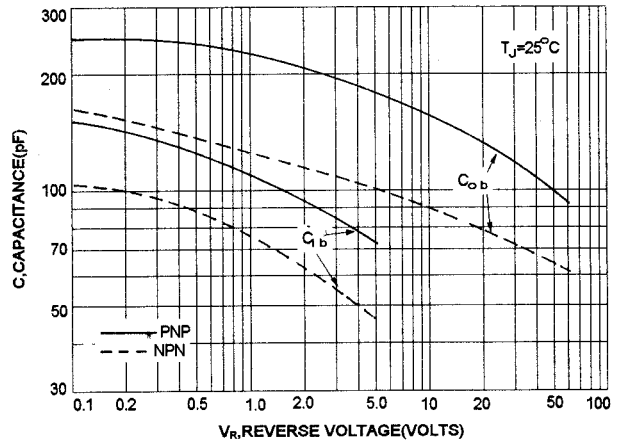
SWITCHING TIMES



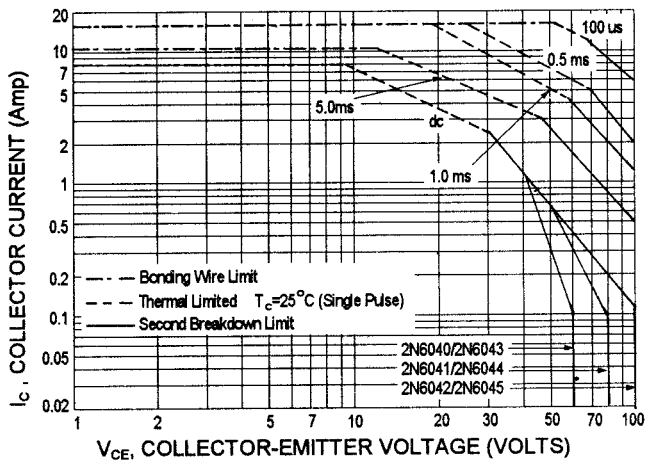
SWITCHING TIMES



CAPACITANCES



ACTIVE-REGION SAFE OPERATING AREA (SOA)

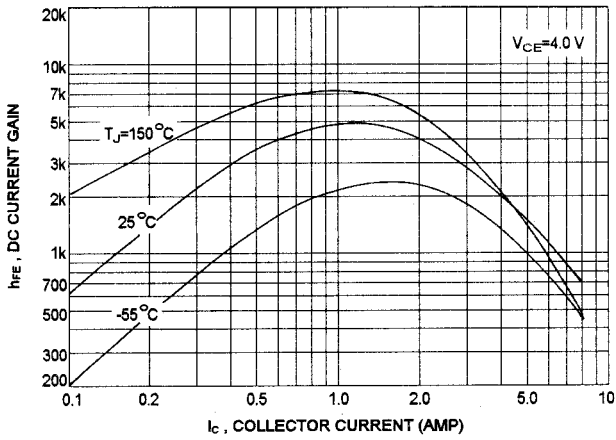


There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on  $T_{J(PK)}=150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(PK)} < 150^\circ\text{C}$ . At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

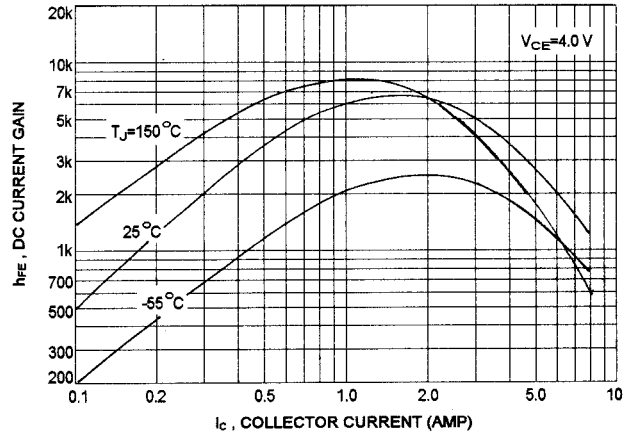
PNP 2N6040, 2N6041, 2N6042

DC CURRENT GAIN

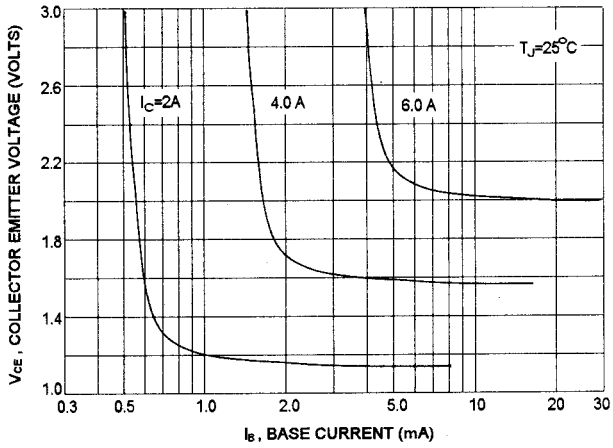


NPN 2N6043, 2N6044, 2N6045

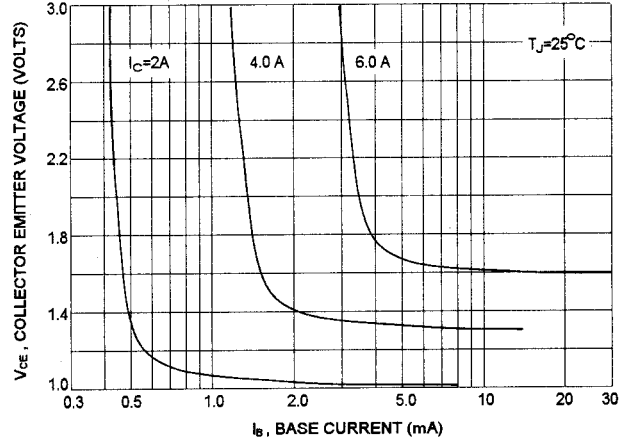
DC CURRENT GAIN



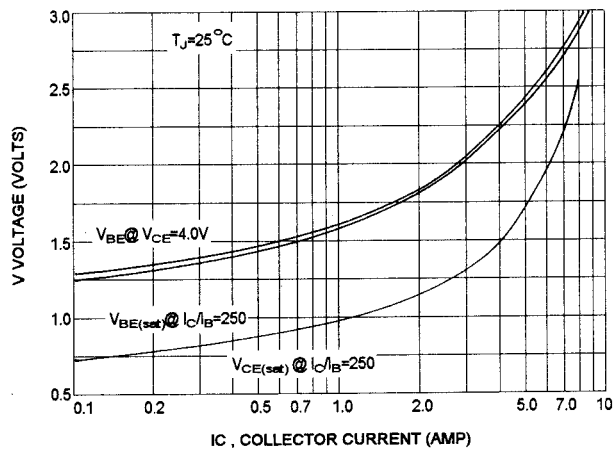
COLLECTOR SATURATION REGION



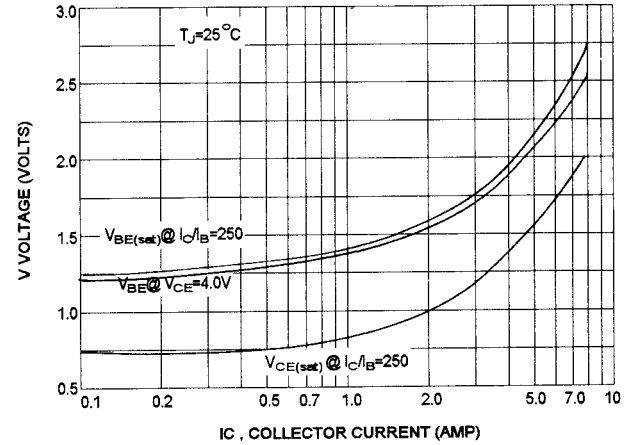
COLLECTOR SATURATION REGION



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