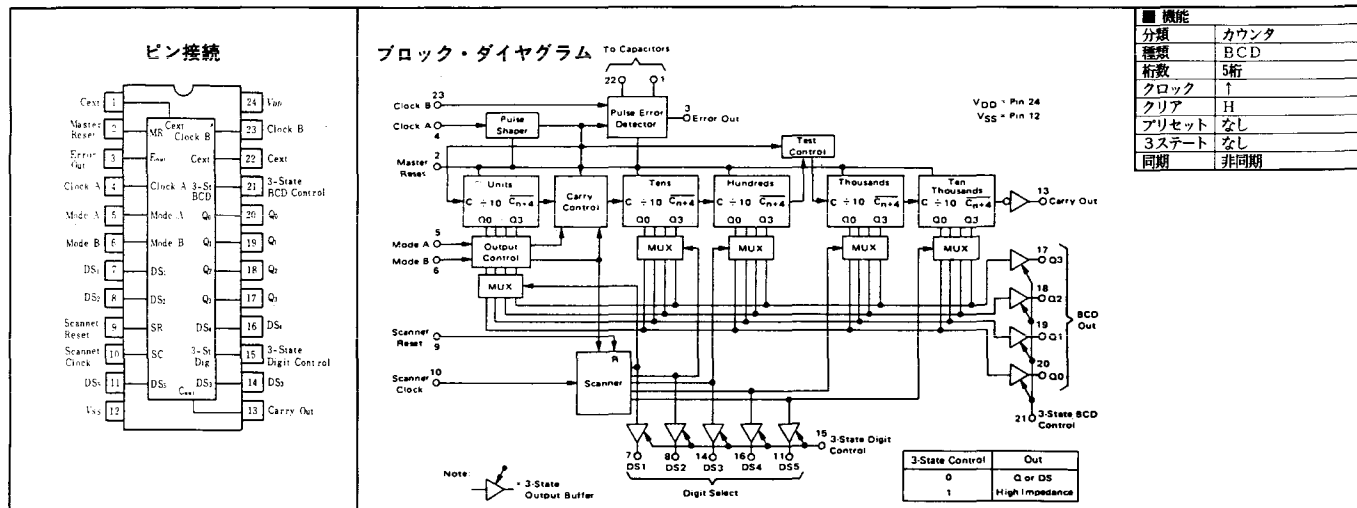


# 4534B 5 Cascaded BCD Counters



## 特徴

- 5桁の10リプル・カウンタからなるリアルタイム5分割カウンタ
- 各カウンタ出力は、内部のスキヤナにより時分割多重され、4個のBCDデータとして出力される。4種類のカウンタ・モードをもち、モード端子で選択可能

## 機能表

Mode A	Mode B	First Stage Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first stage	5-digit Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first stage	4-digit counter with - 10 and roundoff at front end.
1	0	Counts 3, 4, 5, 6, 7 = 5 Counts 8, 9, 0, 1, 2 = 0	At 7 to 8 transition of first stage	4-digit counter with 1/2 pence capability.

## スイッチング特性

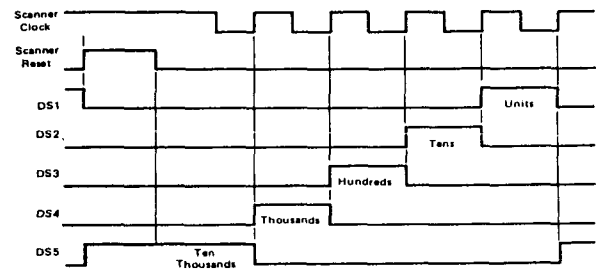
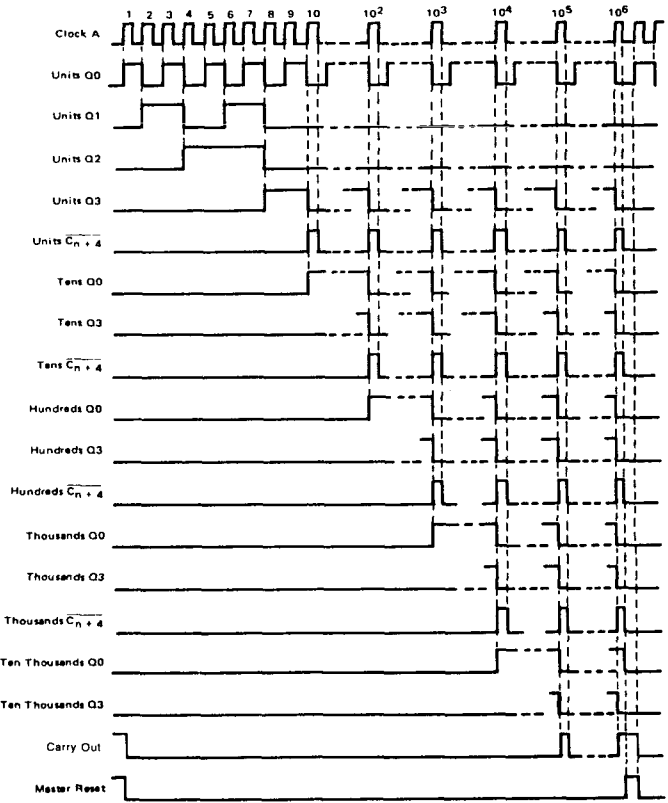
	V <sub>DD</sub>	typ		max	単位
		min	typ		
t <sub>r</sub>	5V	100	200		ns
	10V	50	100		ns
	15V	40	80		ns
t <sub>f</sub>	5V	100	200		ns
	10V	50	100		ns
	15V	40	80		ns
t <sub>PLH</sub> (CLK → Q)	5V	4.00	8.00		ns
	10V	1.50	3.00		ns
	15V	1.00	2.30		ns
t <sub>PHL</sub> (CLK → Q)	5V	4.00	8.00		ns
	10V	1.50	3.00		ns
	15V	1.00	2.30		ns
t <sub>PLH</sub> ( )	5V				ns
	10V				ns
	15V				ns
t <sub>PHL</sub> ( )	5V				ns
	10V				ns
	15V				ns
f <sub>CP</sub>	V <sub>DD</sub>	min	typ		単位
	5V	0.5	1.0		MHz
	10V	1.0	3.0		MHz
	15V	1.2	5.0		MHz

## メーカー別相当品

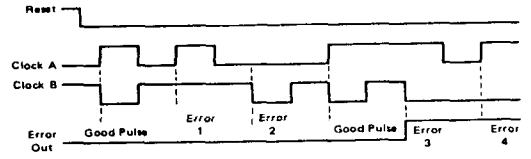
メーカー	型名	パッケージ	
		DIP	SOP
沖			
三洋			
JRC			
東芝			
日電			
日立	HD14534B	●	
富士通			
松下			
三菱			
ローム			
MOT	MC14534B	●	
NS			
RCA			
SGS			
SIG	HEF4534BP	●	●
SSS	SL4534B	●	

### 4534B 5 Cascaded BCD Counters

タイミング・チャート



Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages. DS5 is selected automatically when Scanner Reset goes high.



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.