

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4002B **gates** Dual 4-input NOR gate

Product specification
File under Integrated Circuits, IC04

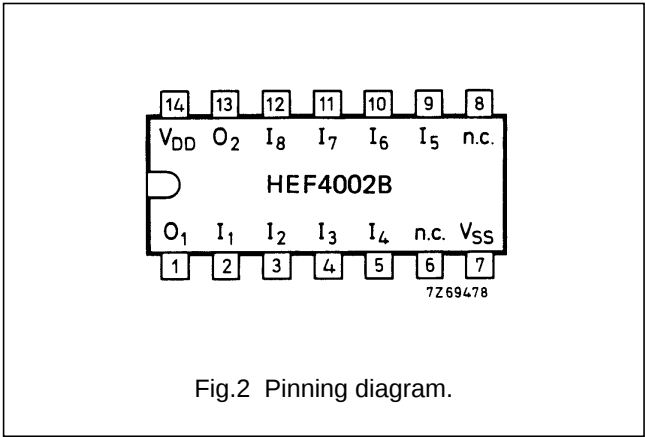
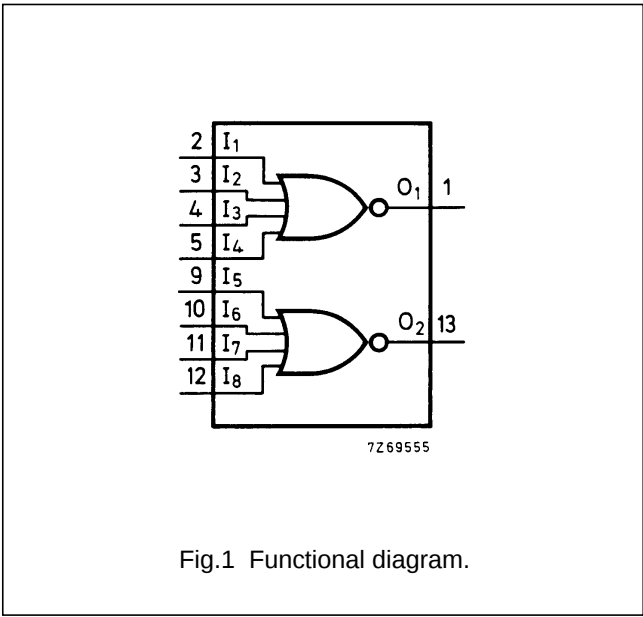
January 1995

Dual 4-input NOR gate

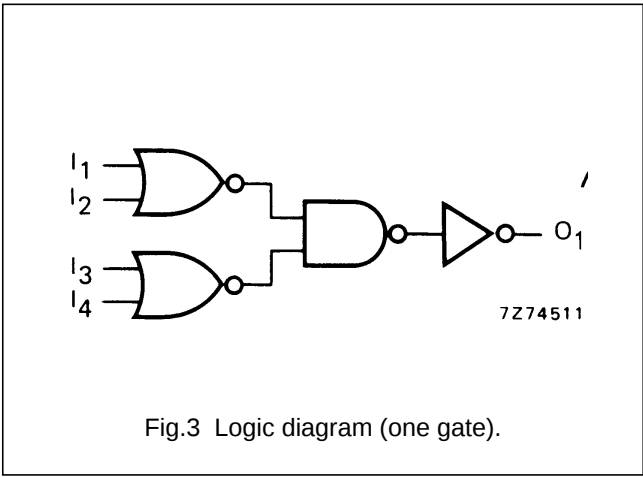
HEF4002B
gates

DESCRIPTION

The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4002BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4002BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4002BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

Dual 4-input NOR gate

HEF4002B
gates

AC CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V _{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays I _n → O _n	5	t _{PHL} ; t _{PLH}	60	120	ns	33 ns + (0,55 ns/pF) C _L
	10		25	50	ns	14 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1050 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4300 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$11\,700 f_i + \sum (f_o C_L) \times V_{DD}^2$	



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