

# 100354

## Low Power 8-Bit Register with Cut-Off Drivers

### General Description

The 100354 contains eight D-type edge triggered, master/slave flip-flops with individual inputs ( $D_n$ ), true outputs ( $Q_n$ ), a clock input (CP), an output enable pin ( $\overline{OEN}$ ), and a common clock enable pin ( $\overline{CEN}$ ). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the  $\overline{CEN}$  input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

A Q output follows its D input when the  $\overline{OEN}$  pin is LOW. A HIGH on  $\overline{OEN}$  holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is  $-2.0V$ , presenting a high impedance to the data bus. This high impedance

reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100354 outputs are designed to drive a doubly terminated  $50\Omega$  transmission line ( $25\Omega$  load impedance). All inputs have  $50\text{ k}\Omega$  pull-down resistors.

### Features

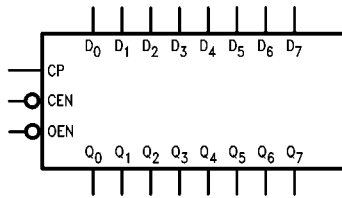
- Cut-off drivers
- Drives  $25\Omega$  load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range =  $-4.2V$  to  $-5.7V$
- Available to industrial grade temperature range

### Ordering Code:

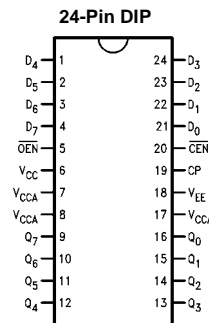
Order Number	Package Number	Package Description
100354PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100354QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100354QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range ( $-40^\circ\text{C}$ to $+85^\circ\text{C}$ )

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol

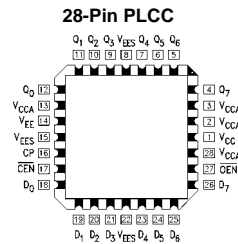


### Connection Diagrams



### Pin Descriptions

Pin Names	Description
$D_0$ - $D_7$	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
$\overline{OEN}$	Output Enable Input
$Q_0$ - $Q_7$	Data Outputs



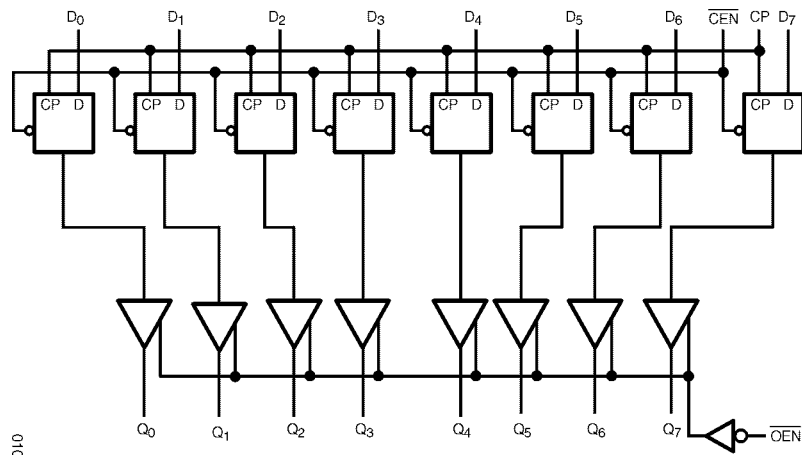
100354 Low Power 8-Bit Register with Cut-Off Drivers

**Truth Table**

Inputs				Outputs
D <sub>n</sub>	$\overline{\text{CEN}}$	CP	$\overline{\text{OEN}}$	Q <sub>n</sub>
L	L	↗	L	L
H	L	↗	L	H
X	X	L	L	NC
X	X	H	L	NC
X	H	X	L	NC
X	X	X	H	Cutoff

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 NC = No Change  
 X = Don't Care  
 Cutoff = Lower-than-LOW State  
 ↗ = LOW-to-HIGH Transition

**Logic Diagram**



81019010

**Absolute Maximum Ratings**(Note 1)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-100 mA
ESD (Note 2)	≥2000V

**Recommended Operating Conditions**

Case Temperature ( $T_C$ )	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage ( $V_{EE}$ )		-5.7V to -4.2V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Commercial Version****DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620		mV
$V_{OHC}$	Output HIGH Voltage	-1035			mV	
$V_{OLC}$	Output LOW Voltage			-1610		$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$
$V_{OLZ}$	Cutoff LOW Voltage			-1950	mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$
$I_{IH}$	Input HIGH Current			240	μA	$V_{IN} = V_{IH} (Max)$
$I_{EE}$	Power Supply Current	-202 -209		-105 -105	mA	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Commercial Version (Continued) DIP AC Electrical Characteristics

 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{MAX}$	Toggle Frequency	250		250		250		MHz	Figures 1, 4
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to Output	1.40	3.00	1.40	3.00	1.50	3.10	ns	Figures 1, 4 (Note 4)
$t_{PZH}$ $t_{PHZ}$	Propagation Delay $\overline{OEN}$ to Output	1.60	4.20	1.60	4.20	1.60	4.20	ns	Figures 3, 7 (Note 4)
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	Figures 1, 4
$t_S$	Setup Time $D_n$ $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	1.10 0.40 1.10		1.10 0.40 1.10		1.10 0.40 1.10		ns	Figures 2, 5
$t_H$	Hold Time $D_n$	0.10		0.10		0.10		ns	Figures 1, 6
$t_{PW(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 4

**Note 4:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## PLCC AC Electrical Characteristics

 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{MAX}$	Toggle Frequency	250		250		250		MHz	Figures 1, 4
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	Figures 1, 4 (Note 5)
$t_{PZH}$ $t_{PHZ}$	Propagation Delay $\overline{OEN}$ to Output	1.60	4.00	1.60	4.00	1.60	4.00	ns	Figures 3, 7 (Note 5)
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 4
$t_S$	Setup Time $D_n$ $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	1.00 0.30 1.00		1.00 0.30 1.00		1.00 0.30 1.00		ns	Figures 2, 5
$t_H$	Hold Time $D_n$	0.00		0.00		0.00		ns	Figures 1, 6
$t_{PW(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 4
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		280		280		280	ps	(Note 6)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		340		340		340	ps	(Note 6)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		340		340		340	ps	(Note 6)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		250		250		250	ps	(Note 6)

**Note 5:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

**Note 6:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW ( $t_{OSHL}$ ), or LOW-to-HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

## Industrial Version

### PLCC DC Electrical Characteristics (Note 7)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620			
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage		-1565		-1610			
$V_{OLZ}$	Cutoff LOW Voltage		-1900		-1950	mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	OEN = HIGH
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH}$ (Max)	
$I_{EE}$	Power Supply Current					mA	Inputs Open	
		-202 -209	-105 -105	-202 -209	-105 -105		$V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	

**Note 7:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{MAX}$	Toggle Frequency	250		250		250		MHz	Figures 1, 4
$t_{PLH}$	Propagation Delay	1.40	2.80	1.40	2.80	1.50	2.90	ns	Figures 1, 4 (Note 8)
$t_{PHL}$	CP to Output								
$t_{PZH}$	Propagation Delay	1.50	4.10	1.60	4.00	1.60	4.00	ns	Figures 3, 5 (Note 8)
$t_{PHZ}$	OEN to Output								
$t_{TLH}$	Transition Time	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 4
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time							ns	Figures 2, 5
	$\overline{D}_n$	1.00		1.00		1.00			
	$\overline{CEN}$ (Disable Time)	0.30		0.30		0.30			
	$\overline{CEN}$ (Release Time)	1.00		1.00		1.00			
$t_H$	Hold Time	$D_n$	0.00	0.00		0.00		ns	Figures 1, 6
$t_{PW(H)}$	Pulse Width High	CP	2.00	2.00		2.00		ns	Figures 1, 4

**Note 8:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Test Circuitry

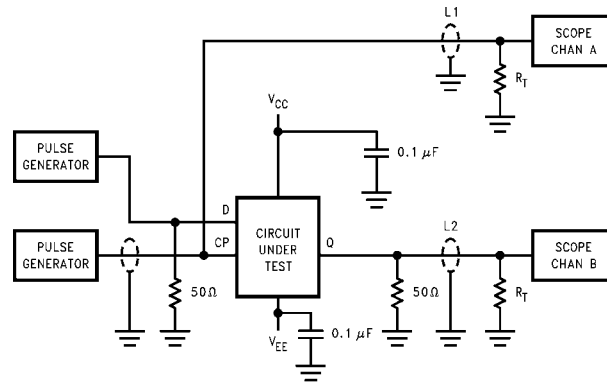


FIGURE 1. Toggle Frequency Test Circuit

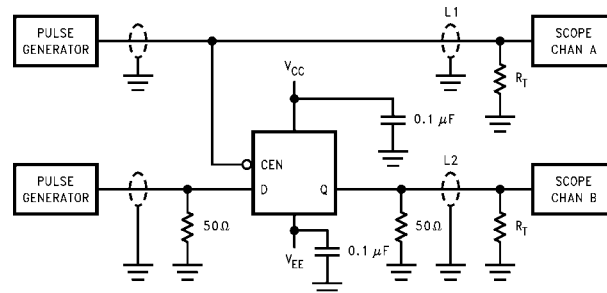


FIGURE 2. AC Test Circuit

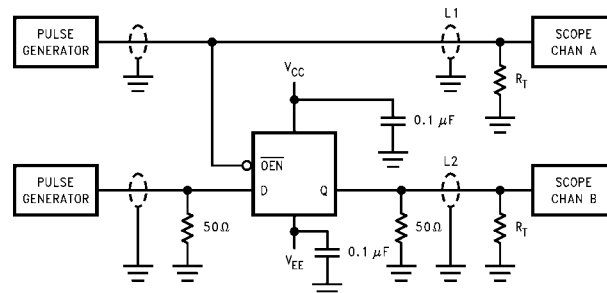


FIGURE 3. AC Test Circuit

**Notes:**

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

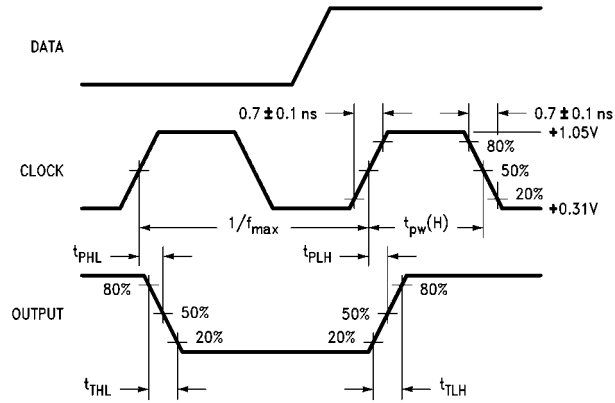
$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1 μF from GND to  $V_{CC}$  and  $V_{EE}$

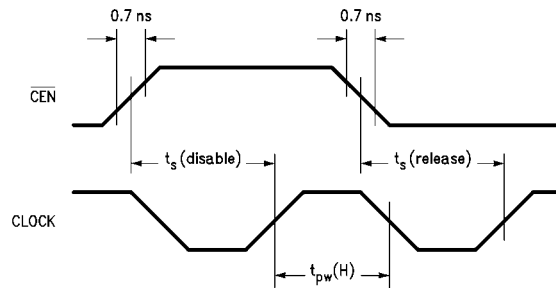
All unused outputs are loaded with 25Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

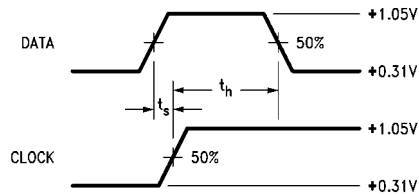
## Switching Waveforms



**FIGURE 4. Propagation Delay (Clock) and Transition Times**



**FIGURE 5. Setup and Pulse Width Times**

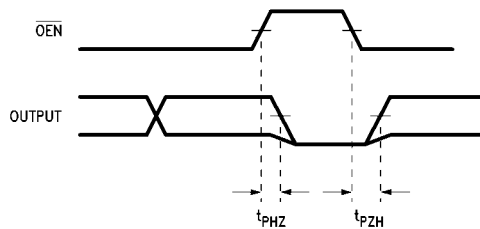


**Notes:**

$t_s$  is the minimum time before the transition of the clock that information must be present at the data input.

$t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

**FIGURE 6. Data Setup and Hold Time**



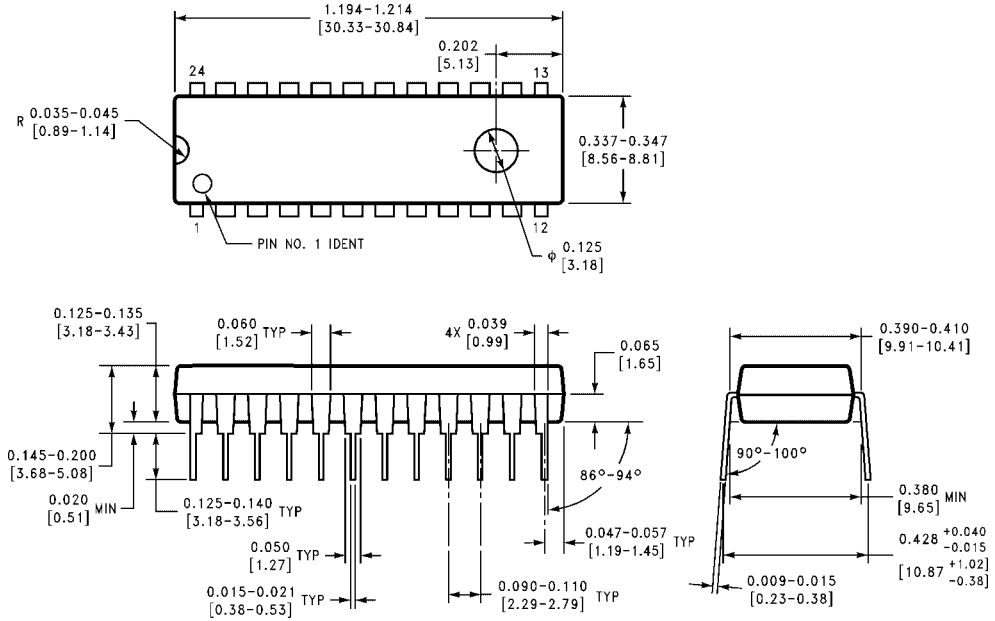
**Note:**

The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active  $V_{OL}$  and  $V_{OH}$ .

**FIGURE 7. Cutoff Times**

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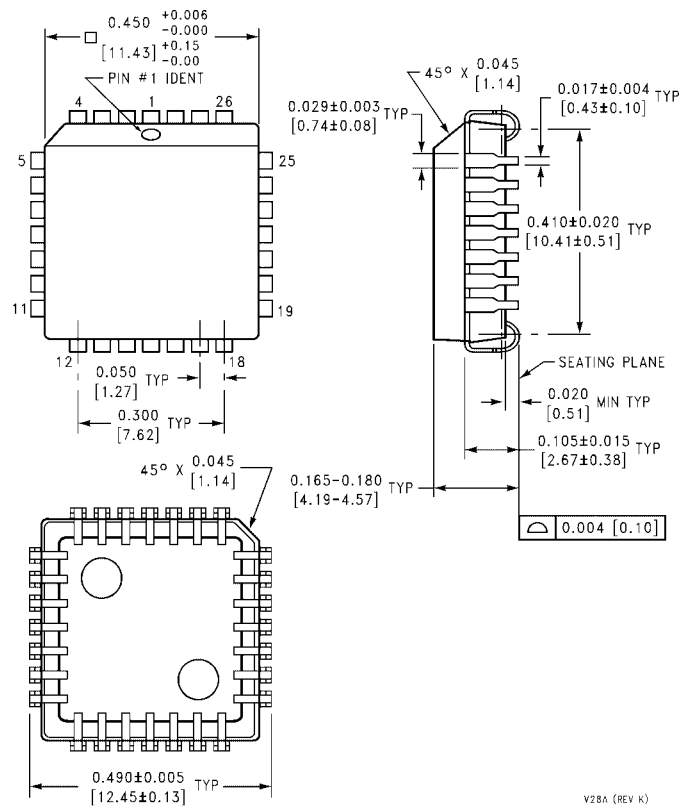
**Physical Dimensions** inches (millimeters) unless otherwise noted



N24E (REV A)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide  
Package Number N24E**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A**

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